

FPGA BASED ENCRYPTION DESIGN USING VHDL

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Abstract

The job of cryptographers is quite crucial as they are responsible to keep privacy of personal information and indirectly the protection of national security. The efficient encryption method ensures the information security. Here VHDL (Very high speed integrated circuits Hardware Description Language) and FPGA (Field Programmable Gate Arrays technology) are used for highly efficient encryption design to secure the information over open network transmission. The proposed work is a composite encryption technique comprised of transposition and substitution to generate complex encipherment. The design is implemented and tested in Xilinx ISE.9.2. A final result signifies the efficiency and reliability for FPGA (SPARTAN-3) device.

Keywords: VHDL, FPGA, Encryption, Xilinx ISE.9.2

1. INTRODUCTION

Encryption is used to transform information into an incomprehensible form. The input to the plaintext (or cleartext) and the output from it is called ciphertext (or cryptogram). The reverse process of transforming ciphertext into plaintext is called decryption (or decipherment). Notice that plaintext and ciphertext are a pair of respective notions: the former refers to messages input to, and the latter, output from, an encryption algorithm. Plaintext needn't be in a comprehensible form; for example, in the case of double encryption, a ciphertext can be in the position of a plaintext for re-encryption. Usually, cleartext means messages in a small subset of all possible messages which have certain recognizable distributions. In general ciphers can be distinguished into two types classical or modern according to the type of input data [7]. It should be useful to point out that the two basic working principles of the classical ciphers: substitution and transposition are still the most important kernel techniques in the construction of modern symmetric encryption algorithms. A combinations of substitution and transposition ciphers founded in two important modern symmetric encryption algorithms: Data Encryption Standard (DES) and Advance Encryption Standard, AES, [1].

A transposition cipher (also called permutation cipher) transforms a message by rearranging the positions of the elements of the message without changing the identities of the elements. Transposition ciphers are an important family of classical ciphers, in addition substitution ciphers, which are widely used in the constructions of modern block ciphers. Modern encryption methods can be divided according to two criteria [7]: the type of key used, and the type of input data. By type of key used ciphers are divided into:

1. Symmetric key algorithms (Private-key cryptography), where the same key is used for encryption and decryption.
2. Asymmetric key algorithms (Public-key cryptography), where two different keys are used for encryption and decryption.

The objectives of this work was to develop a modern technique using a combination of transposition and substitution techniques in order to present an efficient encryption design that help to produce secure cipher and can be more reliable . The paper also aimed to demonstrate how FPGAs can address the need for faster recovery. This encryption algorithm targeted for small embedded applications. It was initially designed for software implementations in controllers, smart cards or processors.

2. MATERIALS AND METHODS

2.1 Materials

The model design synthesizing and implementing (i.e Translate Map & Place and Route) VHDL code with FPGA device are completely done on Xilinx –project navigator ,ISE 9.2i .

2.2 Methods

In a substitution cipher, the encryption algorithm $e_k(m)$ is a substitution function which replaces each $m \in M$ (input data) with a corresponding $c \in C$ (cipher) The substitution function is parameterized by a secret key k . The decryption algorithm $D_k(c)$ is merely the reverse substitution. In general, the substitution can be given by a mapping [1]:

$$\pi : M \rightarrow C \quad (1)$$

And the reverse substitution is just the corresponding inverse mapping

$$\pi^{-1} : C \rightarrow M \quad (2)$$

The previous substitution function mapping explains the essence of this work. The base of encryption is to use unpredictable methods.

2.3 Algorithm

The described design algorithm illustrated in Fig (1) accepts 128 bit input data that is divided into 16(8-bit) sub-blocks. Two stages of encryption were required to process the accepted data. The design used different procedure for each one. The uses of double encryption stage makes it complex, this provides more authentication on the output cipher. The sequence events of algorithm are applied to each input byte.

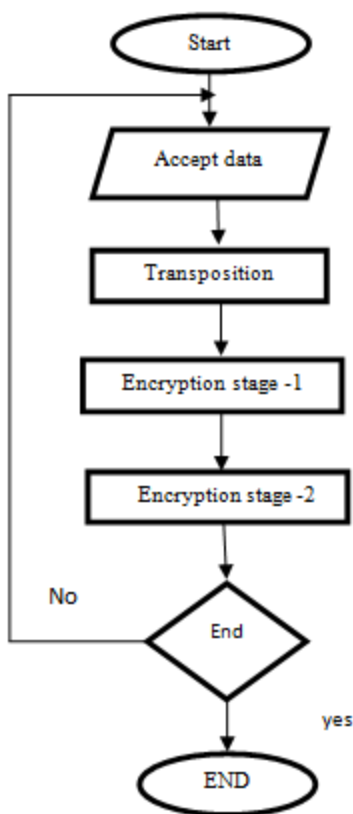


Fig 1: Algorithm Steps

Transposition stage used to improve the design reliability. The used transposition’s mechanism is described in fig (2). Each byte changes position following the illustrated path in the chart.

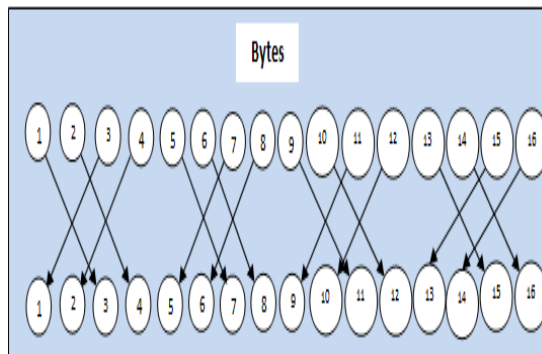


Fig 2: Transposition chart

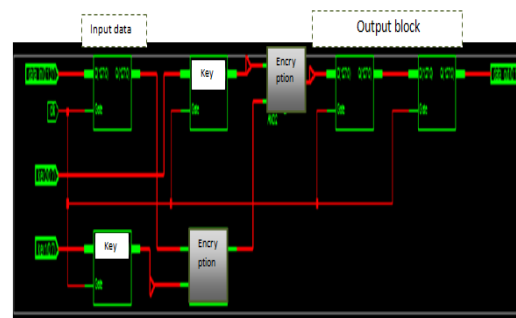


Fig 3: RTL design blocks

In general description the input block is responsible of dividing data into bytes also it performs the transpositions operation, and then data pass through two encryption blocks which consist of a logic combination ,each encryption block has its own key . Finally the output block, this is used to form the output cipher stream.

3. RESULTS

The simulation process applied using ISE VHDL simulator in order to ensure that the design is well performed. The test bench process results presented in fig (4) show the inputs and outputs parameters, the simulation used an FPGA device of Spartan3 type. The results accuracy approved the ability of using this design.

Device Family: Spatran3

Tools used:
o Xilinx ISE 9.2i

o ISE VHDL simulator.

o Device: xc3s1000-5fg675

3.1 Design Overview

The synthesis process used to transform the VHDL code into model design [4] illustrated in fig (3). It divided into blocks each one used to perform a specific function according to their internal logic composition. The design used the resources of the FPGA device. The complete design required about 128 of the 4 input LUTs in addition to 273 IOBs of the available device resources. However the top

model design view consists of four inputs and a cipher output. A clock unit links all blocks and used to control the input/output process.

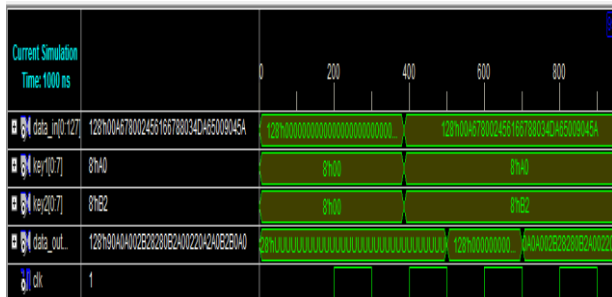


Fig 4: Behavioral simulation

By checking the results obtained from fig(4) it was clear obviously that the design works correctly similar to the previous algorithm illustrated in fig(1) . The test accomplished successfully without errors.

3.2 Device Performance

The following discussion focuses on the performance of various FPGA devices. Synthesis is carried out using different family’s types of Vertex and Spartan devices. Tables (1.upto 6) show the execution results of each device. The evaluating gives the opportunity to recognize the available resources of each device. It determines utilization ratio and time summary for each one. It is acknowledged that synthesis results are with some (approx.8) warnings which are allowable [6].

Spartan Devices Performance:

Table1: program synthesis using the device xc3s1000-5-fg676

| Spartan3(target device xc3s1000 package fg675 speed-5) | | | |
|---|------|-----------|-------------|
| Logic utilization | used | available | utilization |
| Number of slices | 230 | 7680 | 2% |
| Number of 4input LUTs | 128 | 15360 | 0% |
| Number of bonded IOBs | 273 | 391 | 69% |
| Number of CLOCKS | 1 | 8 | 12% |

Timing Summary:

Minimum period: 4.855ns (Maximum Frequency: 205.977MHz)

Minimum input arrival time before clock: 1.572ns

Maximum output required time after clock: 6.141ns

Total delay of the output data path : 6.141ns (5.460ns logic, 0.681ns route).

The number of signals not completely routed for this design is: 0

The average connection delay for this design is: 1.078

The maximum PIN delay is: 3.584

The average connection delay on the 10 worst nets is: 3.239

4. DISCUSSIONS

To be more reasonable in our evaluating it should be known that other factors such as power consumption and device cost should be account in particular when the evaluating expands to cover other known designs that work in the same field [2]. The implementation results lead to observe that in terms of area requirements It was no doubt that this design generally exhibits the smallest hardware consumption than the implementing design in [5] .Also it should be noted that the implementing design is almost faster and has less delay time compared to [5]. Finally it was known according to [3] that Spartans devices have low cost than Virtex

5. CONCLUSIONS &RECOMMENDATIONS

Today’s connected society requires secure data encryption devices to preserve data privacy and authentication in critical application, this helps for developing more researches works to improve the ordinary using of encryption techniques . This work develops a secure encryption system that used FPGA technology in order to provide fast recovery .The paper studied most of the known encryption methods. The design performance was examined to different families of FPGA devices. Future work can be performed to allow more complexity by using additional techniques such as using one of the keys as a public key and the other can be used as private key. Also expanding keys will be useful.

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