16nm BULK CMOS DOCCCII BASED CONFIGURABLE ANALOG BLOCK DESIGN FOR FIELD PROGRAMMABLE ANALOG ARRAY

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Abstract

Field programmable analog array (FPAA) is a rapidly growing technology for fast prototyping of analog signal processing systems facilitating the quick innovation at industry level with saving in terms of both time and cost. Analog signal processing is much faster and consumes less power than conventional digital signal processing, justifying the need for FPAA. Here we propose a Dual output current controlled current conveyor (DOCCCII) in 16nm bulk CMOS technology using PTM (High Performance 16nm Metal Gate / High-K / Strained-Si parameter) and discuss its characteristic. DOCCCII is superior in design among Current Conveyors because it requires no additional resistance for activation, it has it's own parasitic resistance tunable through biasing current and has high bandwidth (GHz range). A configurable analog block (CAB) is also proposed which mainly consists of the DOCCCII readily configurable to realize an application. This cab is used here for the realization of 2nd order filters.

Keywords— *FPAA, Configurable Analog Block, DOCCCII, Electronically Tunable Circuit Design*

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1. INTRODUCTION

Recently, the demand for FPAA's is increasing because it facilitates rapid prototyping and saves design time, design efforts, testing time and cost. It provides a platform for new innovation in analog domain, as complex circuits can be implemented on FPAA in short time by the end user. Substantial work on FPAA based on current mode has been reported in many important publications [1-5]. This work can be considered significant on the basis of various design matrices like high frequency [3,4], low power and low voltage [5] etc. Among different current mode circuits it is clear that current conveyor (CC) plays an important role in analog designing such as signal processing , instrumentation [6-8], and is a versatile building block for the present day scenario of low voltage low power VLSI [6,9,10]. A CC offers both low impedance input and high impedance input nodes simultaneously along with a voltage virtual short among the various input nodes like a conventional OPAMP [9, 10]. It exhibits improved slew rate [11,12], very high gain bandwidth product [13-14], larger dynamic range, greater linearity, small chip area, low power consumption [10,15] and Current controlled current conveyor (CCC) is another version, which exhibits a considerable resistance at the low impedance or current input (node X). It is reported that a CCC is more flexible [16] basically analog but extendible to digital applications [17-19]. Applications like passive comparator, regenerative comparator [19] ,D flip flop [17], XOR/XNOR [18], CMOS clock generator etc. can be seen in literature. A practical CC is deviation from ideal behavior, known as non-idealities [16, 20]. Some of these non-idealities play important roles, e.g. the parasitic resistance at the low impedance node (R_X) leads to define a CCC. Likewise, other non-idealities also sometimes exhibit similar favorable effects [20]. Current negation and current duplication is very easy to obtain in case of a CCC, leading to DOCCC, MOCCC etc. 2nd generation is generally preferred, therefore CCCII, DOCCCII etc. are readily seen in literature. Here in this paper we design two configurable analog blocks (CAB) using the translinear DOCCCII, realized in 16nm bulk CMOS Technology using the PTM [21] CMOS model parameters.

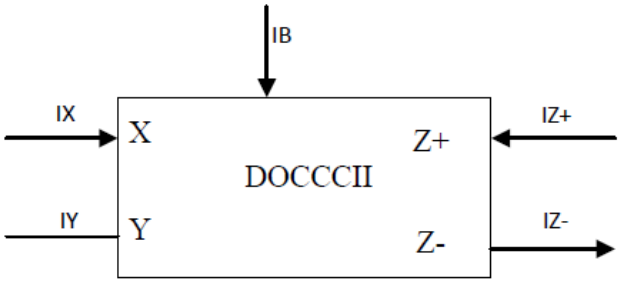


Fig 1- Block diagram representation of the dual output CCCII

Here,

$I_{Z+}= I_X$, $V_X=V_Y +I_XR_X$, $R_X=1/(g_{m2}+g_{m4})$

$I_{Z-}= -I_X$, $I_Y=0$, $g_{mi}=\sqrt{(2\beta_i I_B)}$ $i=(1,2,3....n)$

2. CIRCUIT DISCRIPTION OF DOCCCII

CCCII has parasitic resistance RX at the current input node and is tunable by the biasing current IB [15,20]. A DOCCCII can provide an output current signal and it's quadrature signal simultaneously. The equivalent circuit symbol and the principle equation of DOCCCII are given in Figure 1.

The CMOS implementation of a class AB DOCCCII is presented in Figure 2. The circuit consists of a translinear loop consisting transistors M1 – M4. Two MOS current mirrors (M5 – M6 and M7 – M8) are used to bias the translinear loop with bias current $I_{B,}$ the input cell presents a high input impedance at input port Y and a low input impedance at input port X. This cell acts as voltage follower. The current at node X is copied to output nodes Z+ and Z–. Currents Id18 and Id14 are cross-coupled through transistors M14, M15, M18 and M19 to generate negative current at Z-node. Details are shown in circuit below.

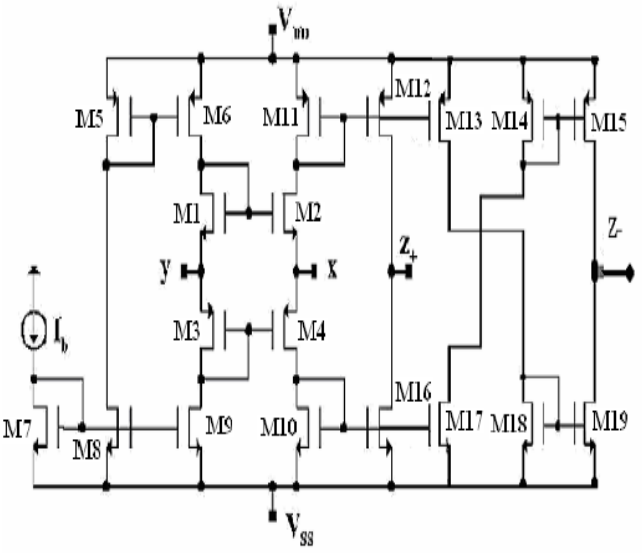


Fig 2- Implementation of translinear DOCCCII

3. DOCCCII BASED CAB

A CAB is a block which can realize an application configurable in user domain. In the present work a pair of CAB's is proposed which can accommodate a larger application spectrum, particularly, the quadratic or bi-quadratic applications, including various analog filters and sinusoidal oscillators.

The CAB-1 contains a DOCCII, a capacitor at node Z+, and NMOS switch S1.

The CAB-2 contains a DOCCCII, a conjoin of capacitor and resistor at node Y, a capacitor at node Z- and X and switches S2 – S8. These CAB's are presented in Figure 3 and 4. In order to include the required capacitors and resistor respective NMOS switches associated with them are closed to configure the CAB's for a given application. A number of these CAB's can be used to construct FPAA and connected together through the switching matrix to realize variety of different applications.

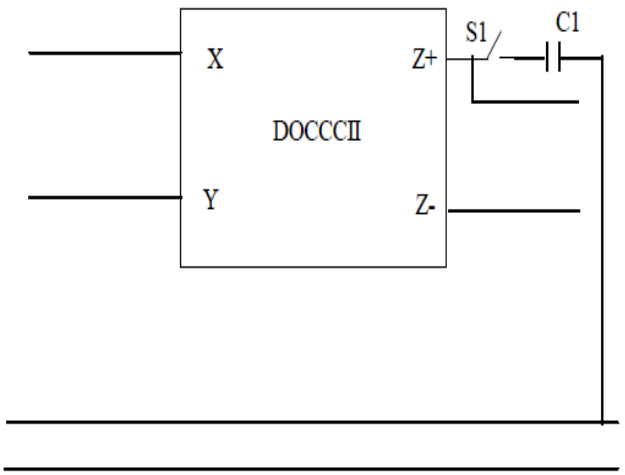


Fig 3- CAB 1

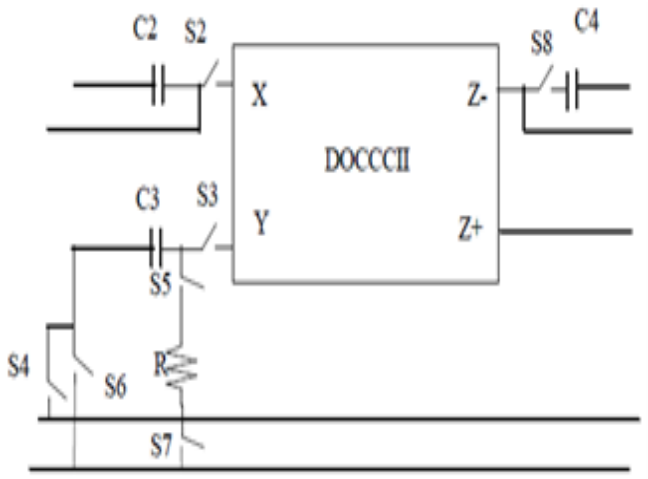


Fig 4- CAB 2

The switch is no more ideal, but is a jargon of large number of non-idealities like offset voltages and currents and various parasitic resistances, inductance and a large number of capacitances. Some of them are important in consideration with FPAA scheme as their effects are dominant. Therefore consideration is that their effects do not alter the circuit performance altogether. Here in this work we try to swamp the switch dominance over the application. For this purpose, an estimate is made for the total effect of various capacitances connected to a node and is assumed as a lumped model of the total capacitance at the node (e.g. C_{GTOTAL}), also suggested by HSPICE. Besides this, channel resistance is also considered in our model. This model is affected by adjusting the external capacitance values and the switch aspect.

4. SIMULATION RESULTS

The performance of the DOCCCII and the CAB's based on it are verified by performing H-spice simulations. The utilized aspect ratios of the DOCCCII are given in TABLE II and the simulation results are summarized in TABLE I. AC analysis and bandwidth plot in Figure 5.

TABLE I: CHARACTERISTICS OF THE DOCCCII

Current gain	1.0996
Bandwidth	12.2825GHZ
Input resistance	27Kohm
Output resistance	645.681Kohm
Total power dissipation	53.25uwatt

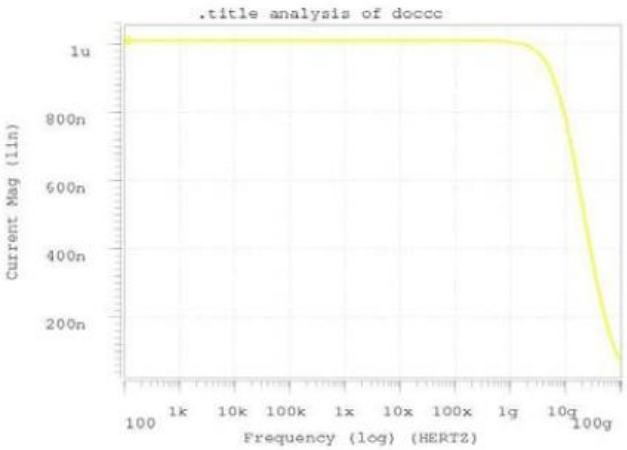


Fig 5: AC analysis for node Z+ at IX=1uA.

The working of the proposed models is demonstrated by running an application with the original circuit on as it is basis and then the same application is realized by using the CAB's which are shown in Figure 3 and 4.

TABLE II: ASPECT RATIOS OF TRANSISTORS OF DOCCCII

Transistors	W(nm)	L(nm)
M1,M2, M5,M7,M8,	32	64
M10,M13,M14,	32	64
M17,M18	32	64
M3,M4	64	64
M6,M9,M11,M12	64	64
M15,M16,M19	64	64

The applications realized include second-order low-pass, band-pass and notch pass filters from the already published work. The results show the waveforms are given in Figure 7(a), 7(b) and 9 and the results are summarized in TABLE III. In Figure 6(a) a filter structure given in [22] is realized using the designed CAB-2 respective switches are closed namely (S2,S3,S5,S6,S7). In figure 8(a) a current mode filter structure given [12] is realized using both the CAB's and the required components are included by closing switches (S3,S6,S8). In simulation results shown in Figure 7(a), 7(b) and 9 the first waveform shows response of filters realized without CAB and the second waveform shows response of filters realized using CAB. The two CAB's will be connected by interconnect matrix on the FPAA not shown here.

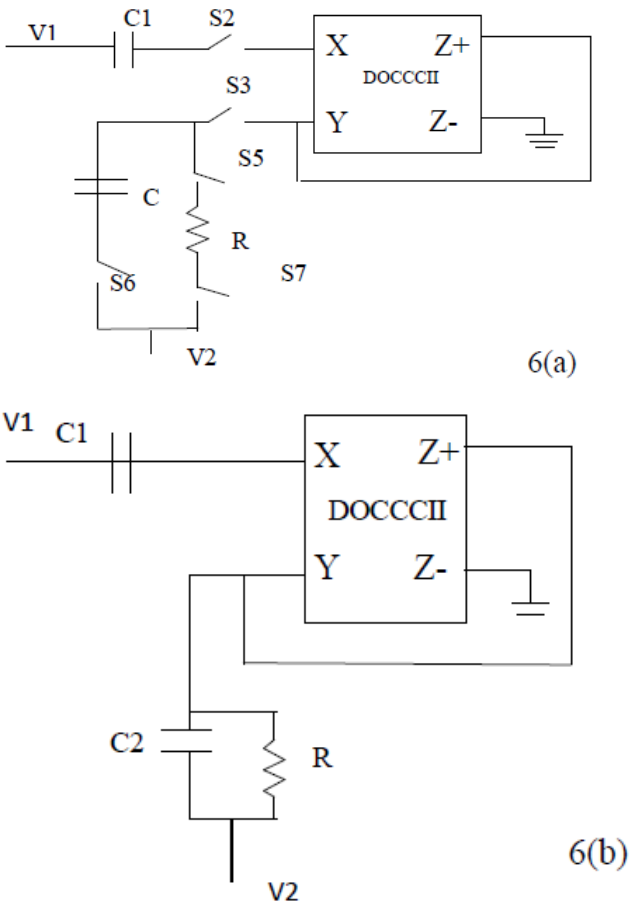


Fig 6 (a) & 6(b) - realization of filter using CAB and without CAB

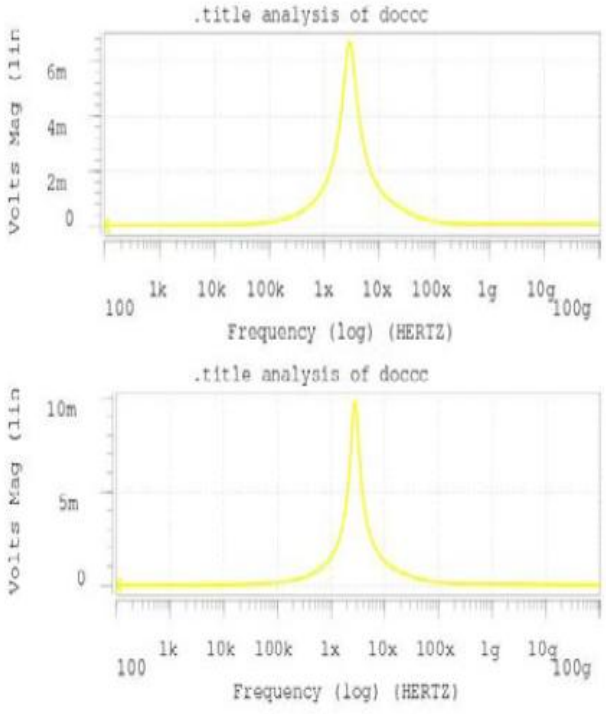


Fig 7(a) - Simulation response of notch pass filter using figure 6(a) and figure 6(b)

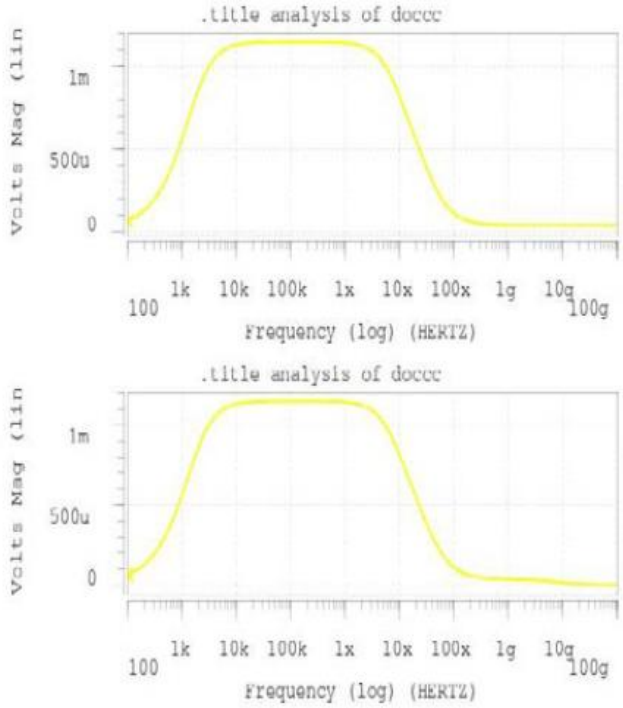
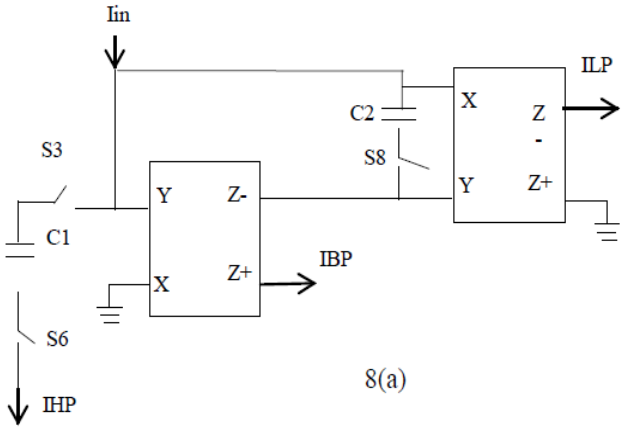


Fig 7(b) - simulation response of band pass filter using figure 6(a) and figure 6(b)



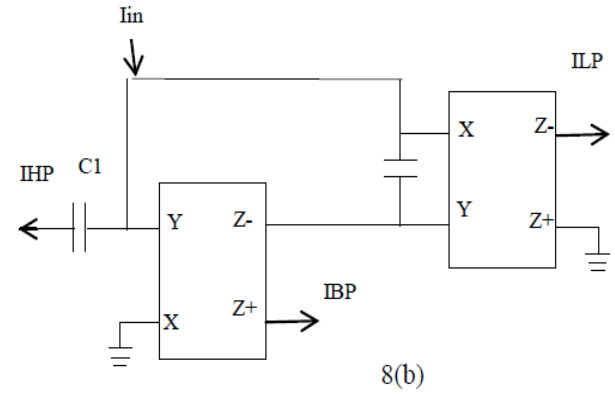


Fig 8(a) & 8(b) - realization of filter using CAB's and without CAB's

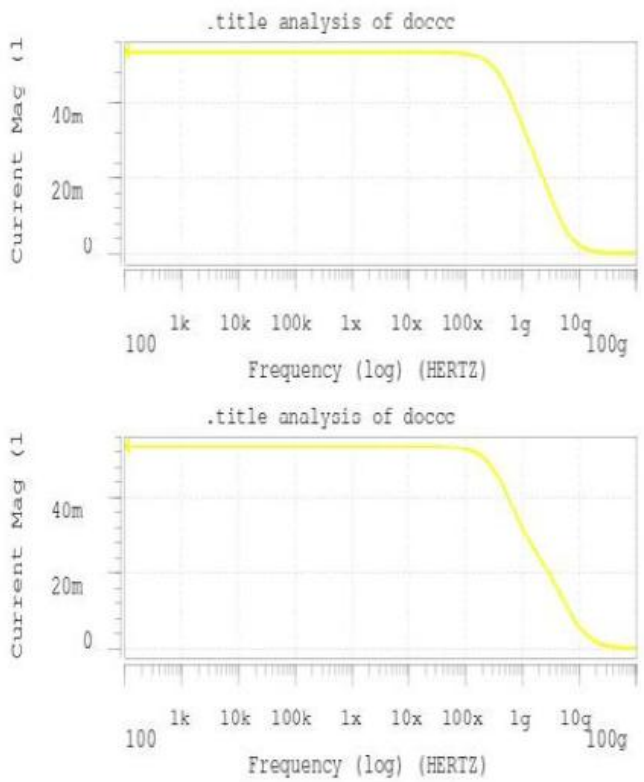


Fig 9-Simulation response of low pass filter using 8(a) and 8(b)

TABEL III: COMPARISON OF SIMULATION RESULTS

	Without cab		With cab	
Name	Bandwidth	Peak voltage	Bandwidth	Peak voltage
Figure 7(a)	1.67515 Mhz	6.70067 mv	1.07323 Mhz	9.810 mv
Figure 7(b)	1.01131 Mhz	1.1459 mv	1.00113 Mhz	1.1463 mv
Figure 9	792.775 Ghz	.5376mv	658.040 Ghz	.5370 mv

5. CONCLUSIONS

A new design for configurable analog block based on DOCCCII for high frequency applications is proposed. Using these CAB together with programmable interconnect FPAA can be constructed which will efficiently realise a number of 2nd order filter topologies, oscillators and amplifiers.

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