DESIGN OF RING VCO USING NINE STAGES OF DIFFERENTIAL AMPLIFIER

Er Fahmida Khatoon[1], Er Tarana A chandel[2]

[1]*Department of Electronics & Communication Engineering, Integral University, Dasauli Kursi Road Lucknow 226026*

[2]*Department of Electronics & Communication Engineering, Integral University, Dasauli Kursi Road Lucknow 226026*

Abstract

The proposed ring oscillator is fundamentally constructed by cascading series of delay cells, complying with the Barkhausen oscillation criterion of gain and phase shift. Focusing the need of low voltage design, which leads to an increased delay cell integration The number of delay cell reflects a high speed with low power consumption. Barkhausen criterion highlights the need of increased number of cascade differential amplifier based delay cell. To overcome the constraint of power dissipation, VCOs with reduced number of delay stages and the operation of sub threshold region has been widely used. In this paper a low power voltage controlled ring oscillator is implemented using the 250nm CMOS technology provided by generic with 2.5 volt power supply. The circuit is a modification of conventional ring oscillator. In favor of easy implementation of the module in small die size a nine stages of differential amplifier has been adopted to fabricate the proposed VCRO. The optimization design are done using S-EDIT software to make the oscillator as small as possible. In, addition Tanner tools is used in the analysis and simulation to verify the predicted performance. The proposed design is suitable for PLL and Timer circuits. The optimized ring oscillator is then compared with the previous design done by other researchers. The existence of various topologies of high-frequency ring oscillator highlight an essential design breakthrough optimizing to the power dissipation and tuning range of 125 MHz-561.798 MHz. The ring oscillator is able to operate with 2.5v supply and consuming around 3.6mwatt.

Keywords— *VCRO, CMOS, Low Power, Differential Amplifier*

----------***----------

1. INTRODUCTION

Now a day's communication is most necessary thing in the world. The wireless communication contains many transceivers such as low-noise amplifiers, power amplifiers, mixers, digital signal processor, filters and phase-locked loops [1].Voltage Controlled Oscillators is an electronic oscillator whose oscillation frequency is controlled by a input voltage. The frequency of oscillation is varied by the applied input voltage. An ideal voltage-controlled oscillator is a circuit whose output frequency is a linear function of its control voltage[2]. Voltage controlled oscillators are used for high speed clock generation, channel selection, frequency modulation and demodulation in various communication circuits. In the modern communication systems, there is a calculated gap between the adjacent channels for the efficient use of frequency spectrum. Like an oscillator, VCO may be considered as an amplifier and feedback loop. For the circuit to oscillate, the total phase shift around the loop must be 360 degrees and the gain must be unity. VCO is one of the important basic building blocks in analog and digital circuits as like in PLL. A PLL comprises of phase detector (PD) ,low pass filter (LPF) , voltage controlled oscillator (VCO) and frequency divider in Fig 1.In this type of PLL - based frequency synthesizer, the most power hungry module is VCO, which generates frequency and changes the oscillation frequency. In the PLL the incoming communication signal is demodulated with the help of a synchronized VCO signal. The output frequency of VCO varies with respect to a reference frequency. Reference frequency is compared with the VCO output frequency, which generates an error signal. This is the control voltage for the VCO.

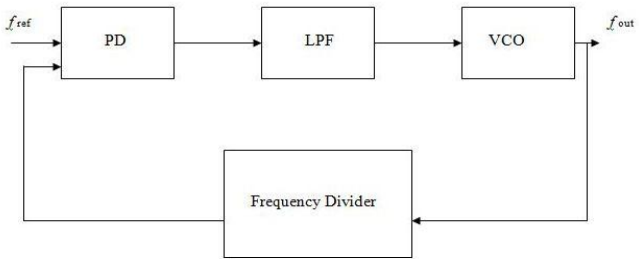

Fig. 1 Block Diagram Of PLL

Till today, generally LC-type and RC- type of CMOS VCOs have been used in wireless communication systems [3].So far LC based VCO has low level of phase noise among all CMOS VCOs. However, it has narrow tuning range, greater power dissipation and large die area[4].In addition, it is very difficult to integrate inductor in digital CMOS technology. These shortcomings of LC-VCO are overcome by a ring based VCO or sometimes called as VCRO. Ring VCO have wide range of frequency swing and easy to implement. Ring VCO also occupy less chip area as they do not have inductor as compared to LC-VCO.

There are two kinds of ring VCOs:- single-ended and differential ring VCOs.[5].The delay cell for the single-ended VCO is a basic inverter and has the highest frequency of oscillation and minimum power dissipation. To replace the by-pass and coupling capacitors, differential ring VCOs can be used [10] –[11].The dual loop technique in a differential VCO increases the oscillation frequency and reduces the phase noise.

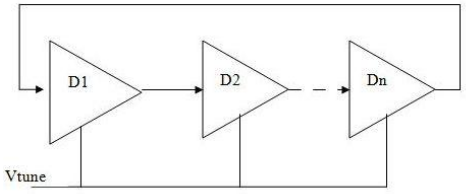

Fig.2. Single-Ended Ring VCO

In the Fig.2. D1 to Dn represents the delay cells,which provide the gain and phase shift.They construct a close loop by cascading all stages.

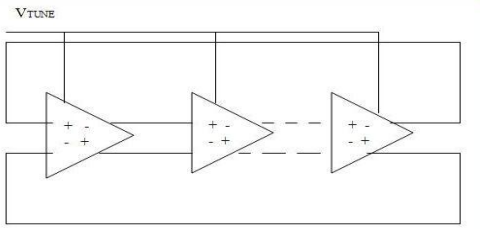

Fig.3. Differential Ring VCO

The above Fig.3.depicts an N-stage ring oscillator realized using differential cells,which have complementary outputs.It is widely used, since it has a differential output to reject common-mode noise, power supply noise.

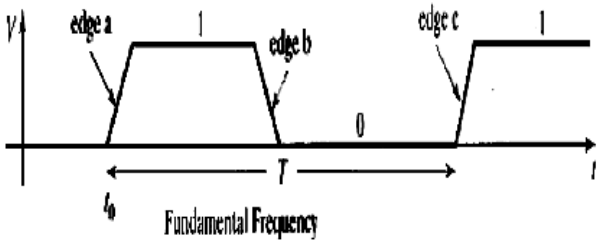

Fig.4. Fundamental Frequency

In the above Fig.4. t_P is defined as propagation delay through each stage , so period T is defined as T=2 N t_P .For a single-ended output cell ,N has to be odd,but for differential cell N can be odd/even , to start an oscillation .

A nine stages voltage controlled ring oscillator is designed using 250nm CMOS technology. The voltage applied to the VCO is 2.5 volt. The output frequency varies from 125 MHz to 561.798 MHz at Vtune=1V to Vtune=2.5V respectively. The overall objective is to design a robust VCO with minimum power consumption.Vtune is control or tuning voltage.

2. VCO DESIGN CONSIDERATIONS

2.1 Proposed Differential Amplifier

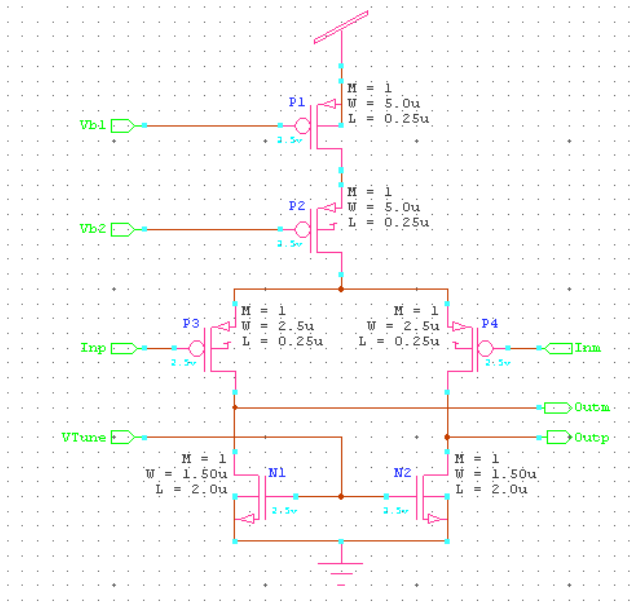

Fig.5. Designed differential amplifier

In the fig.5. differential amplifier consists of two PMOS at the top, two in the middle and two NMOS at the bottom. The two PMOS, P1 and P2 have Vb1 and Vb2 as inputs respectively. These PMOS are biased in the linear region and hence they act as active resistors. The resistance may be denoted as Ron. The two PMOS, P3 and P4 are the main driver MOS with inputs as Inp and Inm. The two NMOS, N1 and N2 are both controlled by tuning voltage Vtune. Therefore they act like constant current source to bias the differential amplifier circuit. The current flowing through them is controlled by Vtune.

Table 1: Size of Devices

Device	W/L
P1,P2	20
P3,P4	10
N1,N2	1.25

2.2 Ring VCO

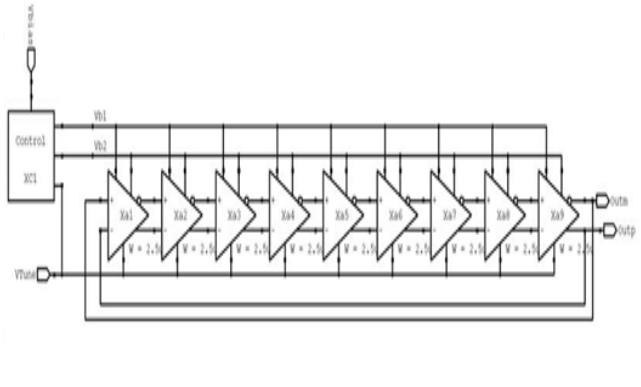

Fig.6. Ring VCO using nine stages of delay cells

The above Fig.6. depicts 9-stages of ring VCO realized using differential cells. The propagation delay of each cells equals to RC time delay. Therefore, as the number of cells increases the RC time delay also increases. The Vb1 and Vb2 act as control voltage of the Ring VCO. If the Vb1 or Vb2 is changed, the resistance R in RC time delay also changed. The parasitic capacitance C is not possible to change, hence only R can be controlled. Propagation time delay (Td) can be controlled by changing the voltages Vb1 and Vb2 and by changing this propagation time delay the frequency fout can be changed.

2.3 Control Circuit of VCO

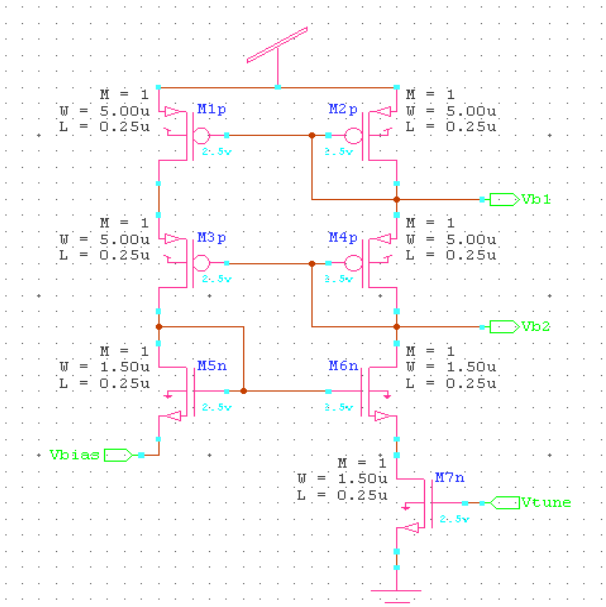

Fig.7. Control Circuit used in VCO

The circuit shown in fig.7 is the control circuit of the voltage
controlled oscillator. There are two arms with two PMOS and one NMOS in each of the arm. Vtune controls the current flows in the circuit. It is basically a cascade current mirror circuit. Vb1 and Vb2 voltages are controlled by this control circuit. If this Vbias is increased, the current flow decreases. This is because current flow depends upon gate to source voltage and drain to source voltage. By varying this current, the current flow in the left arm changes. Now as the circuit acts like a current mirror, the current flow in the other arm also changes.

3. SIMULATION RESULTS AND P PERFORMANCE COMPARISON

The proposed Voltage Controlled Ring Oscillator is implemented in 250nm CMOS technology. We performed spice simulation for proposed circuit by using Tanner EDA software; we use S-Edit, T-Spice and W-Edit as a simulator. The supply voltage required for this VCO is 2.5V.

Performance comparison is given in table 2,where it is shown that the power consumption is least in this work.

Fig.8.shows the transient response at Vtune = 1 V with oscillation frequency Fosc = 125 MHz. Similarly Fig.9. shows the transient response at Vtune = 2.5 V with oscillation frequency Fosc = 561.798 MHz.

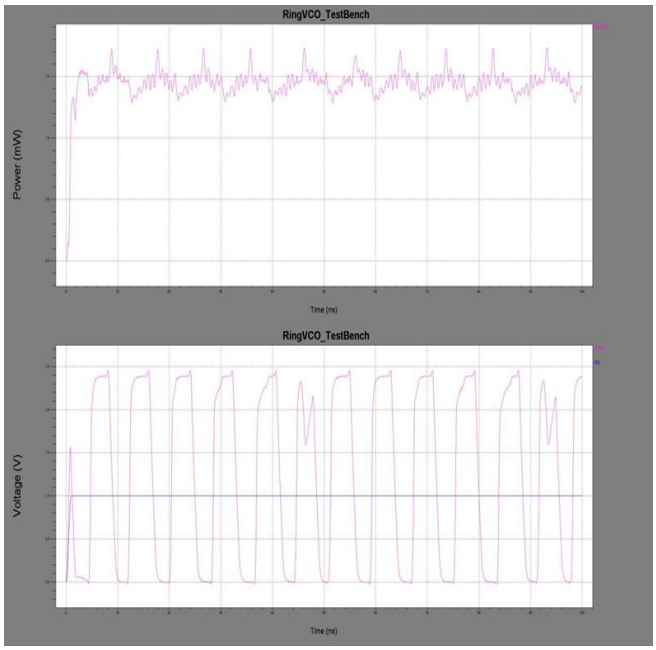

Fig.8. Transient response at Vtune = 1 V

Fosc = 125 MHz
Transient Power at Vtune = 1 V
Pavg = 1.1 mW

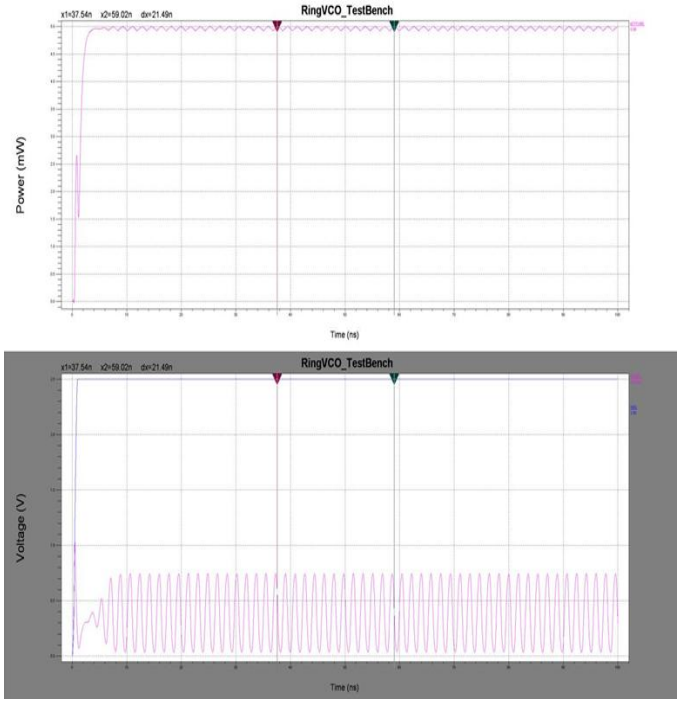

Fig.9. Transient Response at Vtune = 2.5 V

Fosc = 561.798 MHz
Transient Power at Vtune = 2.5 V
Pavg =3.6 mW

Table 2: Performance Comparison

Reference	Process Technology	Type	Power(mW)	Supply Voltage (Volts)
[6]	0.18 µm CMOS	Hartely VCO	6.75	1.8
[7]	0.18 µm CMOS	Colpitt VCO	6.4	1.8
[8]	0.18 µm CMOS	Ring VCO	27	1.8
[9]	250 nm CMOS	Ring VCO	5	2.5
This Work	250 nm CMOS	Ring VCO	3.6	2.5

4. CONCLUSIONS

The proposed voltage controlled oscillator is fabricated in 250nm CMOS technology. The VCRO is design by using the Tanner EDA V13 software. From Circuit simulations, the frequency varies from 125 MHz to 561.798 MHz by adjusting the tuning voltage from 1 Volt to 2.5 Volt. The low power consumption is achieved which is around 3.6 mW at 561.798 MHz.

REFERENCES

[1]. Rashmi K Patli,M.A.Gaikwad and V.G,Nasre,"Area Efficient Wide Frequency Range CMOS Voltage Controlled Oscillator For PLL Inn 0.18µm CMOS Process",IJERA,Vol.2,PP.1696-1699.

[2]. Behzad Razavi,"Design Of Analog CMOS Integrated Circuit",Tata McGraw Hill pvt Ltd,Edition 2002,Eighteenth reprint 2010.

[3]. M. Moghavvemi and A. Attaran, "Performance review of highquality-factor, low-noise, and wideband radio-frequency LC-VCO for wireless communication," IEEE Microw. Mag.,vol. 12, no. 4,pp. 130-146, June 2011.

[4]. M. Moghavvemi and A. Attaran, "Recent advances in delay cell VCOs," IEEE Microw. Mag., vol. 12, no. 5, pp. 110-118, August 2011.

[5]. Jie Ren,"Design Of Low Voltage Wide Tuning Range CMOS Multipass Voltage-Controlled Ring Oscillator" Dalhousie University,Nova Scotia,March 2011.

[6]. S-H. Lee, Y.-H Chuang, S.-L Jang and C.-C Chen, "Low phase noise," IEEE Microwave and Wireless Components Letters Vol. 17, No. 2, PP. 145–147, February 2007.

[7]. J-A. Hou and Y.-H.Wang, "A 5 GHz differential Colpitts CMOS VCO using the bottom PMOS cross couple current source," IEEE Microwave and Wireless Components Letters Vol. 19, No. 6, PP. 401–403, June 2009.

[8]. Y. A. Eken and J. P. Uyemura, "A 5.9-GHz voltage-controlled ring oscillator in 0.18-µm CMOS," IEEE J. Solid-State Circuits, vol.39, No. 1, pp. 230-233, January 2004.

[9]. Mrs. Devendra Rani and Prof.Sanjeev M.Ranjan,"A Voltage Controlled Oscillator Using Ring Structure In CMOS Technology",International Journal Of Electronics And Computer Science Engineering Vol.1,No.3,ISSN 2277-1956.

[10]. C.H.Park and B.Kim, "*A low noise ,900 MHz VCO in 0.6- µm CMOS,*" IEEE J.Solid- State Circuits, vol. 34,no. 5, pp. 586-591,May 1999.

[11]. G. Haijun, S. Lingling, et al, "*A* low- phase- noise ring oscillator with coarse and fine tuning in a standard CMOS process," IOP Science Journal of Semiconductors, vol. 33,no. 7, July 2012.