

RECONFIGURABLE AND VERSATILE BiRC ARCHITECTURE DESIGN WITH AN AREA AND POWER EFFICIENT TECHNIQUE

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Abstract

Coarse Grained Reconfigurable Architecture based systems have become increasingly important in these days. In order to handle multiple applications with low area and power requirement, a new coarse grained reconfigurable architecture (CGRA) is exhibited here. The architecture which is named BilRC, Bilkent Reconfigurable Computer manipulates an execution-triggering mechanism. By mapping real-world applications, the adaptability of the architecture and the computation model are justified. BilRC design is done by using Xilinx and analysis of Area and Power are done. The proposed architecture design can also be implemented by mapping the applications to a 90-nm FPGA array. The model minimizes the configuration size to about 33 times. The design is further developed leading to a new architecture design so as to support multimedia applications. One of the distinguishing features of the proposed BilRC architecture is that the hardware and the programming language are code signed. The simulation results show an increase in the performance by reducing the power consumption to 92%. The design is synthesized with 90-nm technology, and the mapping applications on BilRC run faster than those on FPGA about 2.5 times. The expectation from BilRC is the replacement of FPGAs with BilRC in Coarse Grained Applications.

Keywords : CGRA, FPGA, execution Triggering, BilRC, coarse grain

1. INTRODUCTION

Recent progress in the field of reconfigurable computing have paved way to the development of many sophisticated choices regarding reconfigurable architectures for various applications. Data streaming applications, such as signal processing, multimedia applications and data encryptions, are the dominant workload in many electronic systems. High Performance with stringent power budget is the constraint of such applications. Because of the rapid advancement in architectures for algorithms and applications in DSP, there has been an increasing demand for the computing platforms to be easily adaptable, low cost while consistently delivering maximum performance at all times. Coarse grained reconfigurable (CGRA) solutions cater to this demand to some extent, with their high level of flexibility and more efficient routing structures. As a solution, General purpose programmable digital signal processors(DSPs) are widely used in conventional data-path oriented applications due to their flexibility and ease of use. However, DSPs lag due to their sequential software execution. Next, the application specific integrated circuits (ASICs) become a customized solution to meet these ever increasing demands. ASICs generally have fixed data flow with predefined functionalities that makes them unable to accommodate new system requirements or changes in standards[2]. ASIPs with dedicated memory architecture and instructions for FFT was discussed in [3]. As a solution to meet the emerging applications, FPGAs are developed.As opposed to ASICs, where the device is custom built for the particular design, FPGAs can be programmed as per the application or functionality requirements. But FPGA lags performance

during its runtime programmability for high volume applications.

Instead of the FPGA use, the employment of CGRAs is constructive because the pathwidths are greater than 1 bit here. This is because of the fact that huge routing area overhead and poor routability of the fine-grained architectures are sizably less efficient. Comparisons were done previously depending upon the interconnection networks on various CGRAs., datapath granularities as well as mapping.[4]. Reconfigurable structures with computation elements as heterogeneous, namely FPGA and CPU, were discussed by Compton et al. [6] According to the proposal in the works [4]–[6], Reconfigurable Architectures can be branched into single-time configurable, statically reconfigurable, and dynamically reconfigurable configuration depending upon the configuration type. Also, the execution control of the CGRAs can be statically scheduled type or dynamically scheduled. Architectures with Coarse grain strategy allows CFBs at operator level, datapath at word level, datapath routing with powerful area-efficiency.

2. EXISTING BiRC ARCHITECTURE

The architecture of the BilRC is based on coarse grained computing that enables standard performance, better flexibility than the other previous architectures. BilRC is destined to be a novel CGRA system targeting at applications with very high throughput requirements. The main aim of the BilRC architecture is towards Low Power, High Flexibility, Shorter compile time, High clock frequency, Efficient Space Usage, User friendly developing

Programming and Very High Performance. BiIRC exhibits a segmented interconnect architecture and so the Processing Element (PE) is designed. The execution depends totally on the PE for the architecture. BiIRC is classified as

- Arithmetic logic unit
- Memory and
- Multiplier

With respect to Processing Element

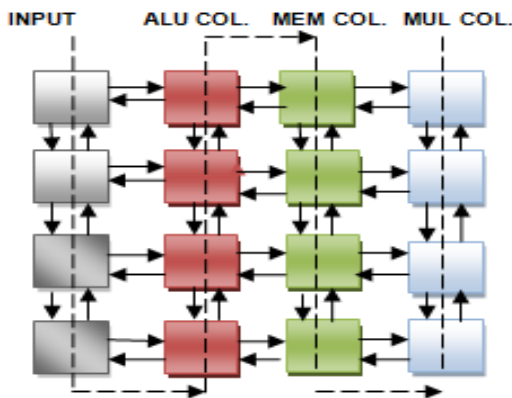


Fig – 1: Columnwise allocation of PE

As seen in some viable architectures of FPGA, PEs are organized in a row column format with identical PEs are arranged in the similar column. PEs are arranged in such a way that each PE is connected to four adjacent ones through communication channels[5]. Channels which are at the periphery of the structure are used to connect them to the external world.

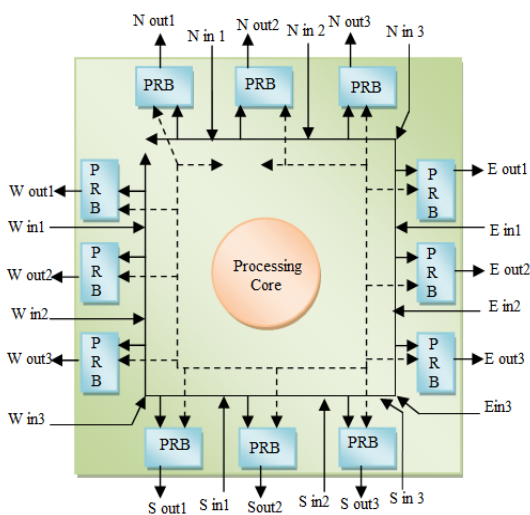


Fig - 2: Input/output signal connections of PE

Each PE is characterized by three inputs and three outputs. Interconnection is done by the connection of input and output of the PE. The 17 bits constitute the input output signals out of which data bits constitute 16 bits. The last 1 bit is the Execute enable bit (EE). Control signal is the Execute Enable bit. In the middle of every PE, Processing

cores (PC) are situated. Signal routing takes place at the sides where Port route boxes (PRB) are there. It is used for routing the PC output in the particular direction.

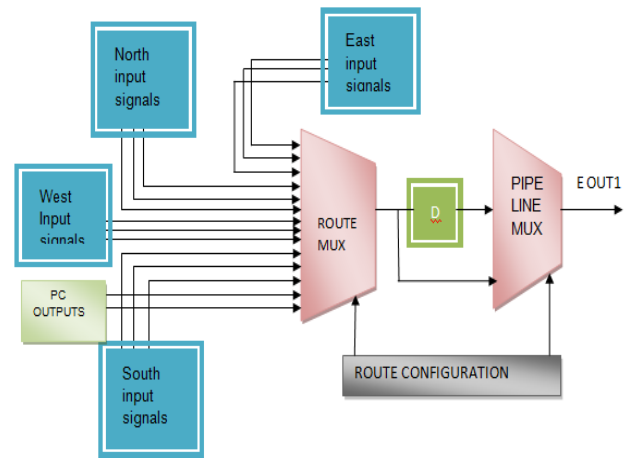


Fig – 3: Internal structure of PRB.

ALUs and MULs have two PC outputs and MEM has one PC output. Internal multiplexers are used by the PC to select the input signals. The response from various directions are fed to the route multiplexer which is got from the PC and those directions. The multiplexer employed here has the characteristic of pipelining. The output which is fed from the route multiplexer is delayed for one clock period by the pipeline multiplexer. The configuration of the BiIRC is done statically, hence both the interconnects and the instructions programmed in PCs remain unchanged at the run time.

3. PC ARCHITECTURES OF BiIRC

3.1 Memory Architecture

PC architecture of the Memory is characterized by 2 buses namely a DATA bus and an EE bus. The Dual port Sis of the size 1024 × 16

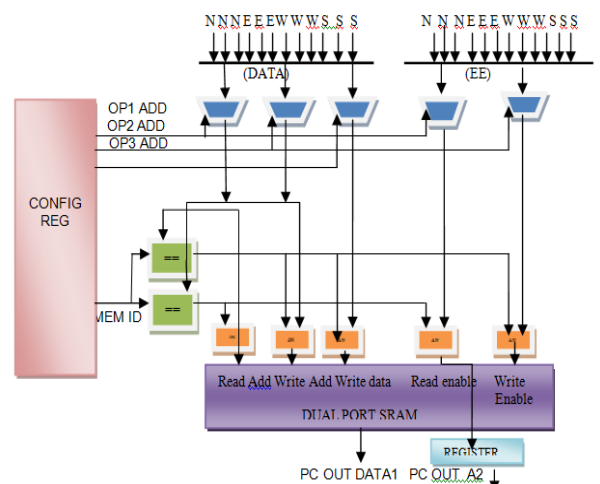


Fig – 4: Memory Architecture

OP1 Address is assigned by the configuration register (CR). The decision of which one among the 12 Inputs portrays the read address is selected by the OP1 address. Write Address is chosen by the OP2 Address. CR has a Mem ID and the comparison is done with the most significant six bits. If both values are detected as equal, correspondingly either A Write as well as Read or any one of the operations are performed. Data to be written from one of the input ports is selected by the OP3 Address.

3.2. ALU Architecture

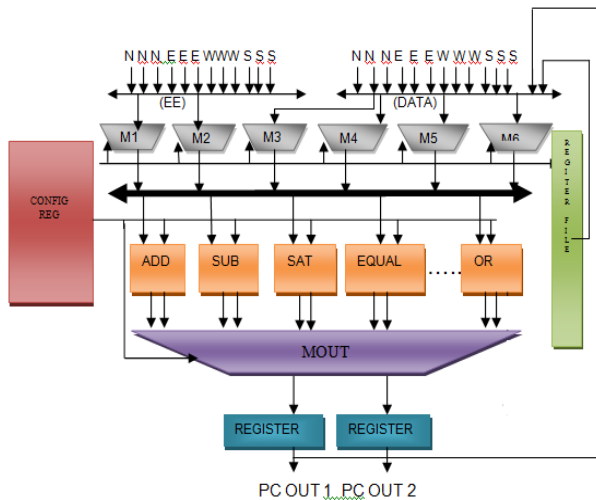


Fig – 5: ALU Architecture

There are two buses in ALU. One for the input data and the other for EE signals. The Multiplexers selects the corresponding operands as per the instructions from the data bus. Data operands which are of constant type are stored in the register file of size 8x16. the control bit here is the EE bit and it controls the execution of the program and instructions. By enabling the particular code of the corresponding operation, the multiplexer selects and the desired operation is performed by the PC.

3.3. Multiplier Architecture

The operation of the Multiplier is the same as that of ALU. The PE performs the Multiplication and shift operations. Two operands which can be either of constant type or variable type can be multiplied and therefore the output is a 32 bit value. Multiplication is performed in one clock period and shifting is performed in the other period. There is a need of two clock cycles for manipulating each instruction. Here Wallace tree multiplier is employed and for the addition Ripple Carry Adder is used. Both save area and Power thus contributing to the overall performance.

4. PROPOSED BiIRC ARCHITECTURE

The main issue of the conventional BiIRC architecture is all about the cost and hardware software codesign. The proposed architecture overcomes these issues by employing

fully distributed memory architecture, extendable datapath and separate memory for data and instruction.

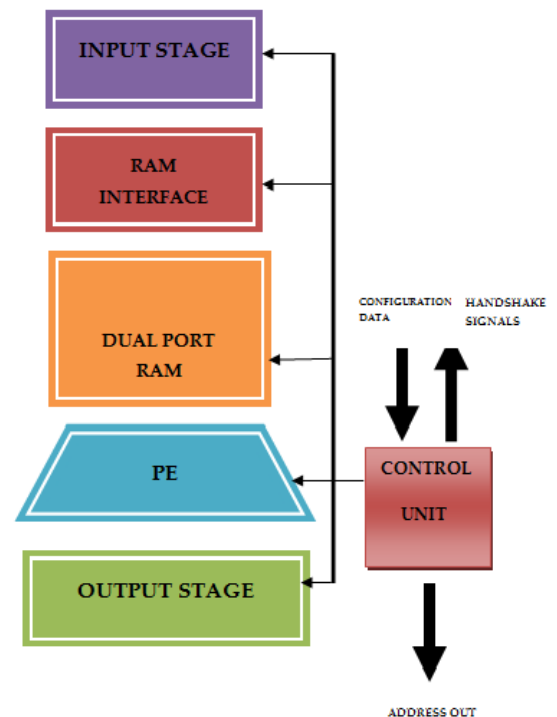


Fig – 6: Block diagram of the Proposed Architecture

The Proposed BiIRC architecture contains an array of 2-D reconfigurable cells (RC) which are organised in quadrants of four 4 x 4. Here local data and the instruction memory is issued for every Element. This enables the employment of compact, quicker memory structures.

4.1 Block Diagram of the Processing Element

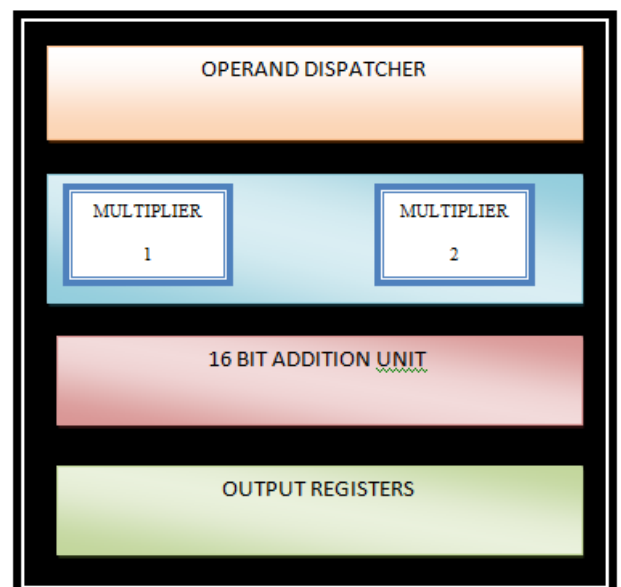


Fig – 7: Block diagram of the Processing Element

The Processing Element performs all the logic, arithmetic and accumulation processes. All 8-bit signed, unsigned operations such as addition, subtraction, multiplication in addition to the accumulation operation are did by the PE. Here, Karatsuba multiplier is employed which imparts low power and smaller area. This multiplier divides the operands into smaller sub units and calculates the solution in a short period.

4.2 Features of the Proposed Architecture

- Instead of processing inputs in four directions, the proposed architecture gets input as a whole .
- Here, a distinguishing action named pass-through operation is employed .It enables passing the operands through the PE instead of direct processing .This functionality permits the RC to handle any type of data transfers like single or blocked transfers. So, mapping is easier.
- The modified PE architecture of the BilRC uses a Dual Ported RAM instead of centralized RAM system. Here each Reconfigurable Computing Element is supplied with 256×8 memory of data. This feature allows each unit to process independently so that it avoids power consumption and large area overhead.
- Dual Port Memory type provides facility to employ two input 8 bit operands and one output.
- The proposed architecture enables port to port transfer of data in the memory allocated for data.
- An additional feature included here is the swapping of data in between memory ports by means of the Shifter/rotator in the PE. This feature employs almost 14% increase in speed when compared to the previous works.
- The use of D3L design, provides to design the architecture with minimal clocking and the design is fully dynamic with the requirement of clock signals only for driving counters and registers

5. SIMULATION RESULTS

The BilRC architecture design is developed using FPGA Xilinx Integrated Software Environment (ISE) design tool . The VHDL Language has been used for budding the code of the designed processor. The design has been tested for behavior and timing functionality. Software Tools used are Xilinx FPGA Navigator 13.2 and ISE Simulator (ISim). The synthesis summary of the Processing Element shows the least essential figure of logic blocks, flipflops as well as registers. The PE element uses only 1% of the available slice registers. This is greatly reduced when compared with previous BilRC architecture. The modified BilRC architecture achieves 92% increase in the Performance of the PE in terms of power. Also there is a considerable reduction in the area utilized.

5.1 Screenshot of the Inputs

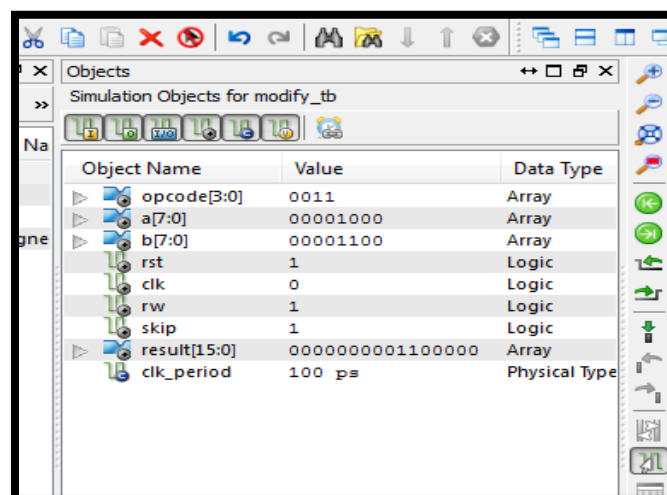


Fig – 8: Screenshot of the Inputs fed to the processor

5.2 Simulation Output



Fig – 9: Screenshot of the output from the processor

5.3 Area Report of the Proposed BilRC

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Project File:	multimedia.xise	Parser Errors:	No Errors
Module Name:	Mem_Bit_modify	Implementation Status:	Placed and Routed
Target Device:	xc3u256-5pg210	Errors:	No Errors
Product Version:	ISE 13.2	Warnings:	13 Warnings (13 new)
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (default)	Timing Constraints:	All Constraints Met
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	32	4,896	1%	
Number used as Flip Flops	16			
Number used as Latches	16			
Number of 4-input LUTs	213	4,896	4%	
Number of occupied Slices	122	2,448	4%	
Number of Slices containing only related logic	122	122	100%	
Number of Slices containing unrelated logic	0	122	0%	
Total Number of 4-input LUTs	217	4,896	4%	
Number used as logic	181			
Number used as a multiplexer	4			
Number used for Dual Port RAMs	32			
Number of bonded I/Os	40	158	25%	

Fig – 10: Area Report

5.4 Power Report of Proposed BiIRC

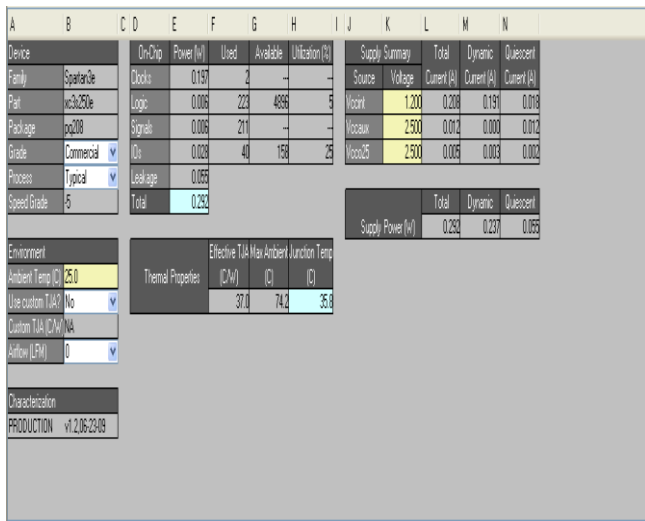


Fig - 11: Power report

The power requirement of the BiIRC is reduced to 0.292W. So minimal power is enough for this modified BiIRC architecture.

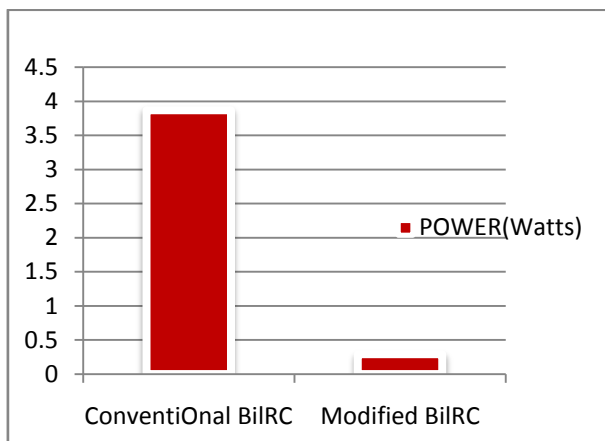


Fig – 12 : Power Comparison

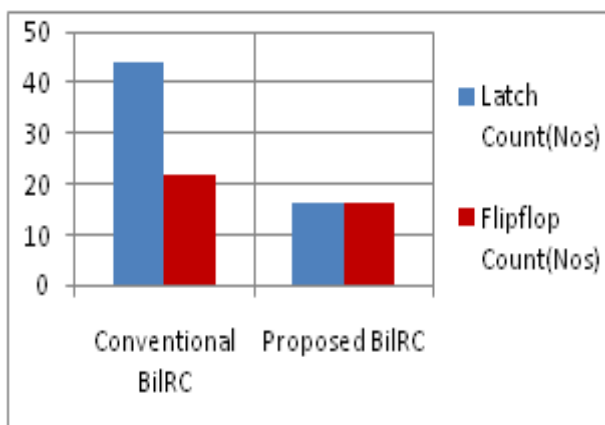


Fig – 13 : Area Comparison

The following table shows the comparison of area and power for the conventional BiIRC and its modified form.

Table – 1 : Summary of Area and Power

S. N O	TYPE	NO. OF FFs	NO.OF LATCHES	NO. OF SLICES	POWER (Watts)
1	Existing BiIRC	22	44	124	3.866
2	Proposed BiIRC	16	16	122	0.292

6. CONCLUSIONS

This paper presented the proposition of a modified BiIRC architecture which enhances the performance with reduced area and power. The proposed BiIRC architecture is a coarse grained reconfigurable architecture in which the configuration size is decreased about 33 times. Since BiIRC is an execution triggered model, delay is negligible. BiIRC will be extremely useful in the field of architectural development and the practical applications include finding highest worth of an Array, 2-Dimensional Inverse Discrete Cosine Transform Algorithm, UMTS Turbo Decoder, as an accelerator combined to a DSP processor for applications which needs high computation power, and as a replacement of FPGA in Coarse Grained Applications. Using BiIRC, the area is effectively utilized and it leads to reduction in power dissipation. From the Simulation results , Power has been reduced to 0.292 Watts which decreases the power by 92%. VHDL Coding is written for the entire architecture and it is simulated using Xilinx ISIM and verified. Simulation results demonstrate the significant reduction in size with minimal area.

Here, Statical configuration is employed for the Processing Element. These CGRAs provide a good utilization of the PE. Since BiIRC is an execution-triggered model it is a flexible interconnect architecture, and also the performance is far better than the existing works.

We would like to extend this work further by reducing the area and power by modifying the architecture.

REFERENCES

- [1] Oguzhan Atak and Abdullah Atalar, "BiIRC: An Execution Triggered Coarse Grained Reconfigurable Architecture", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 7, pp. 92–102, Jul. 2013.
- [2] O. Muller, A. Baghdadi, and M. Jezequel, "From parallelism levels to a multi-ASIP architecture for turbo decoding," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 1, pp. 92–102, Jan. 2009.
- [3] O. Atak and A. Atalar, "An efficient computation model for coarse grained reconfigurable architectures and its applications to a reconfigurable computer," in

- Proc. 21st IEEE Int. Conf Appl.-Specific Syst. Arch. Process., Jul. 2010, pp. 289–292.
- [4] R. Hartenstein, “A decade of reconfigurable computing: A visionary Retrospective,” in Proc. Eur. Design, Autom. Test Conf., 2001, pp. 642–649.
- [5] B. De Sutter, P. Raghavan, and A. Lambrechts, “Coarse-grained reconfigurable Array architectures,” in Handbook of Signal Processing Systems, S. S. Bhattacharyya, E. F. Deprettere, R. Leupers, and J. Takala, Eds. New York: Springer-Verlag, 2010, pp. 449–484.
- [6] B. Mei, A. Lambrechts, J.-Y. Mignolet, D. Verkest, and R. Lauwereins, “Architecture exploration for a reconfigurable architecture template,” IEEE Design Test Comput., vol. 22, no. 2, pp. 90–101, Mar.–Apr. 2005
- [7] Kuon and J. Rose, “Measuring the gap between FPGAs and ASICs,” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 26, no. 2, pp. 203–215, Feb. 2007.
- [8] K. Compton and S. Hauck, “Reconfigurable computing: A survey of systems and software,” ACM Comput. Surv., vol. 34, no. 2, pp. 171–210, 2002.
- [9] M. Lanuzza, S. Perri, P. Corsonello, and M. Margala, “Energy efficient coarse-grain reconfigurable array for accelerating digital signal processing,” in Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation (Lecture Notes in Computer Science), L. Svensson and J. Monteiro, Eds. Berlin, Germany: Springer-Verlag, 2009.
- [10] Purohit, S. Chalamalasetti, M. Margala, P. Corsonello, “Power-Efficient High Throughput Reconfigurable Datapath Design for Portable Multimedia Devices,” in Proceedings of International Conference on Reconfigurable Computing and FPGAs, pp. 217-222, 2008.
- [11] S. Chalamalasetti, S. Purohit, M. Margala, and W. Vanderbauwhede, “MORA: Architecture and programming model for a resource efficient coarse grained reconfigurable processor,” in Proc. ACM NASA/ESA Conf. Adapt. Hardw. Syst., 2009, pp. 389–396
- [12] Sohan Purohit, Sai Rahul Chalamalasetti, Martin Margala, and Wim Vanderbauwhede, “Throughput/Resource-Efficient Reconfigurable Processor for Multimedia Applications,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 7, pp. 92–102, Jan. 2013.
- [13] Purohit, S. Chalamalasetti, M. Margala, P. Corsonello, “Power-Efficient High Throughput Reconfigurable Datapath Design for Portable Multimedia Devices,” in Proceedings of International Conference on Reconfigurable Computing and FPGAs, pp. 217-222, 2008.

BIOGRAPHIES



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