HIGH PERFORMANCE LOW LEAKAGE POWER FULL SUBTRACTOR CIRCUIT DESIGN USING RATE SENSING KEEPER

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Abstract

Dynamic CMOS are widely employed in high-performance CMOS chips due to high speed and less area in comparison with Static CMOS. However, Dynamic CMOS circuits are inherently less noise tolerant than Static CMOS circuits. This problem becomes more severe with aggressive technology scaling into nanometer process, particularly caused by the charge sharing, the sub-threshold leakage current, the power rail noise and the crosstalk noise. Both noise and process variations impact reliability, causing logic errors that can result in system failure. Process variation is defined as "the deviation from intended or designed values for a structure or circuit parameter of concern" parameter of concern". In this project, a full subtractor circuit is designed and simulated using rate sensing keeper technique with 120nm technology and V_{dd}=1.2V for improving the timing and noise tolerance also the noise tolerance characteristics of the full subtractor circuit designed using Rate Sensing Keeper is compared with Twin-Transistor, Current Mirror Keeper based full subtractor circuit.

Keywords: *charge sharing, rail noise, noise tolerance, rate sensing and timing optimization*

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1. INTRODUCTION

Dynamic CMOS circuits are now commonly used in the design of high performance microprocessors. The dynamic CMOS logic has gained importance due to its speed and ability to perform higher frequency circuit operations. Dynamic CMOS is also important because of its reduced area. Dynamic CMOS circuits do not have the complementary PMOS pull-up networks which results in reduced loading and hence reduced area. This makes Dynamic CMOS logic faster than static CMOS. In other words, dynamic CMOS are same as static CMOS except that it uses a clock controlled PMOS for implementing the PMOS pull-up network. For all these advantages dynamic CMOS logic is very popular among present day designers. The dynamic CMOS circuit shown has two modes of operation: Precharge phase and Evaluation phase. The delay of the dynamic circuits can be controlled by varying the sizes of transistors in the circuit. The circuit delay can be reduced by increasing the transistor sizes in the circuit. This means that high speed circuits require larger area. So for dynamic circuits, there is a trade off exist between speed and area.

Precharge phase: This happens when clock signal is LOW. Thus the NMOS pull-down network is turned OFF. The clock controlled PMOS transistor is turned ON. So the 'Output' node is charged to V_{dd}. Hence this is called Precharge phase or setup phase. Evaluation phase: This happens after the Precharge phase and when the clock signal is HIGH. The 'Output' node is either pulled down or pulled up depending on the inputs to the NMOS transistors. This defines the operation of the dynamic CMOS circuit.

Timing optimization of dynamic CMOS is the major area of concern for the present day designers. Timing optimization in dynamic CMOS has great challenges because of the transistor sizing and the poor noise tolerance of the dynamic CMOS circuits. Over the last decade there were many algorithms proposed for transistor sizing of the dynamic CMOS circuits to give better timing optimization. Timed Logic Synthesizer (TILOS) was an algorithm which performed sizing of the transistors iteratively based on a fixed ratio [3]. The sizing of the transistors was done only on the critical paths. Therefore the other timing paths present in the design were not considered. INFLOTRANSIT is another algorithm which iteratively performs transistor sizing but requires directed acyclic graphs to be generated. This makes the algorithm difficult to understand and implement. Computation of logic effort is another method to perform timing optimization. Because of the complexity of these algorithms, the Load Balancing of Multiple algorithm LBMP was proposed. This algorithm is simple and easy to understand and implement. The effect of process variations is also included in the LBMP which makes the algorithm more attractive. Also considering the process variations reduce the delay uncertainty. Delay uncertainty is defined as the difference in maximum time delay and minimum time delay. The process variations results give the mean and standard deviation of a particular

parameter. These mean and standard deviation values correspond to the intra-die and inter-die variations respectively.

In spite of the advantages, there is a major disadvantage with the dynamic CMOS logic is poor noise tolerance. The noise tolerance is less when compared to the static counterpart, which in turn degrades the performance of dynamic CMOS circuits and the entire system as well. In other words, Dynamic CMOS circuits are less noise tolerant but faster than Static CMOS. So designer will need to focus on improving the noise tolerance for Dynamic CMOS circuits when making the digital system faster. Noise is an unwanted perturbation to a signal that affects the functionality of the given design producing erroneous results. For example, because of the leakage currents, the pull-down NMOS transistor network may be turned 'ON' but it should have been 'OFF' for that particular set of inputs. Improving the noise tolerance without having much impact on the performance of the dynamic CMOS circuits is a great challenge.

The paper is organized as follows. Section II details the circuit implementation and operation of the full subtractor using RSK technique. Section III evaluates the performance of the full subtractor circuit designed using RSK technique and compares its performance with full subtractor circuits designed using twin transistor and diode footed domino techniques using the simulated results. Section IV concludes the paper.

2. CIRCUIT DESIGN

A simple domino logic circuit consists of a pull down network, a P-type pull up transistor, an N-type footer transistor a keeper transistor and an inverter. The clock signal is connected to the gates of p-type pull up and n-type footer transistors. The keeper transistor is used to reduce the effect of charge leakage at the dynamic node .When clock goes low, the dynamic node is precharged to V_{DD} and the output goes low in this condition. When the clock signal goes high the circuit evaluate the logic function. The circuit diagram of the Full adder sum circuit implemented using simple domino logic is shown in Fig-1.

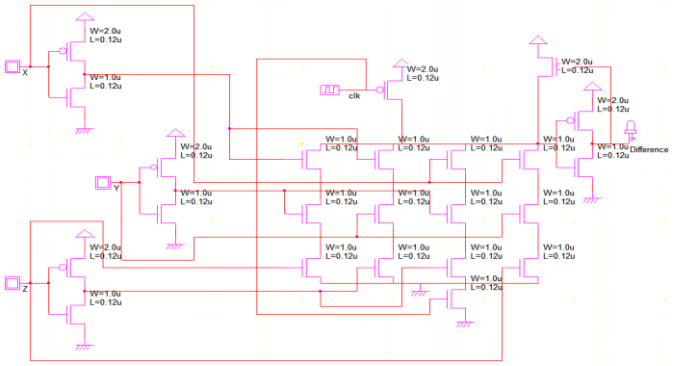

Fig -1: Full subtractor Difference circuit using domino

The layout of the sum circuit of the full subtractor designed using simple domino technique is shown in Fig-2. The circuit is implemented using L=0.12µm technology with V_{DD} =1.2V.The I_D-V_{DD} characteristics of the NMOS transistor measured from the layout of the full subtractor difference circuit designed using simple domino logic technique is shown in Fig.3. Domino logic circuits have been excellent choice in the design of high-performance modules in modern microprocessors. The only demerit of domino logic circuits is their relatively low noise margin compared to that of standard CMOS circuits

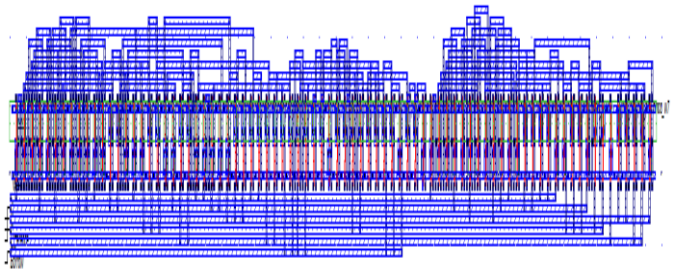

Fig -2: Layout of the Full subtractor Difference circuit using domino

Traditionally, this issue has been resolved by employing a P-type keeper transistor that compensates for leakage current of the pull-down network. However, aggressive scaling trends of CMOS technology along with increasing levels of process variations have reduced effectiveness of the traditional p-type keeper transistor approach.

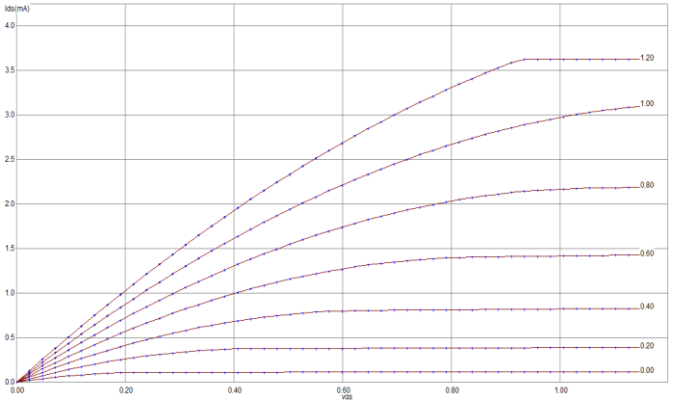

Fig -3: I_D-V_{DD} characteristics of the NMOS transistor measured from the layout

The full subtractor difference circuit implemented using current mirror technique is shown in Fig-4

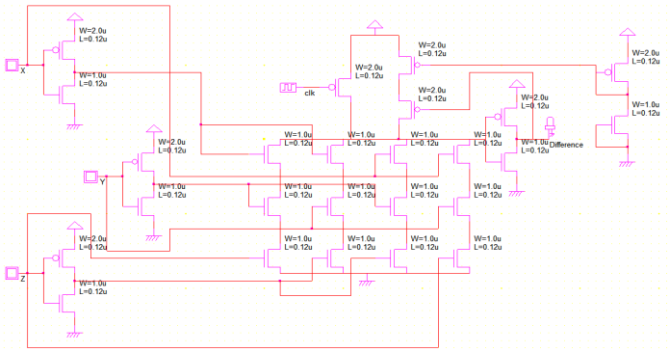

Fig-4: Full subtractor Difference circuit using current mirror technique

The layout of full subtractor difference circuit implemented using current mirror technique is shown in Fig-5

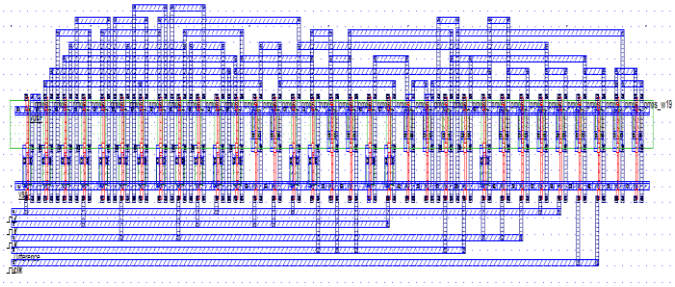

Fig-5: Layout of Full subtractor Difference circuit using current mirror technique

In this full subtractor circuit a current mirror is connected to the keeper transistor which compensates for leakage current of the pull-down network. This current mirror can be shared for all the logic gates in the circuit. In this configuration the keeper and current mirror circuit reduces the delay of the circuit by reducing the effect of charge sharing. The full subtractor borrow circuit implemented using current mirror technique is shown in Fig-6

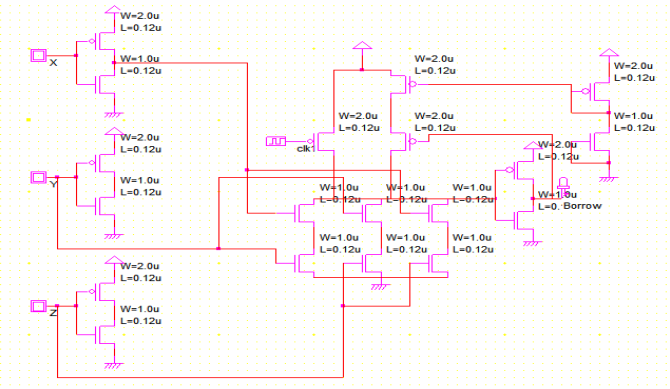

Fig-6: Full Subtractor Borrow circuit using current mirror technique

The corresponding full subtractor borrow circuit using current mirror technique layout is shown in Fig-7.

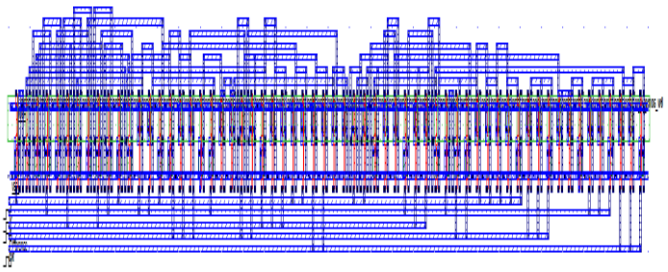

Fig-7: Layout of Full Subtractor Borrow circuit using current mirror technique

Since the keeper is strongly ON during the beginning of the evaluation phase, the contention is still high in this circuit technique. Also the replica transistor does not track the leakage current due to noise and DIBL in the pull down NMOS network. The area overhead of the replica and mirror pMOS transistors becomes very high which inturn leads to excess static power dissipation in the replica circuit.

A single current mirror structure can be shared among more than one domino logic circuits, this design technique is useful for constructing wide fan in circuits. The clock frequency used in this design is 500MHz. As the clock frequency increases the output voltage decreases due to the parasitic capacitances. When clock is low, the dynamic node will be precharged to V_{DD} (precharge phase) and the output remains low in this condition. When the clock signal changes the state from low to high the circuit evaluate the logic function (evaluation phase).

Twin transistor technique can be used for designing noise-tolerant dynamic logic circuits**.** In a 0.12-µm CMOS technology and at a supply voltage of V_{DD}=1.2V, the full subtractor circuit designed using twin transistor technique provides a significant improvement in the noise immunity of dynamic circuits. The full subtractor difference circuit designed using twin-transistor technique is shown in Fig-8 and this circuit achieves additional noise immunity at the expense of energy.

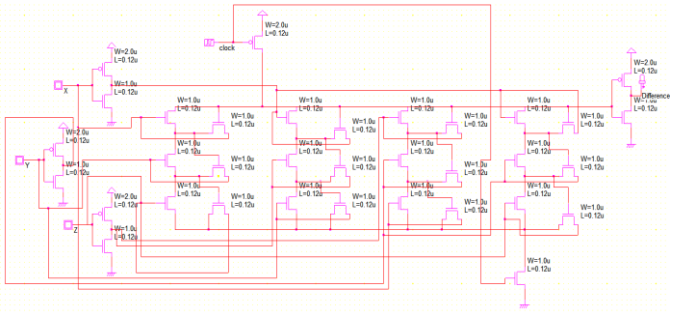

Fig-8: Full subtractor difference circuit using twin transistor technique

The layout of the full subtractor difference circuit designed using twin transistor technique is shown in Fig-9

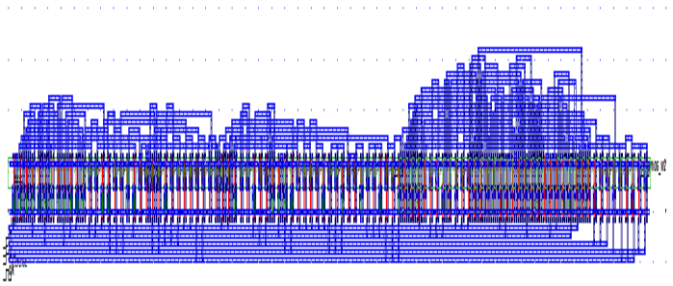

Fig-9: Full subtractor difference circuit using twin transistor technique

The full subtractor borrow circuit designed using twin-transistor technique is shown in Fig-10 and the layout of the full subtractor borrow circuit is shown in Fig-11.

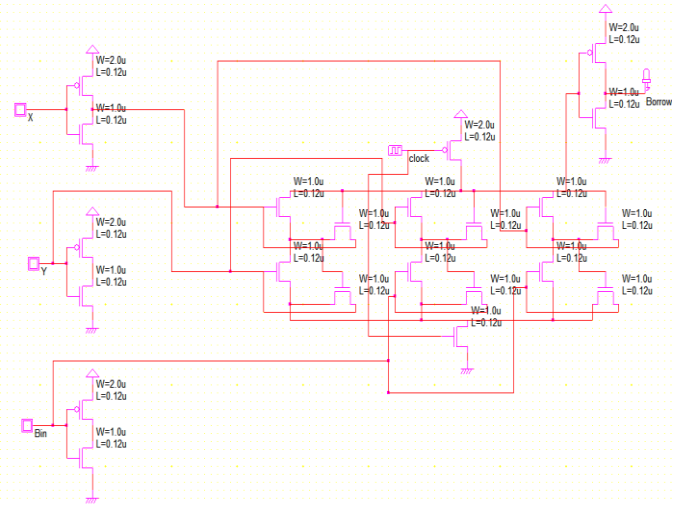

Fig-10: Full subtractor borrow circuit using twin transistor technique

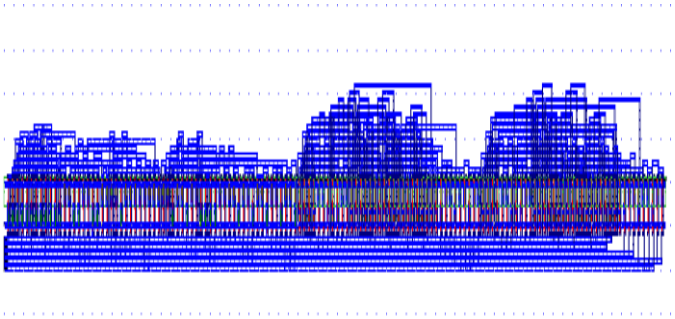

Fig-11: Layout of Full subtractor borrow circuit using twin transistor technique

The twin transistor technique improve the noise immunity of the circuit by increasing the threshold voltage of the NMOS transistor which is connected to the input through a cross coupled transistor called twin transistor. It has been shown that the full subtractor circuit designed using twin transistor technique is more energy-efficient than existing noise-tolerant full subtractor circuits designed using other dynamic techniques. Since the twin transistors increase the node capacitance of the full adder circuit, the circuit delay will be increased. Twin-transistors also reduce the charge-sharing problem that occurs in dynamic logic circuits. The main advantage of the full subtractor circuit designed using the twin transistor technique is that it achieves higher noise immunity than a conventional full subtractor circuit, and also this full subtractor circuit can be operated at a smaller supply voltage to achieve the noise immunity of the conventional full subtractor circuit at a higher voltage.

The full subtractor circuit designed using rate sensing technique works based on the difference in the rate of change of voltage at the dynamic node of the circuit during the ON and the leakage condition and the average of these two rates called reference rate is used to control the keeper transistor. This technique helps to achieve high speed and low noise.

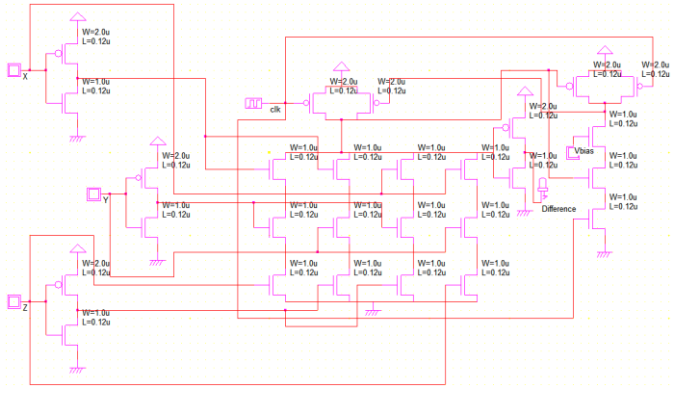

Fig-12: Full subtractor difference circuit using rate sensing keeper technique

The full subtractor circuit implemented using rate sensing keeper technique is shown in Fig-12 and its layout is shown in Fig-13.

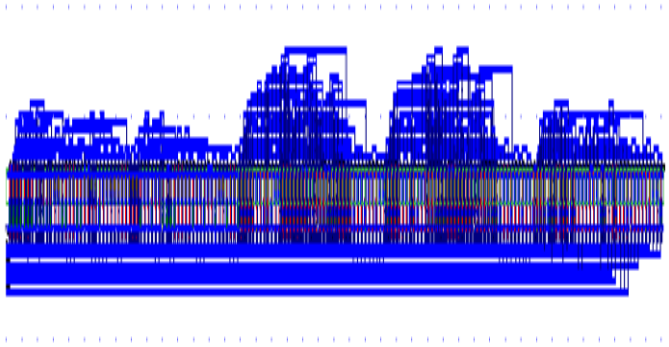

Fig-13: Layout of Full subtractor Difference circuit using rate sensing keeper technique

The full subtractor borrow circuit implemented using rate sensing keeper technique is shown in Fig-14

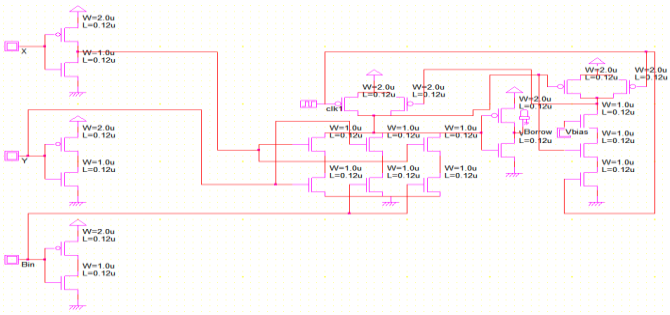

Fig-14: Full subtractor CARRY circuit using rate sensing keeper technique

The layout of full subtractor borrow circuit implemented using rate sensing keeper technique is shown in Fig-15

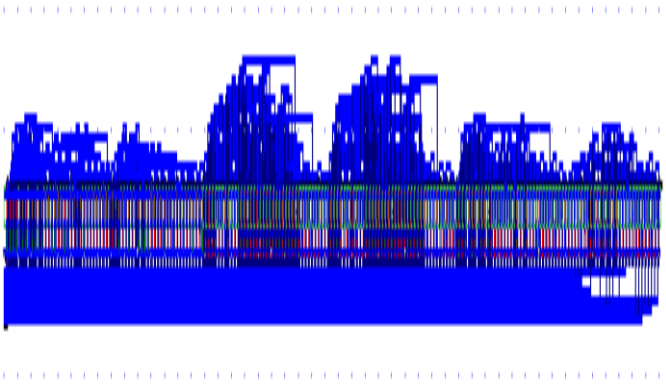

Fig-15: Layout of Full subtractor Borrow circuit using rate sensing keeper technique

3. SIMULATION RESULTS

The simulations are performed using L=0.12µm technology along with the supply voltage V_{DD}=1.2V. The timing diagram of the full subtractor difference circuit implemented using rate sensing technique is shown in Fig-16

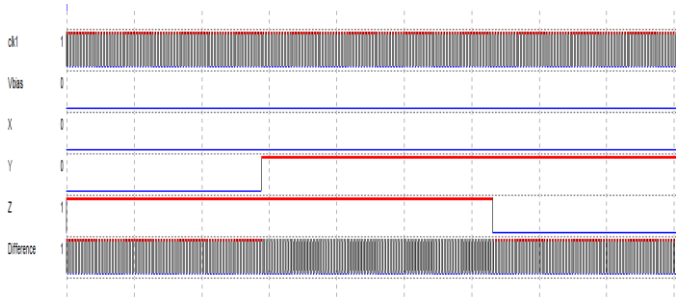

Fig-16: Timing diagram of the Difference circuit of the full subtractor

The timing diagram of the borrow circuit is shown in Fig-17.

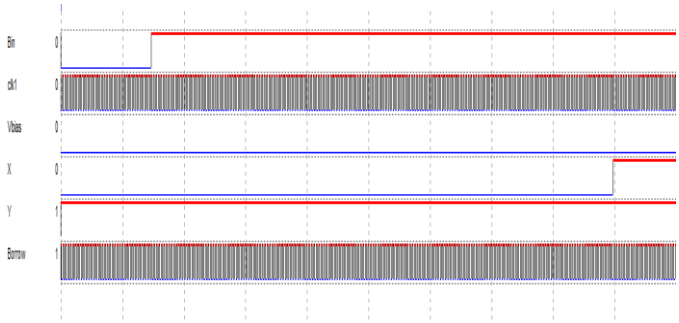

Fig-17: Timing diagram of the borrow circuit of the full subtractor

The I_D-V_{DS} characteristics of PMOS used to implement the full subtractor circuit with L=0.12µm W=1 µm at V_{DD}=1.2V is shown in Fig18. The drain current is 600µA at V_{DD}=1.2V. The I_D-V_{GS} characteristics of NMOS devices used in this full subtractor circuit with L=0.12µm at V_{DD}=1.2V is shown in Fig-19. The I_D-V_{GS} characteristics of PMOS used in this full subtractor circuit with L=0.12µm at V_{DD}=1.2V is shown in Fig-20

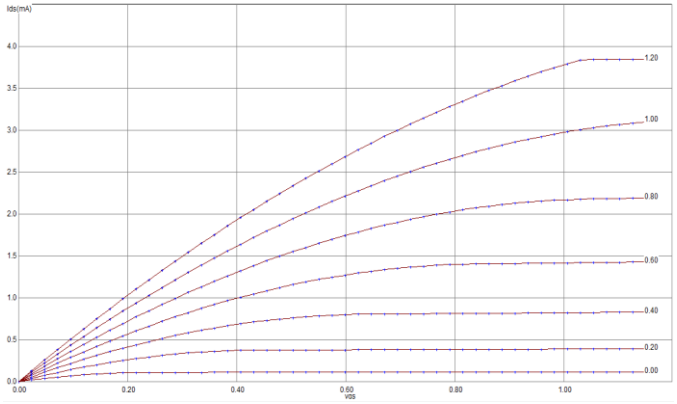

Fig-18: I_D-V_{DS} characteristics of PMOS with L=0.12µm W=1 µm at V_{DD}=1.2V

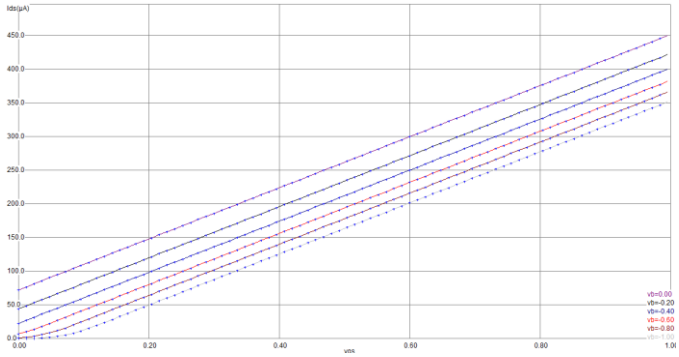

Fig-19: I_D-V_{GS} characteristics of NMOS with L=0.12µm at V_{DD}=1.2V

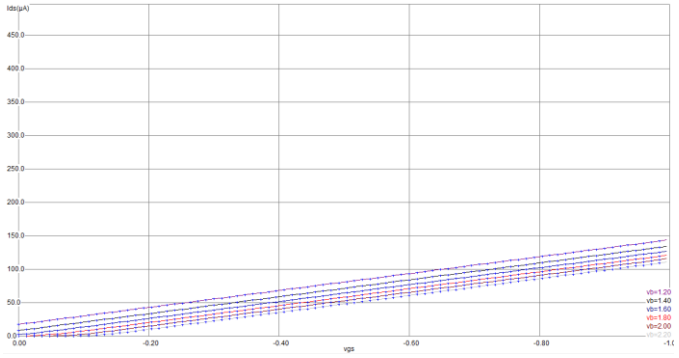

Fig-20: I_D-V_{GS} characteristics of PMOS with L=0.12µm at V_{DD}=1.2V

The output noise characteristic of the full subtractor circuit implemented using rate sensing keeper is shown in The output noise can be reduced by properly selecting the bias voltage value. The output noise decreases with increase in bias voltage. But the increase in bias voltage also increases the circuit delay. So the selection of bias voltage plays a major role in the circuit operation. The full subtractor circuit implemented based on an adaptive keeper technique called rate sensing keeper (RSK) that enables faster switching and the experimental results shows that the full subtractor circuit designed using rate sensing keeper transistor technique gives superior performance compared to the other alternatives such as Conditional Keeper (CKP) and current mirror-based keeper (LCR).

4. CONCLUSIONS

In this paper the performance of a full subtractor circuit designed using rate sensing keeper transistor technique is analyzed in detail and its performance is compared with other full subtractor circuits. The full subtractor circuit is simulated using L=0.12µm technology along with supply voltage V_{DD}=1.2V. The experimental results shows that the full subtractor circuit designed using rate sensing keeper transistor technique gives superior performance compared to full subtractor circuits designed using conventional domino techniques.

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BIOGRAPHIES

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