DESIGN AND ANALYSIS OF A TWO STAGE MILLER COMPENSATED OP-AMP SUITABLE FOR ADC APPLICATIONS

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Abstract

In this paper a two stage RC Miller compensated op-amp and its analysis is presented. In order to obtain a high dc gain, a two stage op-amp is used. The two stage op-amp consists of a telescopic op-amp in the first stage and a common source output rail-to-rail stage in the second stage .In addition to the dc gain ,the main advantage of this op-amp is the voltage swing .The simulated results shows a DC gain of 60dB ,phase margin of 50^0,CMRR of 48.7dB and a slew rate of 100V/µs respectively .The total power dissipation obtained from the op-amp circuit is 1.3mW. For comparison, a similar op-amp which uses a double cascode telescopic input has been realized .And both these op-amps are designed using 0.18µm CMOS process.

Keywords: *Cascoded telescopic op-amp, CMOS technology, CMRR, Miller compensated op-amp, pipelined analog-to-digital converter, Slew Rate, telescopic op-amp.*

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1. INTRODUCTION

The most modern telecommunication system needs high speed and medium resolution Analog-to-Digital Converters which will lead to new design challenges for the op-amp circuits. Now the recent challenges related with designing of an op-amp is the reduced supply voltage with reduced channel length. Pipelined ADCs are most popular high speed, medium resolution and high accuracy ADC. In this paper, the two stage op-amp is considered as a part of the Multiplying Digital-to-Analog converter (MDAC) in the stages of the pipelined ADC.

The two stage op-amp consists of a telescopic op-amp stage and a common source output rail-to-rail stage. Designing of high speed op-amp is the challenging part of the pipelined ADC .As per Liang and Gulati, the main bottleneck is that there is a tradeoff between speed and gain ,because high dc gain demands a multistage design with long-channel devices and a low bias current levels, whereas the high speed demands single stage design , short channel devices and a high bias current levels [1-2].The telescopic op-amp is mainly used because of its simplicity over other circuit designs and it allows high speed operation and low power consumption. The op-amp circuit uses RC Miller compensation in order to obtain maximum bandwidth and stability.

To achieve high gain and high bandwidth the well known differential topology is used .The main advantage of the differential topology is the higher immunity towards the environmental noise.

In this paper, two stage RC miller compensated op-amp is designed and compared with another similar op-amp which uses double cascode telescopic input in the first stage and common source amplifier in the second stage. As per Nagaraj , the op-amp with double cascode telescopic input provides low output resistance and minimum output signal loss[3]. Also the load capacitors improves the phase margin of the Miller compensated op-amp.

The paper is organized as follows: Section II presents the op-amp structure, Section III describes the optimal design procedure to achieve minimum power consumption, Section IV describes the simulation results, Section V describes the AC analysis and Conclusion is given in Section VI.

2. OP-AMP STRUCTURE

Operational amplifiers are the superior part of many analog circuits. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for performing mathematical operations. It is reported that in order to achieve high gain and high bandwidth a two stage miller compensated op-amp is used[4].As per Sinha ,in some applications the gain and/or the output swings provided by cascade op-amps are not adequate[5].In such cases, a two stage op-amp is used ,where the first stage providing a high gain and the second stage which gives larger swing. In contrast with cascade op-amps, a two stage configuration in op-amps will isolate the gain and swing requirements.

In a two stage op-amp circuit design, in order to get stability in the system, proper compensation techniques should be added with the op-amp circuits. There are several compensation techniques available like pole splitting miller compensation, self compensating capacitor, feed forward compensation using an additional amplifier, negative miller compensation. In comparison with various compensation techniques RC miller compensated technique provides high gain and voltage swing and has been used in this two stage op-amp circuit.

In the two stage op-amp circuits problem arises due to the dominant poles .Because of the two dominant poles in the two stage op-amp, instability can occur due to the inadequate phase margin value. This serious problem should be taken carefully by the designers, otherwise the op-amp will act as an oscillator instead of an amplifier. There will be zero in the right-half plane. So in order to cancel the non-dominant poles and to move the right half zero an extra resistor R_Z is also added to the circuit. Also a Miller capacitor with a nulling resistor is used which is similar to miller capacitor but a series resistance is added which control the gain over the RHP zero[4]. It is reported that the actual implementation of the R_Z will occupy more area for larger resistance value .It is reported that the resistor R_Z is implemented using a MOS transistor in the triode region [6].

The two stage op-amp circuit consists of an double cascode telescopic input in the first stage to obtain high gain and common source amplifier in the second stage. As per Tero Nieminen, the advantage of common source amplifier over the differential is high output swing .It is reported that in addition of increased DC gain, the most obvious is the larger output swing [7]. Nowadays the principal challenge in the op-amp design is to obtain the maximum output swing. The bandwidth of the op-amp is limited by using Miller compensation technique. It is reported that to obtain sufficient gain and signal headroom, the design utilizes a two-stage Miller compensated amplifier, with input telescopic and output common-source rail-to-rail stage [8]. The architecture of the two stage op-amp is shown in the figure 1.

In this architecture M0,M1,M2,M3,M4,M5,M6,M7 and M8 constitutes the telescopic part and the remaining transistors M9,M10,M11 and M12 constitutes the common source amplifier .The op-amp using double cascode telescopic as first stage which constitutes the M0,M1,M2,M3,M4,M5,M6, M7,M8,M9,M10,M11,M12 as the telescopic part and remaining transistors function for the common source amplifier.The architecture for the double cascode-telescopic as input stage is shown in figure 2.

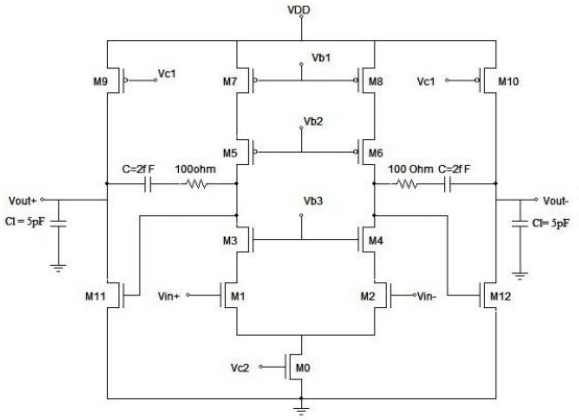

Fig-1: Architecture of the two stage RC miller compensated op-amp

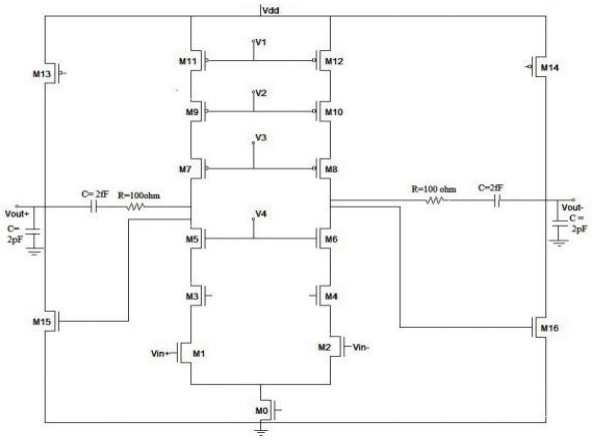

Fig-2: Architecture of the two stage RC miller compensated op-amp using double cascode telescopic op-amp

3. DESIGN PROCEDURE

To design an op-amp, a 1.8V supply voltage and a power budget of 1mW is assumed initially. For 1mW power budget, an I_{TOTAL} of 0.555mA is obtained .This total current is then divided into the four branches of the circuit .The W/L ratios of the transistors are chosen based on the saturation region operation.The first assumption values taken are μ_n*C_{ox}= 150 $\mu A/V^2$ and μ_p*C_{ox} = 60 $\mu A/ V^2$. It is reported that the aspect ratios (W/L) of transistors are calculated using the saturation region current equation [9] given below.

$$I_D = \frac{1}{2}\mu_{n,p}*C_{ox}(W/L_{n,p})(|V_{gs}| - V_T)^2 \qquad (1)$$

In the above equation I_D is the drain current which is taken as the biasing current, μ_n and C_{ox} are the process parameters, W/L is the aspect ratio of a transistor, V_{gs} is gate-source voltage and V_T is the threshold voltage.

Then the respective overdrive voltages for the PMOS and NMOS transistors are assigned .Generally, the overdrive voltage for PMOS transistor is always taken as larger than NMOS transistors, since the PMOS transistors have lower mobility than the NMOS transistors .In this paper, PMOS and NMOS overdrive voltages are taken as 350mV and 250mV respectively. Approximate values for the biasing voltages are obtained. Both the op-amp circuits were designed using the above equations. The op-amp circuit is designed and simulated in 0.18µm CMOS process. The transistor aspect ratios for the op-amps are given in the Table 1 and Table2.

Table- 1: Aspect Ratios of the Transistors (W/L)µm for the Two Stage Compensated Op-Amp

Transistors	Aspect Ratios (W/L)µm
M0`	3/1.8
M1,M2	20/1.8
M3,M4	9/1.8
M5,M6	24/1.8
M7,M8	12.2/1.8
M9,M10	1.2/1.8
M11,M12	4/1.8

Table- 2: Aspect Ratios of the Transistors(W/L)µm for the second architecture with Double Telescopic Op-Amp input stage.

Transistors	Aspect Ratios (W/L)µm
M0	8/1.8
M1,M2	20/1.8
M3,M4	18.5/1.8
M5,M6	16.9/1.8
M7,M8	28.3/1.8
M9,M10	26/1.8
M11,M12	24/1.8
M15,M16	4/1.8

4. SIMULATION RESULTS

4.1 Two Stage RC Miller Compensated op-amp with Simple Telescopic Input.

The two stage op-amp is simulated using the 180nm CMOS technology. The transient analysis for the op-amp circuit is taken for 1.6V p-p differential voltage and a frequency of 80MHz as per the requirement of the ADC application. The schematic for the two-stage op-amp is shown in figure 3.

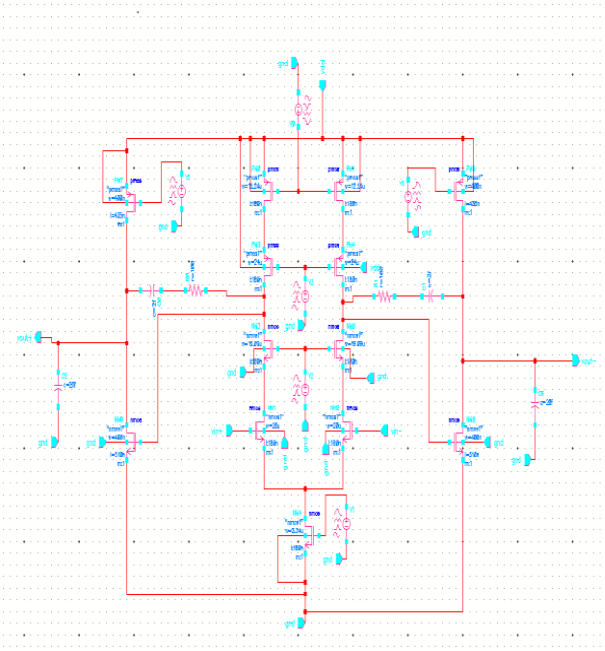

Fig-3: Schematic of two stage op-amp

The transient analysis of the two stage op-amp circuit is shown in figure 4. The load capacitors are given with a value 20fF.

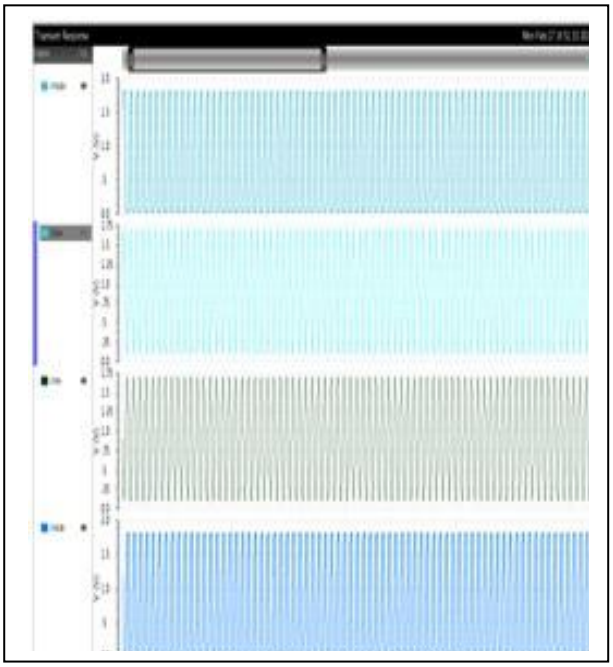

Fig-4: Transient analysis of the two stage op-amp

Two stage RC miller compensated op-amp using double cascode telescope as input stage is designed

The schematic of the two stage RC miller compensated op-amp is shown in figure 5.

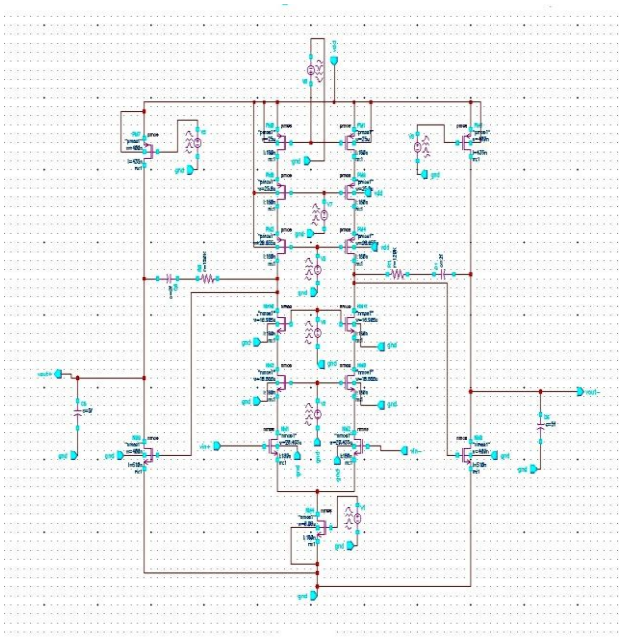

Fig- 5: Schematic of the two stage RC miller compensated op-amp using double cascode telescopic input as first stage

Compared to the previous structure the number of transistors used here is increased .The waveform obtained for the above architecture is given below in figure 6.

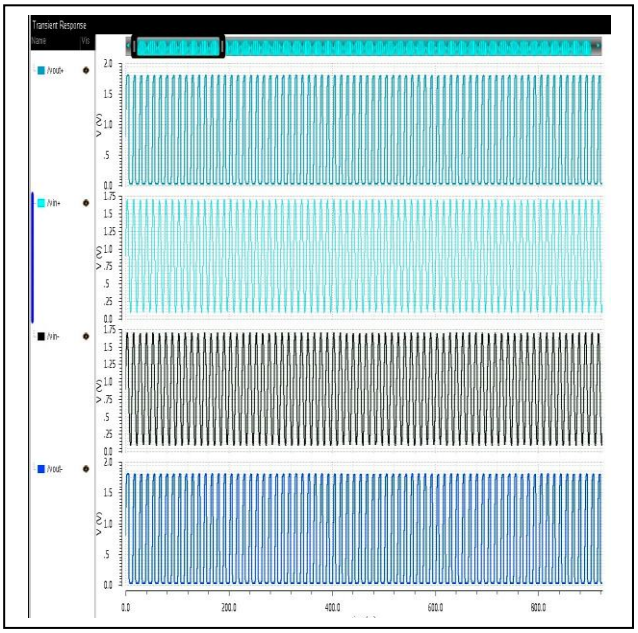

Fig-6: Waveform for the two stage RC miller compensated op-amp using double cascode telescopic input as first stage

5. AC ANALYSIS

5.1 Gain and Phase Plots

The simulation of the simple two stage op-amp gives a dc gain of 60dB, slew rate of 100V/µs, CMRR of 48.7dB, total power of 1.3mW and an average power of 0.7mW is obtained. The simulated gain and phase plot of two stage op-amp is shown in figure 7.

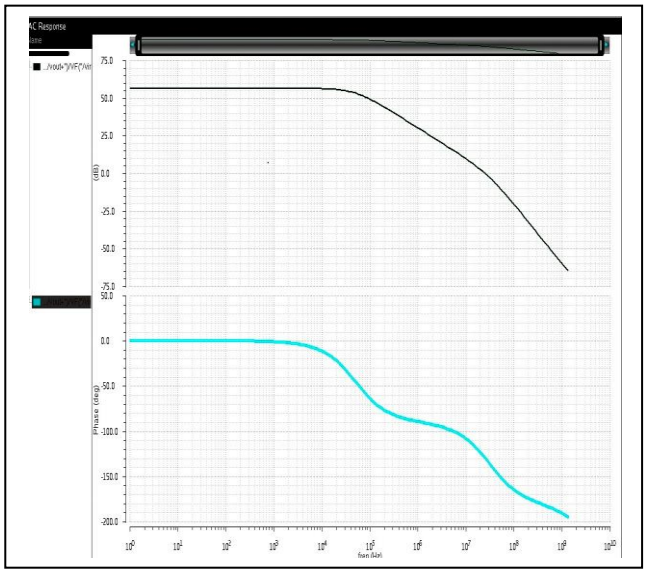

Fig-7: Gain and phase plot of the two stages Op-amp

The simulation result shows that the two stage op-amp using the double cascode telescope as input stage which gives a dc gain of 52.56dB, slew rate of 2V/µs, CMRR of 26.05dB, total power of 2.07mW is obtained. The simulated gain plot and phase plot is shown in figure 8

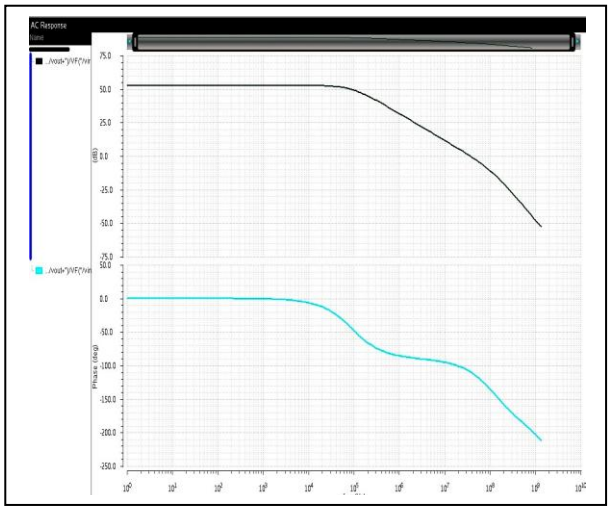

Fig -8: Gain and phase plot of the two stage op-amp using the double cascode telescope

5.2 Power Plots

The power waveform for the simple two stage op-amp is shown in figure 9.The total power consumption for this op-amp is 1.3mW and the average power is 0.7mW.

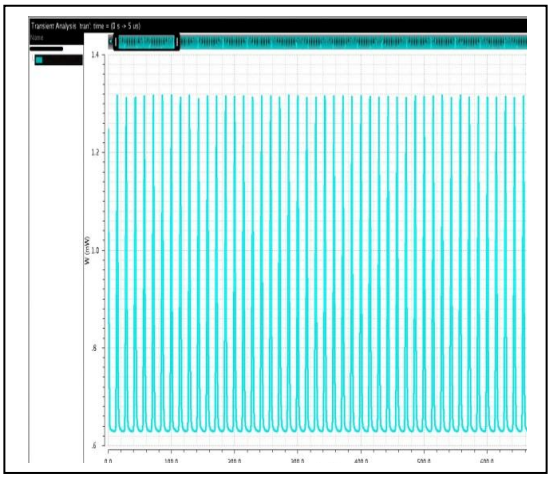

Fig-9: Simulated power waveform for simple two stage op-amp

The simulation results shows that the total power obtained for the two stage op-amp using double cascode telescopic op-amp is 2.07mW.And the average power obtained is 1.23mW.The power plot is shown in figure 10.

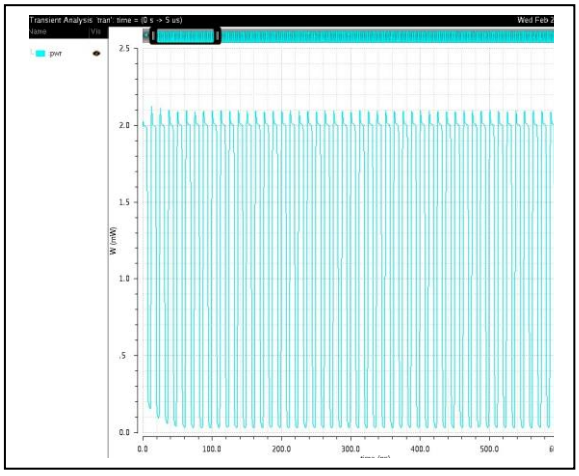

Fig-10: Simulated power waveform for the two stage op-amp using the double cascode telescopic op-amp.

The test bench circuit for the two stage op-amps is shown in figure11.The test bench circuit which is then used for determining the CMRR ,Slew rate of the given op-amp circuit.

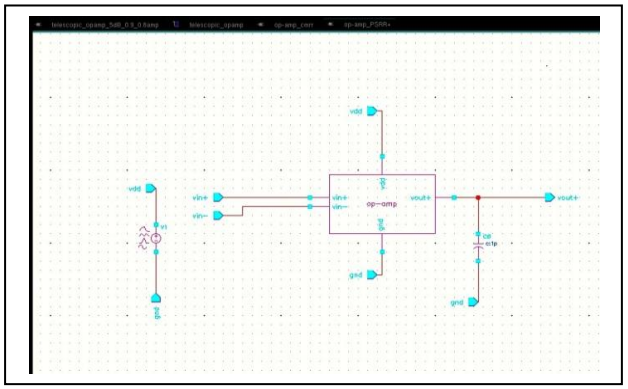

Fig-11: Test bench circuit for the two stage RC miller compensated op-amp

5.3 CMRR

The CMRR value obtained for this op-amp by connecting the inputs Vin+ and Vin- each other and a capacitor is connected across the output .The op-amp common mode rejection ratio is defined as the ratio of common-mode gain to differential-mode gain Vcm/Vdm .It is expressed in dB. The plot which showing the CMRR in dB is shown below in figure 12.

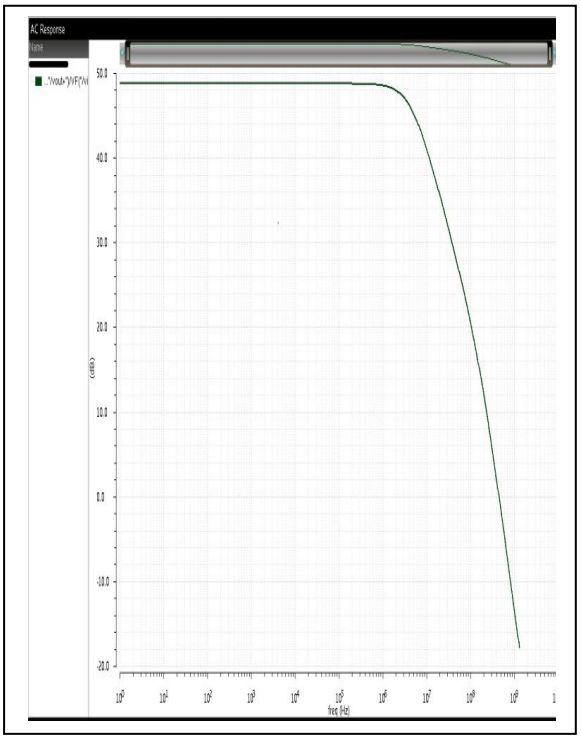

Fig-12: CMRR plot showing a CMRR value of 48.7dB

The CMRR plot for the for the two stage op-amp using the double cascode telescopic op-amp is shown in figure 13.

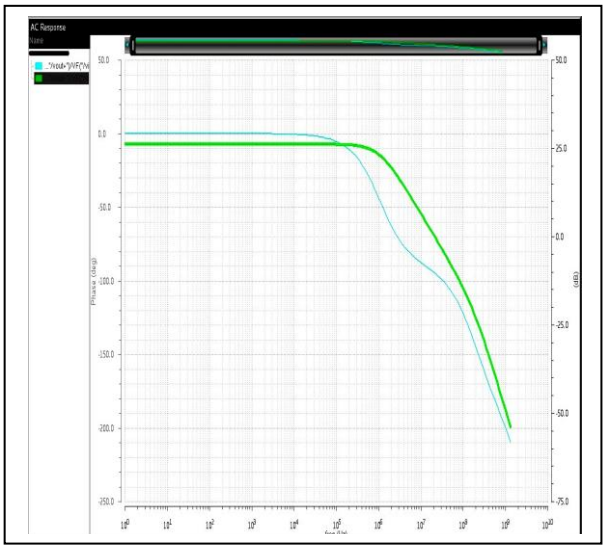

Fig-13: CMRR plot waveform for the two stage op-amp using the double cascode telescopic op-amp

The CMRR value obtained for the for the two stage op-amp using the double cascade telescopic op-amp is 26.05dB.

5.4 Slew Rate

The slew rate of an op-amp is defined as the maximum rate of change of an output voltage for all possible input signals,it is reported in [10].Slew rate is expressed in V/µs .The slew rate is calculated by giving the Vin+ a square wave and Vin- is feedback to the output .The simulated output which showing slew rate of 100V/µs is shown in figure 14.

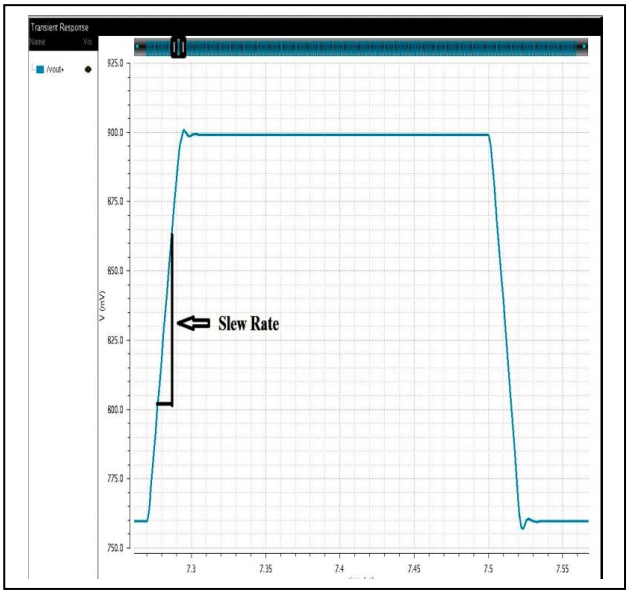

Fig-14: Transient response showing the slew rate of 100V/µs

The slew rate obtained for the two stage op-amp using the double cascode telescopic op-amp is 2V/µs. And slew rate plot is shown in figure 15

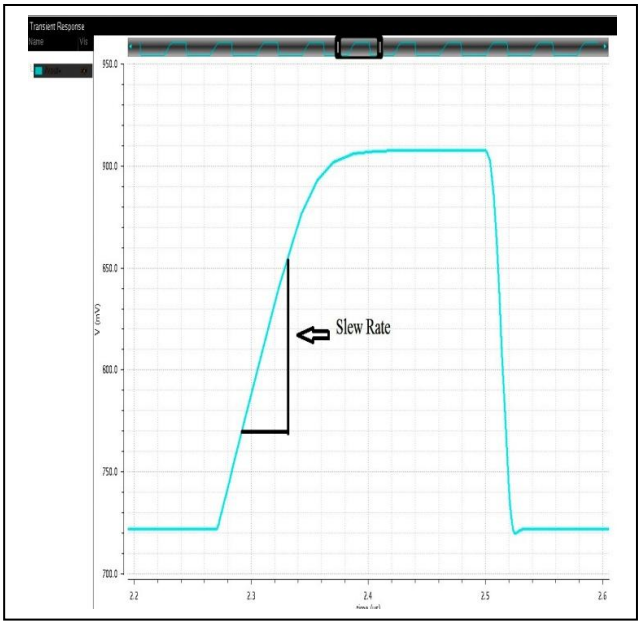

Fig-15: Transient response showing the slew rate of 2V/µs.

Table 3 shows the performance summary of the op-amps.

Table -3: Performance Summary of the Op-Amps

Specifications	Simple two stage telescopic op-amp	Two stage op-amp using double cascode telescopic op-amp
Power supply	1.8V	1.8V
Technology	180nm	180nm
Input Range	1.6Vpp	1.6Vpp
DC gain	60dB	52.5dB
CMRR	48.7dB	26.05dB
Slew Rate	100V/µs	2V/µs
Phase Margin	50^0	70^0
-3dB Gain	57dB	49.56dB
Unity Gain Frequency	26.0266MHz	37.442MHz
Total Power consumption	1.3mW	2.07mW

The table 4 shows the phase margin for different capacitor values for the simple two stage RC miller compensated op-amp.

Table-4: Phase Margin Values Obtained for Different Capacitor values .

Capacitor values F	Phase Margin ^{0}
1pF	25^0
2pF	34^0
3pF	42^0
4pF	46^0
5pF	50^0

The phase margin is improved by adjusting the load capacitor values in the simple two stage miller compensated op-amp.

6. CONCLUSIONS

A two stage RC Miller compensated op-amp in 0.18µm process has been designed to obtain high gain and low power consumption .The architecture and the circuits issues were discussed. The simulation results shows a DC gain of 60dB with 1.3 mW power consumption is obtained for the simple two stage op-amp .The simple two stage op-amp is showing a high gain and less power consumption by comparing with two stage op-amp using double cascode telescopic op-amp which is using a power supply of 1.8 V. And it gives a -3dB gain of 53.19dB and unity gain frequency of 26.0226MHz. The phase margin can be improved using the load capacitors. Because of the high gain and low power consumption a two stage RC Miller compensated op-amp is suitable for ADC applications.

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Benazir Kooran was born in Ernakulam , India in 1988. She received B.Tech degree in electronics and communication engineering from MG University, Kerala, India. She is

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