DESIGN AND ANALYSIS OF LOW POWER PSEUDO DIFFERENTIAL CLASS-AB TELESCOPIC OPERATIONAL AMPLIFIER

D. S. Shylu¹, D. Jackuline Moni², Neenu Brigit Francis³

¹Assistant Professor(SG), Electronics and Communication Engineering, Karunya University, Tamilnadu, India ²Professor, Electronics and Communication Engineering, Karunya University, Tamilnadu, India ³P G scholar, Electronics and Communication Engineering, Karunya University, Tamilnadu, India

Abstract

In this paper, the design of a pseudo differential class-AB cascoded telescopic op-amp for a 10-bit pipelined ADC is presented. A pseudo differential class-AB telescopic op-amp is used for the ADC architecture because of its large signal swing and high power efficiency. To further enhance the dc gain of the pseudo differential class-AB cascoded telescopic op-amp, two additional load capacitors are used. This proposed amplifier is designed in 180nm CMOS technology, and the simulation results show rail-to-rail input and output swings. With the modified pseudo differential class-AB cascoded telescopic op-amp the DC gain obtained is 43.41dB. The Common mode Rejection Ratio (CMRR) is 43.4dB, 91.19747° phase margin, 165.4544V/µs slew rate with 8-pF load capacitor and the power consumption is 0.4mW.

***_____

Keywords: ADC, CMRR, op-amp, pseudo-differential, slew rate, telescopic.

1. INTRODUCTION

Designing of high performance analog circuits is challenging with reduced power supply voltages [1]. In an analog circuit design the main important circuit is an operational amplifier. There is a tradeoff among speed, power, gain and other performance parameters at large power supply. The above performance parameters provide a contradictory choice among different op-amps.

Power reduction is a main issue among all aspects of portable or battery-operated applications. In low-voltage Pipelined ADC design, the most power-hungry block is the operational amplifier. Therefore several approaches are designed to reduce the power consumed by the operational amplifier. Usually conventional pipelined ADC's require high gain amplifiers for its accurate signal processing. So such ADC's are unsuitable for low power applications. The split capacitor CDS technique in pipelined ADC [2] helps in avoiding the use of high gain amplifiers by correcting finite op-amp gain error in low gain op-amps.

Telescopic op-amp has low power consumption and better bandwidth than any other topologies. So that pseudo differential class-AB approach is used for the telescopic cascode op-amp to enhance the effective values of the slew rate and further more reducing the power consumption. Thus a low power op-amp is designed which is required for pipelined ADC, to make it suitable for low power applications. In this paper the class-AB capacitors are used to enhance the DC gain and bandwidth of the operational amplifiers. In addition to that two load capacitors are employed to further more enhance the DC gain of the operational amplifier. Since the power dissipation of the op-amp depends on the load capacitors and the unity gain frequency, optimum values for the load capacitors are designed to further more reduce the power consumption of the pseudo differential class-AB telescopic op-amp.

This paper is organized as follows: In section 2 the modified architecture of the pseudo differential class-AB telescopic opamp is described which includes the basic operation of this opamp. Section 3 describes the design procedure of the operational amplifier and gives the aspect ratios of the transistors. Section 4 presents the simulation results and power comparison of the modified op-amp. Section 5 gives the conclusion.

2. PSEUDO DIFFERENTIAL CLASS-AB TELESCOPIC CASCODED OP-AMP

ARCHITECTURE

Usually pipelined ADC's requires high gain amplifiers, which makes them unsuitable for low power applications. So in order to make it suitable for low power applications a low power pseudo differential class-AB telescopic op-amp is designed.

Even though telescopic op-amp has smaller swing which means that they have low dynamic range, this is offset by the

low noise factor. So the telescopic op-amp is a better choice for low power application circuits. The single stage architecture is normally designed for low power consumption. The figure 1, shows the circuit diagram of the modified pseudo differential class-AB telescopic cascaded operational amplifier. The structure employs a switched capacitor level shifter to provide a signal-dependent current in the current source of the common-source amplifier [4].

The structure of the op-amp is called as telescopic because, the cascades are connected in series between the power supplies resulting in a structure in which the transistors in a branch are connected in a line. The transistors M1-M2 and M7-M8 are the transistors must have at least V_{dsat} , to offer good common mode rejection ratio and dc gain [8-9].In figure 1, C_1 and C_2 are the capacitors used for further improvement in the dc gain and bandwidth of the amplifier. In addition to that two load capacitors are employed to further more enhance the DC gain and also the output swing. The equivalent transconductance G_m of the amplifier is

$$Gm = gm_N + \left(\frac{C_1 + C_2}{C_p + C_1 + C_2}\right)gm_P \tag{1}$$

Where gm_N and gm_P are the transconductance of M_n and M_p respectively [2]. The equivalent transconductance is proportional to the ratio of the parasitic capacitor of PMOS C_p and the class-AB capacitor ($C_1 + C_2$).



Fig -1: Pseudo differential class-AB telescopic op-amp

3. DESIGN PROCEDURE

The supply voltage given to the pseudo differential class-AB telescopic cascoded op-amp circuit is 1.8Vp-p. Also an initial power of 1μ W is assumed, so the total biasing current is 0.5 μ W. This is the total current which should be divided into two branches equally. So that, a total current of 0.25 μ W will flows to each of the two branches in the op-amp structure. Since the mobility of PMOS is approximately 2.5 times less than NMOS the overdrive voltage of PMOS is greater than that of NMOS.

The W/L ratio in (μM) can be calculated by the drain current equation of MOSFET in saturation region. Thus the aspect ratio (W/L) of the transistors can be calculated by this drain current equation as we know the current and overdrive voltage.

$$I_D = \frac{\mu_n}{2} C_{ox} \frac{W}{L} \left(V_{gs} - V_t \right)^2$$
(2)

In equation I_D is the biasing current, μ_n and C_{ox} are the process parameters, W/L is the aspect ratio. Also Vgs and Vt are the gate source voltage and the threshold voltage of the device respectively. In this op-amp design it is assuming that $\mu_n ^* C_{ox}$ and $\mu_p ^* C_{ox}$ as $110 \mu A/V^2$ and 60 $\mu A/V^2$ respectively. The aspect ratio (W/L) of the transistors can be calculated by this drain current equation as we know the current and overdrive voltage [3].

The circuits were simulated in 180nm technology. The substrate terminal of all the NMOS and PMOS is connected to the ground and V_{dd} respectively. In order to further enhance the gain of the pseudo differential amplifier class-AB telescopic cascaded op-amp additional load capacitors are added. Hence the gain is improved more in comparison to the gain reported in [2].

Table -1 shows the aspect ratio of the transistors designed in the op-amp circuit.

Transistors	Aspect Ratio(W/L)
M0, M1	4.625/0.18µm
M3,M4	10.4/0.18 µm
M5, M6	4.48/0.18 μm
M7, M8	7.41/0.18 μm

Table -1: Aspect ratio of the transistors

4. SIMULATION RESULTS

4.1 Transient Analysis

The class-AB pseudo differential telescopic operational amplifier was designed. The simulation is done in 180nm technology. The schematic of the pseudo differential class-AB telescopic op-amp is shown in figure 2.

In the schematic, Vin+ and Vin- are the two input signals given to the circuit which are of 1.6Vp-p. The transient response is obtained for the input frequency of 10MHz using Virtuoso Schematic Editor. The transient waveform of pseudo differential class-AB telescopic operational amplifier is shown in figure 3.



Fig -2: Schematic of pseudo differential class-AB telescopic op-amp

Fig -3: Transient analysis of pseudo differential class-AB operational amplifier

The inputs Vin+ and Vin- are of 1.6 Vp-p and the outputs Vo+ and Vo- have a peak to peak of 1.8V.

4.2 AC Analysis

The AC analysis of pseudo differential class-AB telescopic operational amplifier is done with an input frequency of 10MHz and 1.6Vp-p. The AC response of the operational amplifier is shown in figure 4.



Fig -4: Transient analysis of pseudo differential class-AB operational amplifier



From figure 4, it is observed that the dc gain of the pseudo differential class-AB telescopic operational amplifier is improved to 43.4147dB. Also the phase plot is also shown in this figure. The phase margin of the designed pseudo differential class-AB telescopic op-amp is 91.19747°. The phase degree at which the dc gain becomes zero is known as the phase margin of an operational amplifier.

The -3dB gain of the operational amplifier designed is 40.4739dB. The plot is shown in figure 5.



Fig -5: -3dB gain plot of op-amp

Figure 6, shows the test circuit used for obtaining the CMRR and the slew rate.



Fig -6: Op-amp test circuit

From figure 7, the CMRR of the operational amplifier obtained is 43.4dB. The value is almost equal to the dc gain of the operational amplifier.

The CMRR of an op-amp is the rejection by the device of unwanted input signals common to both input leads, relative to the wanted difference signal.



Fig -7: CMRR of op-amp

The maximum slew rate that can be obtained by the operational amplifier is given by,2 Π Vpeakf_{max} [3]which is 2*3.14*1.6*10M. The theoretical value obtained is 100.48V/µs. The slew rate of the pseudo differential op-amp is given by $\frac{I_{tail}}{C_L}$ where I_{tail} is the tail current and C_L is the load capacitance [3].

The slew rate obtained is 165.4544V/µs. The output waveform of the slew rate is shown in figure 8. The slew rate can be a value greater than or equal to the maximum slew rate of an operational amplifier.

Slew rate is defined as the maximum rate of change of output voltage per unit time and is expressed as volt per micro second.



Fig -8: Output waveform of slew rate of op-amp

The settling time of an amplifier is the time elapsed from the application of an ideal instantaneous step input to the time at which the amplifier output has entered and remained within a specified error band, usually symmetrical about the final value. The settling time of the pseudo differential class-AB telescopic operational amplifier is $1.952 \ \mu s$.

Table-2: Performance summary of modified pseudo

 differential telescopic operational amplifier

Technology	180nm
Supply voltage	1.8V
Input range	1.6Vp-p
Power consumption	0.4mW
Phase margin	91.19747 ⁰
Unity GBW	820.462MHz
DC gain	43.4147dB
CMRR	43.4dB
Slew rate	165.4544V/μs
Settling time	1.952 µs

Table -2 shows the performance summary of the modified pseudo differential class-AB cascode telescopic operational amplifier during the simulation of the operational amplifier.

Table -3 shows the power comparison of the pseudo differential class-AB telescopic operational amplifier with other reported work in the Literature survey. The power obtained for the designed pseudo differential op-amp is also shown in Table-3.

Table-3: Power Compa	rison	Table
-----------------------------	-------	-------

Reference	Power Obtained
[4]	16mW
[10]	2.8mW
[13]	0.5mW
This work	0.4mW

5. CONCLUSIONS

A modified pseudo differential class-AB telescopic op-amp is designed and simulated in 180nm technology for low power Pipelined ADC applications. The class-AB pseudo differential op-amp is chosen because of its low power efficiency and signal swing. The dc gain obtained for the op-amp is 43.4147dB and the slew rate obtained is $165.4544V/\mu$ s. Also the CMRR of the op-amp is 43.4dB and the power consumed is 0.4mW.Simulation results shows that the power consumption of the modified pseudo differential class-AB cascode telescopic operational amplifier is low and the op-amp can be used for low power Pipelined ADC applications.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the support provided by the Centre of excellence in VLSI Lab, Karunya University.

REFERENCES

- K. Gulati and H.-S. Lee, —A High-Swing CMOS Telescopic Operational Amplifier, in *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 12, pg. 2010, December 1998.
- [2] Jin-Fu Lin, Soon-Jyh Chang, Chun-Cheng Liu, Chih-Hao Huang, — A 10-bit 60-MS/s Low-Power Pipelined ADC With Split-Capacitor CDS Technique, in IEEE transactions on circuits and systems—ii: express briefs, vol. 57, no. 3, march 2010.
- [3] D. S. Shylu, Dr. D. Jackuline Moni. Anita Antony, A J Sowjanya. K, Neetha C John- A single stage low gain pseudo differential class-AB telescopic cascaded opamp for pipelined ADC, in International journal of advanced computer research, vol. 2, no. 4, issue-6, December 2012.

- [4] Taherzadeh-Sani,M, Lotfi, R. ,Shoaei, O, —A pseudoclass-AB telescopic-cascode operational amplifier, in IEEE transactions on circuits and systems-Vol 1,pg. 737-40,May 2004.
- [5] Behzad Razavi, Design of analog CMOS integrated circuits, Tata McGraw-Hill Edition 2002.
- [6] J. Ramirez-Angulo, R. G. Carvajal, A. Torralba, and C. Nieva, —A new class AB differential input stage for implementation of low-voltage high slew-rate opamps and linear transconductors, in Proc. 2001 IEEE Int. Symp. Circuirs Systems, May 2001, Vol. 1, pp.671-674.
- [7] Fan Mingjun, Ren Junyan, Guo Yao, Li Ning, Ye Fan, Li Lian- A novel low voltage operational amplifier for low power pipelined ADCs, Journal of semiconductors, January 2009.
- [8] A. R. Mortazavi, M. R. Hassanzadeh, J. Talebzadeh, and O. Shoaei, "Design Procedure for a High dc-gain and High bandwidth amplifier", Master of Science thesis, University of Tehran, Iran, 2001.
- [9] A. J. Gano and J. E. France, "Fully differential variable gain instrumentation amplifier based on a fully differential DDA topology," IEEE Journals of Solid State Circuits, vol.78, No.3, pp-5682-5689, 1998.
- [10] Chaloenlarp. W, "Low voltage pipelined ADC using class-AB pseudo differential OTA", IEEE International symposium on communication and information technology, vol.1, pp-128-132, 2004.
- [11] Suadet .A, Kasemsuwan. V,"A CMOS invertor based class-AB pseudo differential amplifier for HF applications", IEEE International conference of Electron devices and solid state circuits, Dec. 2010.
- [12] Thongleam. T, "A 0.5 V class-AB quasi FGMOS pseudo fully differential CMOS op-amp with rail-to-rail input/output swing", International conference on Modeling, Simulation and Applied Optimisation", April 2011.
- [13] Herve Facpong Achigui, "A 1-V DTMOS-based class-AB operational amplifier: Implementation and experimental results", IEEE journal of solid state circuits, vol.41, issue:11, pp-2240-2248., Nov.2006.

BIOGRAPHIES



D.S.Shylu is working as an Assistant Professor (SG) in ECE Department, Karunya University. She received her BE degree in EEE from M.S.University, Tirunelveli and M.Tech in VLSI Design from SASTRA University, Thanjavore

.Now pursuing Ph.D in Karunya University, Coimbatore. She has 11 years of teaching experience. She has published more than 25 papers in National and International Journals and conferences. Her areas of interest are Analog VLSI Design, Device modeling, Low Power VLSI Design.



Dr.D.Jackuline Moni working as a Professor in ECE Department, Karunya University. She is in charge of M.Tech (VLSI design) in Karunya university. She did her B.Tech in Electronics Engineering at Madras Institute of Technology. Anna

University, M.E in (Applied Electronics) from Government College of Technology, Coimbatore, and her Ph.D in (VLSI DESIGN) from Anna University, Chennai. She has over 25 years of teaching experience .She has guided more than 70 UG and PG projects in the area of VLSI design and Embedded systems. She has presented and published more than 60 papers in National and International Journals and conferences. Her areas of interest are CAD VLSI Design, Device modeling, Low Power VLSI Design, analog VLSI and Embedded System Design.



Neenu Brigit Francis, was born in Kottayam, India, in 1989. She received B-Tech degree in Applied electronics and Instrumentation engineering from MG University, Kerala, India. She is currently pursuing her M-Tech degree in VLSI Design

at Karunya University, Tamil Nadu, India. Her post graduate research is directed towards design of low power pipelined ADCs.