PERFORMANCE ANALYSIS OF FULLY DEPLETED DUAL MATERIAL GATE (DMG) SOI MOSFET AT 25NM TECHNOLOGY

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Abstract

The emergence of CMOS technology in the semiconductor industry is predominant. However, there is degradation of MOSFET characteristics as the technology is scaled down to nanometer regime. In this paper, Dual Material Gate MOSFET is analyzed to study the performance characteristics like DIBL, Subthreshold Slope and I_{on}/I_{off} ratio using TCAD simulation. We observed that the DMG MOSFET is effective in reducing DIBL. Also, by using HfO_2 as spacer, we obtained improvement in the I_{on}/I_{off} ratio and reduction in DIBL and Subthreshold Slope.

Keywords: *DIBL, Silicon-On-Insulator, Single Material Gate, Dual Material Gate, MOSFET, SCE, TCAD, Ion/Ioff*

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1. INTRODUCTION

The Dual Material Gate is implemented by making half of the gate with one metal and the other half with another metal. There is a difference in the workfunction of both the metals such that for an n-channel MOSFET, the workfunction of the metal used in the source side is higher than the workfunction of the metal used in the drain side and vice versa for a p-channel MOSFET, which in turn introduces a step in the channel potential. This paper is a study of performance improvements of DMG MOSFET and its effective suppression of the short channel effects in FD SOI MOSFETs. A similar concept was first proposed by M. Shur [1] by applying different gate bias in split-gate structure. But there was a problem of fringing capacitance which made it difficult to realize the two metal split-gate FET. As the distance between the two metal gates decreases, the fringing capacitance of the split-gate FET increases. The Dual Material Gate structure was first proposed by Long [2] in 1999. Gate material engineering was used instead of doping engineering [3-6]. When we are using gate material engineering, the channel potential is redistributed in such way that the short channel effects are reduced and transport of carriers is enhanced. There is a way of fabricating Hetro-Material Gate Structure by inserting one additional mask in the bulk CMOS processing technology which was first suggested by Zhou [7]. He also showed the characteristics of this new structure.

2. SHORT CHANNEL EFFECTS

Due to the extent of integration getting more and more, it is important to reduce the modern VLSI's power consumption. This power consumption may be reduced by using a lower power supply voltage. But, by doing so, the current driving capability will get degraded. Thus, there is a strong need of scaling MOS devices in order to improve the current driving capability so that we can fabricate VLSI chips with improved functionality [8]. If the channel length of a device is reduced, the threshold voltage of the device reduces. This dependence of device characteristics on channel length is a Short Channel Effect (SCE) due to which there is a variation in the device characteristics due to variation in the channel length during manufacturing. This also affects the controllability of the gate voltage over the channel and hence drain current. Thus, the subthreshold slope of the device gets degraded and there is an increase in the drain off-current as a result of increase in leakage. There are some popular ways of preventing SCEs like using shallow source/drain junctions and thinning gate oxide [13].

While scaling down the device, if the channel length is of the order of channel depth, then SCEs occur. When we scale down the device, channel length is reduced which reduces the threshold voltage and hence degrades the control of the gate voltage over the channel due to increase in the charge sharing effect from source/drain. The first SCE model proposed by Poon and Yau [9] describes the charge sharing effect by gate and drain electric fields in the depletion channel.

When the device is operating in the weak inversion mode, there exists a potential barrier between the source and the channel which the electrons have to cross before entering the channel. This barrier height should ideally be controlled by the gate voltage. But, due to DIBL (as indicated in Fig. 1), when we change the drain voltage, there is a change in this barrier height. If we increase the potential at the drain side, this barrier height gets reduced and more carriers enter the channel from source leading to an increase in the drain off-current of the device. Thus, due to DIBL, the drain voltage along with

the gate voltage is responsible for controlling the drain current.

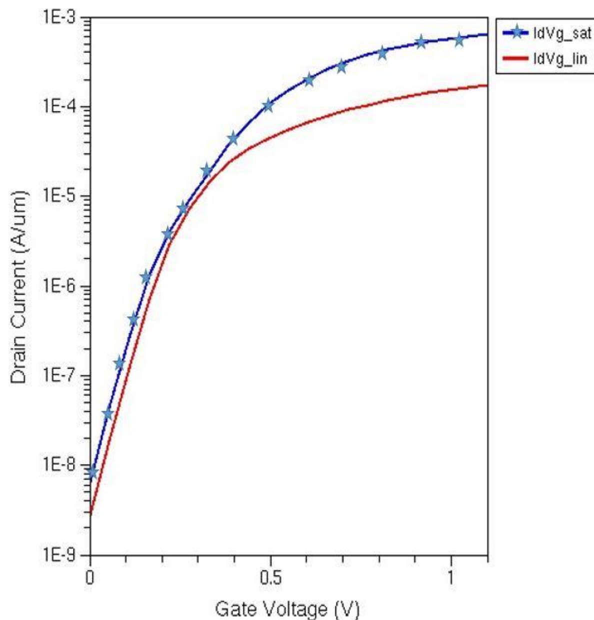

Fig 1: DIBL Curve of SMG FD SOI MOSFET

3. DEVICE STRUCTURE

The dual material gate FD SOI MOSFET structure is as shown in Fig. 2. As we are working at 25nm technology, the channel length is 25nm, the lengths of source and drain are 45nm. Source/drain thickness is 6nm. The thickness of buried oxide layer is 20nm. Half of the gate is made up of Molybdenum and half of the gate is made up of Manganese.

One half of the gate near the source side is made up of Molybdenum and the other half of the gate is made up of Manganese. There is a reduction in hot carrier effect due to half of the gate at the drain side being made up of lower workfunction metal which reduces the peak electric field.

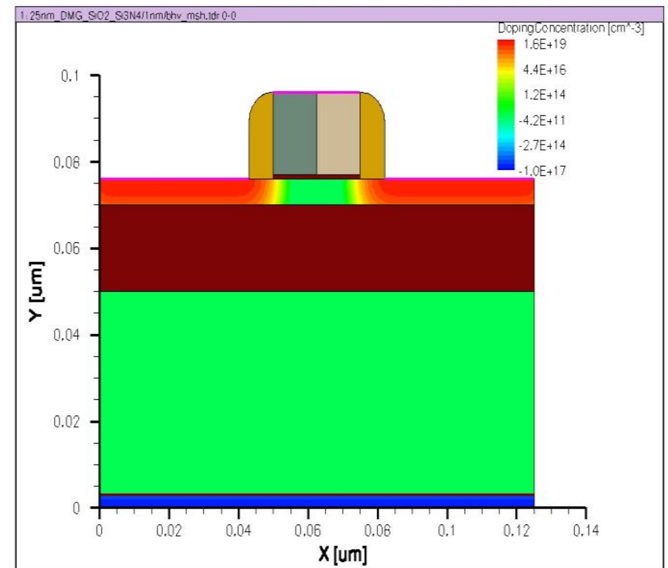

Fig 2: Device structure of DMG FD SOI MOSFET

Also, there is an increase in the average velocity of electrons due to the half of the gate at the source side being made up of higher work function metal which enhances the peak electric field at the source side. Thus, in the dual material gate structure, there is an increase in transconductance and reduction in drain conductance.

4. RESULTS AND DISCUSSIONS

The DIBL curves for Single Material Gate Fully Depleted Silicon on Insulator MOSFET and Dual Material Gate Fully Depleted Silicon on Insulator MOSFET are plotted and the improvement in DIBL can be clearly seen from Fig. 3.

As explained earlier, there is a reduction in DIBL from 30.7 mV/V for SMG FD SOI MOSFET to 10.1 mV/V for DMG FD SOI MOSFET. We have also studied and shown the effects of variation of dielectric constant of spacer material on Ion/Ioff ratio (Fig. 4), DIBL (Fig. 5), Subthreshold Slope (Fig. 6). There is a reduction in off current of the device due to increase in the threshold voltage with an increase in dielectric constant of the spacer material which results better subthreshold slope and increased Ion/Ioff ratio.

5. CONCLUSIONS

It is concluded that there is a significant performance improvement in case of Dual Material Gate Fully Depleted Silicon on Insulator MOSFET as compared to its single material gate counterpart. Also, we observe that with an increase in the dielectric constant of the spacer material, there is a reduction in leakage in the device and hence the Ion/Ioff ratio is getting improved as the dielectric constant of the spacer material is increased. Also, the DIBL and Subthreshold slope is reduced with an increase in the dielectric constant of

the spacer material. Thus, DMG MOSFET is suitable candidate for the VLSI application in nanometer regime.

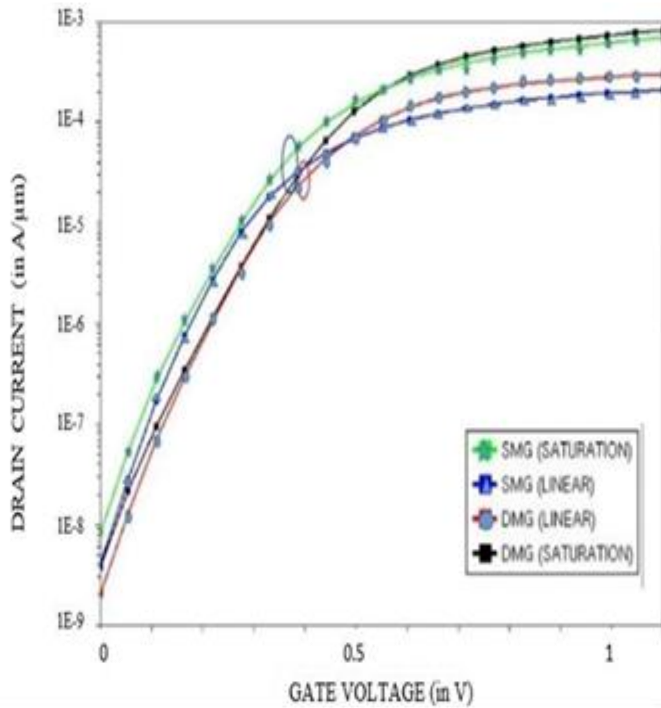

Fig 3: Comparison of DIBL Curves of SMG and DMG FD SOI MOSFET

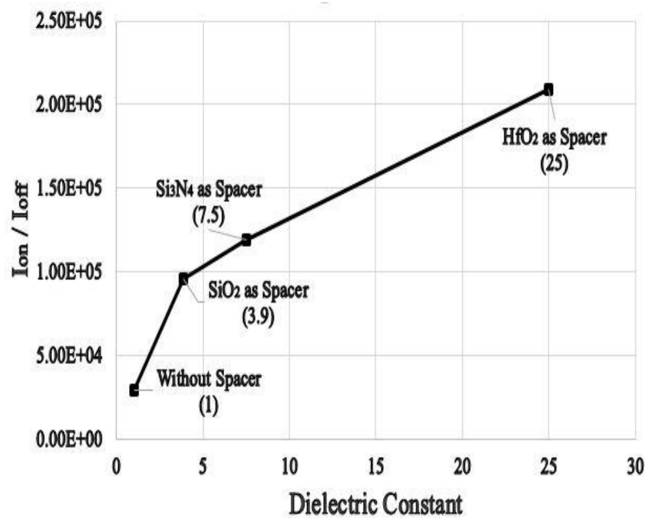

Fig 4: I_{on}/I_{off} graph of DMG FD SOI MOSFET for different spacer materials

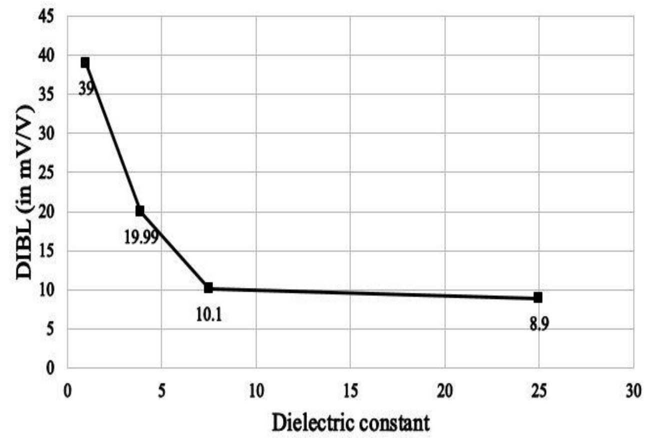

Fig 5: DIBL graph of DMG FD SOI MOSFET for different spacer materials

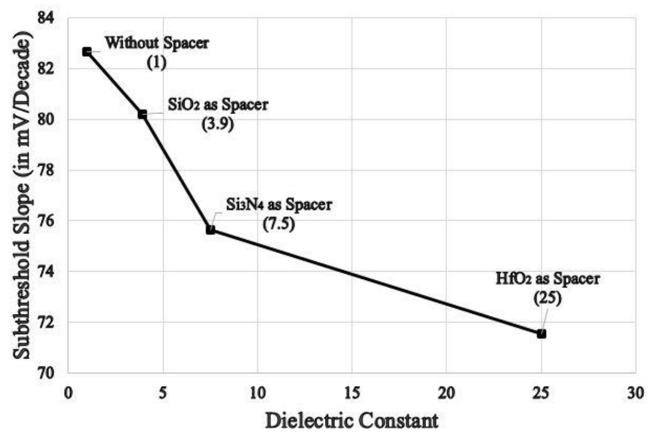

Fig 6: Subthreshold graph of DMG FD SOI MOSFET for different spacer materials

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BIOGRAPHIES

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