

FPGA BASED SOLUTION FOR THE IDENTIFICATION OF RADAR PULSE SEQUENCES FOR DEFENSE APPLICATIONS

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Abstract

The main objective of this paper is to design a generalized architecture for polyphase code identification used in RADAR signal processing applications. The proposed VLSI architecture will identify the type of a given polyphase code, amount of phase change and number of phase changes. RADAR signal processing applications require a set of sequences with individually peaky autocorrelation and pair wise cross correlation. Obtaining such sequences is a combinatorial problem. This paper aims at implementation of an efficient VLSI system for the design of polyphase codes identification useful for RADAR applications. The VLSI system is implemented on the field programmable gate array as it provides the flexibility of reconfigurability and reprogrammability and it is a real time signal processing solution which identifies the polyphase codes. The simulation results and the FPGA implementation shows the successful code identification, amount of phase, number of phase changes for a given input sequence.

Keywords- Code Identification, Phase Identification, Frank Codes, Polyphase codes, RADAR, FPGA, VLSI, LPI

I. INTRODUCTION

Polyphase code identification and localization are basic and important problems in RADAR systems. Localizing the received code is an important task in the detection of polyphase codes. Localization of the received signal can lead to incorrect target range measurements. Pulse RADAR that uses pulses as the RADAR signal is being used in aviation control, weather forecasting, and ships. The strength of the received signal by the radar varies with the distance from radar to the target and is also dependent on the target RADAR cross section. The proposed architecture will identify the type of polyphase code, amount of phase change and number of phase changes among the polyphase codes which are present in the Low Probability of Intercept (LPI) RADAR. Identification of these parameters like code, phase, number of phase changes can guide and retransmit to the transmitter without any effect to our electronic systems. With this system the unwanted signals are retransmitted to the transmitter.

2. POLYPHASE CODES

The transmitted complex phase coded signal can be expressed in the following form

$$s(t) = Ae^{j2\pi f_c t + \phi_i} \quad (1)$$

Where A is the amplitude, f_c is the carrier frequency and ϕ_i is the discrete phase sequence. Each phase has the same time duration. In the following, five different polyphase pulse

compression codes are presented. The codes presented are the Frank, P1, P2, P3, and P4 codes.

2.1 Frank Codes

The Frank code is a step approximation to a linear frequency modulation (LFM) waveform using N frequency steps and N samples per frequency. Thus, the total number of samples in a Frank code is N^2 . The phase of the i^{th} sample of the j^{th} frequency of a Frank code is given as

$$\Phi_{ij} = \frac{2\pi}{N} (i-1)(j-1) \quad (2)$$

Where $i = 1, 2, \dots, N$ and $j = 1, 2, \dots, N$. The pulse compression ratio of the Frank code is N^2 . The Frank code has the highest phase increments from sample to sample in the center of the code, where the numbers represent multiplying coefficients of the basic phase angle $2\pi/N$.

2.2 P1 Polyphase Codes

The P1 code also consists of N^2 elements as Frank code, that way P1 code signal with $N = 4$ produces a matrix of 16 different phases, if $N = 8$ produces a matrix of 64 phases. In a p1 code, the phase of the i^{th} sample of the j^{th} frequency is given by

$$\Phi_{ij} = \frac{-\pi}{N} [N - (2j - 1)] [(j - 1)N + (i - 1)] \quad (3)$$

Where $i = 1, 2, \dots, N$ and $j = 1, 2, \dots, N$.

2.3 P2 Polyphase Codes

This code is essentially derived in the same way as the P1 code. The P2 code has the same phase increments within each group as the P1 code, except that the starting phase is different. The P2 code is valid for N even, and each group of the code is symmetric about 0 phases. In a p2 code, the phase of the i^{th} sample of the j^{th} frequency is given by

$$\Phi_{ij} = \left\{ \frac{\pi}{2} [(N - 1)N] - \left[\frac{\pi}{N} (i - 1) \right] \right\} [N + 1 - 2j] \quad (4)$$

Where $i = 1, 2, \dots, N$ and $j = 1, 2, \dots, N$.

2.4 P3 Polyphase Codes

This code is derived by converting a linear frequency modulation waveform to baseband using a local oscillator on one end of the frequency sweep and sampling the In phase component I and Quadrature component Q at the Nyquist rate. If the waveform has a pulse length T and frequency $f = f_0 + kT$, where k is a constant and the bandwidth of the signal will be approximately $B = kT$. The bandwidth will support a compressed pulse length of about $t_c = 1/B T$ and the waveform will provide a pulse compression ratio of $pc = \frac{T}{t_c} = BT$. Assuming that the first sample of I and Q is taken at the leading edge of the waveform, the phases of successive samples taking t_c apart are

$$\Phi_i = 2\pi \int_0^{(i-1)t_c} [(f_0 + kt) - f_0] dt = \pi k (i - 1)^2 t_c^2 \quad (5)$$

where $i = 1, 2, \dots, N$. Substituting $k = B/T$ and $t_c = 1/B$, the equation can be written as

$$\Phi_i = \frac{\pi(i-1)^2}{BT} = \frac{\pi(i-1)^2}{N} \quad (6)$$

2.5 P4 Polyphase Codes

The P4 code consists of discrete phases of the linear chirp waveform taken at specific time intervals and exhibits the same range Doppler coupling associate with the chirp waveform. Phase code elements of the P4 code are given by

$$\Phi_i = \frac{\pi(i-1)^2}{N} - \pi(i-1) \quad (7)$$

Where $i = 1$ to N

2.6 Barker Codes

Barker sequence is a finite sequence of N values of '+1' and '-1'. The coding scheme used in direct sequence spread spectrum (DSSS) radio systems. A_i for $i = 1, 2, 3, \dots, N$. such that the off peak autocorrelation coefficients.

$$\sum_{i=1}^{i-k} a_i a_{i+k} \leq 1 \quad (8)$$

For all $1 \leq k < i$. Barker codes are used for pulse compression of radar signals. There are Barker codes of lengths 2, 3, 4, 5, 7, 11, and 13, and it is conjectured that no longer Barker codes exist.

3. PROPOSED ARCHITECTURE

Fig 1 show the block diagram for code identification, phase identification and number of phase changes identification. An input sequence of N bit length is applied to the proposed system. The first 3 MSB bits $X_{N-1}, X_{N-2}, X_{N-3}$ are useful for code identification and the remaining bits from X_{N-4} to X_0 bits are used for phase identification. The input code word format is shown in table 1.

Table 1 Generalized Input Code Word.

Code Identification Bits			Phase Identification Bits			
X_{N-1}	X_{N-2}	X_{N-3}	X_{N-4}	..	X_1	X_0

X_{N-4} phase identification bits will give the 2^{N-4} phase changes. The system will find which type of code it is by comparing the coefficients of those respective codes i.e. whether it is Frank, p1, p2, p3, p4 and Barker codes that are stored in the memory.

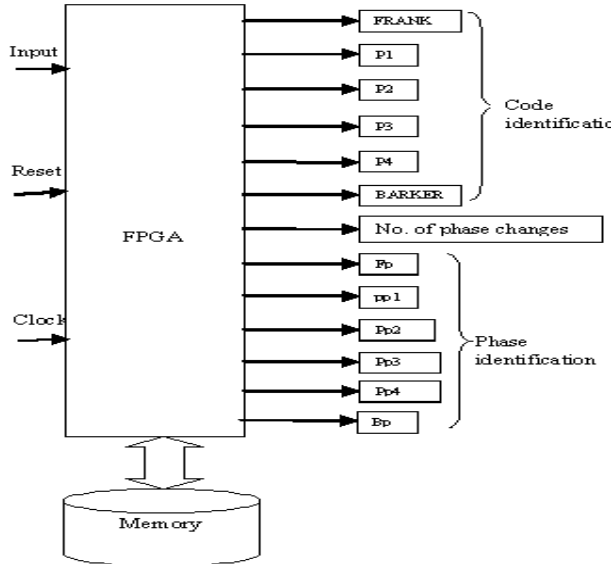


Fig 1 Block Diagram for Code Identification, Phase Identification and Number of Phase changes Identification.

The system has other inputs of clock and reset signal. The count block will give the number of phase changes in the respective code. The registers fp, pp1, pp2, pp3, pp4 are useful for storing the amount of phase change from the adjacent alphabets of the codes.

3.1 Code Identification

When an input code word shown in table 1 is given by the MSB bits X_{N-1} , X_{N-2} , X_{N-3} are used for code identification where the code identification bits X_{N-1} , X_{N-2} , X_{N-3} are given as inputs. The output is the corresponding identified (frank, p1, p2, p3, p4 and barker) code. Figure 2 shows the generalized block diagram for code identification.

The code identification logic and its corresponding input output relationships are shown in the table 2. When the code identification bits are 000 then it will identify as frank code and similarly when the code identification bits are 001,010,011,100 and 101 they correspond to the p1, p2, p3, p4 and barker codes respectively.

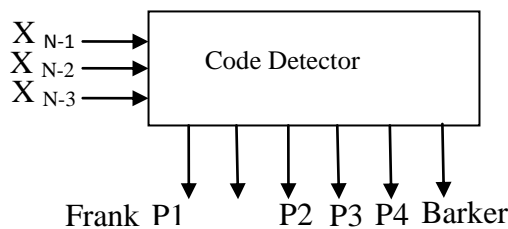


Fig 2 Block Diagram for Code Identification

3.2 Phase Identification

The remaining bits from X_0 to X_{N-4} are used for phase identification. Table 3 gives the phase change identification and amount of phase change from one phase to another phase among the polyphase codes. X_{N-4} phase identification bits will give the 2^{N-4} phase changes. The phases are given as from ϕ_0 , $\phi_1, \dots, \phi_2^{N-5}, \phi_2^{N-4}$.

Table 2 Generalized Code Identification Logic

Code identification bits			Code
X_{N-1}	X_{N-2}	X_{N-3}	
0	0	0	Frank
0	0	1	P1
0	1	0	P2
0	1	1	P3
1	0	0	P4
1	0	1	Barker
1	1	0	Used for Future Expansion
1	1	1	

Table 3 Generalized Phase Change Identification.

X_{N-4}	X_{N-5}	X_1	X_0	Phase
0	0	0	0	ϕ_0
0	0	0	1	ϕ_1
0	0	1	0	ϕ_2
.
.
1	0	0	0	ϕ_{N-4}
1	0		0	1	ϕ_{N-3}
.
.
1	1	1	0	ϕ_2^{N-5}
1	1	1	1	ϕ_2^{N-4}

Fig 3 shows the generalized block diagram for the phase change identification. The phase identification unit comprises of state machine diagram as shown in the figure 4

Code identification output enables the corresponding phase identification units. Based on the identified code, the corresponding state machine will be activated. The counter will identify the number of phase changes in the given sequence. For the N-4 bits it will identify 2^{N-4} phase changes. The enable inputs are useful for activating the appropriate state machine for calculating the number of phase changes and amount of phase. The State machine consists of 2^{N-4} states and $2^{N-4}+1$

outputs and N-4 inputs. The Fig 5 shows the N-4 inputs and N-4 next state outputs and corresponding complements. The reset and clock are given as the other inputs of the phase identification unit.

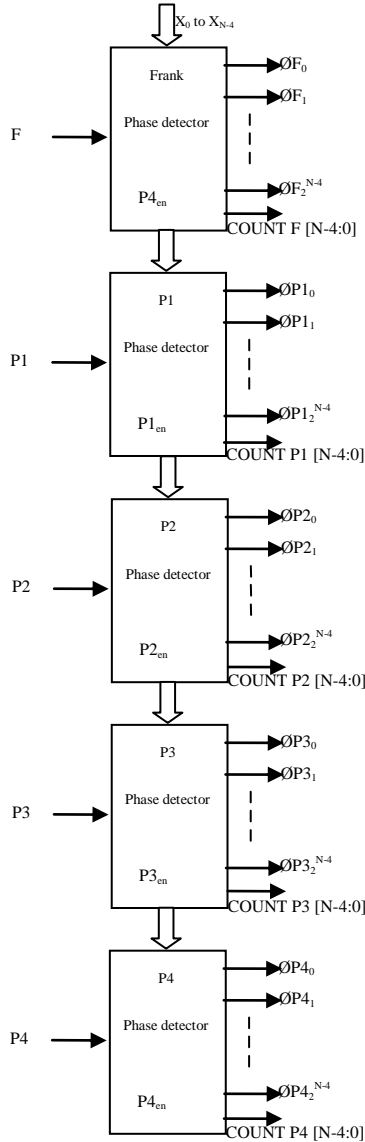


Fig 3 Block Diagram for Phase Change Identification

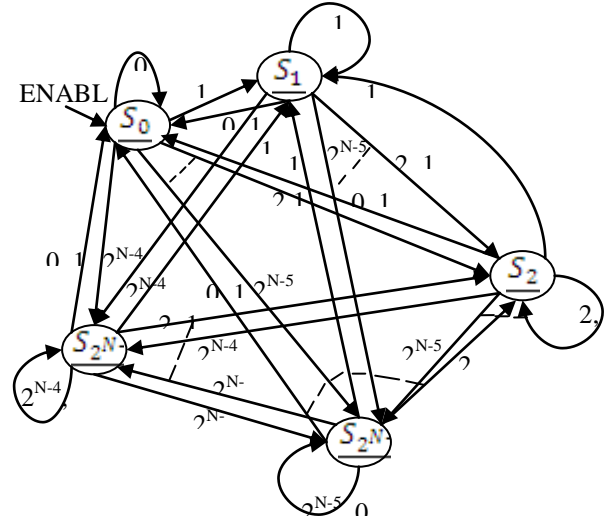


Fig 4 State diagram for 2^{N-4} Phase Identification

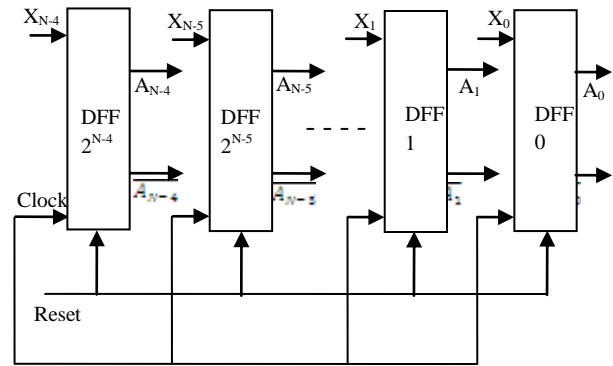


Fig 5 Generalized Hardware Implementation for Phase Change Identification

From the table 3 the generalized phase changes equations are given below. The phase change can be calculated by using the given equations.

$$\left. \begin{aligned} \Phi_0 &= \overline{A_{N-4}} \overline{A_{N-5}} \dots \overline{A_1} \overline{A_0} \\ \Phi_1 &= \overline{A_{N-4}} \overline{A_{N-5}} \dots A_1 \overline{A_0} \\ &\vdots \\ 2^{\Phi_{N-5}} &= A_{N-4} A_{N-5} \dots \overline{A_1} \overline{A_0} \\ 2^{\Phi_{N-4}} &= A_{N-4} A_{N-5} \dots A_1 \overline{A_0} \end{aligned} \right\} (9)$$

The number of phase change identification can be identified by using the following equations

$$X(n) = \{ X_{N-4}, X_{N-5}, \dots, X_1, X_0 \} \quad (10)$$

$$X(n-1) = \{ A_{N-4}, A_{N-5}, \dots, A_1, A_0 \} \quad (11)$$

The phase change is given by

$$Z = X(n) \oplus X(n-1) \tag{12}$$

if $Z=1$ then count = count+1;
 else
 count = count;

The count value depends on the number of phases. The number of phases is equal to ϕ_2^{N-4} then the count value $2^{\text{count}} \geq \phi_2^{N-4}$.

4. EXAMPLE FOR FOUR PHASE IDENTIFICATION

For a five input sequence the first three MSB bits are used for the code identification and the remaining two bits are used for the phase identification. The clock and reset signals are given to the buffer register. The buffer register is used to split the code identification bits and phase identification bits. The code identification block is used to identify which type of code whether frank, barker, and polyphase code i.e. p1, p2, p3, p4. The level detection unit will give the phases for the corresponding inputs bits. The Z_{phase} will give the phase change among the phases. The phase display unit will give the phase angle corresponding to the four phases. The counter block will give the number of phase changes among the four phases. The internal block diagram of the system is given in Fig 6.

Fig 7 shows the code identification unit for the five input sequences. The three MSB bits $X_{in}[4]$, $X_{in}[3]$, $X_{in}[2]$ are the code identification bits. These are the inputs given to the code identification unit. The corresponding codes frank, p1, p2, p3, p4 and barker are the outputs of the code identification unit. The clock and reset are the other inputs of the code identification unit. The code identification logic is shown in table 4.

Table 4 Code Identification Logic

$X_{in}[4]$	$X_{in}[3]$	$X_{in}[2]$	FRANK	P1	P2	P3	P4	BAR KER
0	0	0	1	0	0	0	0	0
0	0	1	0	1	0	0	0	0
0	1	0	0	0	1	0	0	0
0	1	1	0	0	0	1	0	0
1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	1

If the three MSB bits shows 000 then it will identify the frank code similarly for 001,010,011,100,101 it will give p1, p2, p3, p4, barker codes and the bits 110, 111 are reserved for the future expansion. Figure 8 shows the level detection unit.

$X_{in}[0]$, $X_{in}[1]$ are the inputs and $Z1$, $Z2$, $Z3$, $Z4$ and Z_{phase} are the outputs of the level detection unit. Clock and reset are given as the other inputs of the level detection unit.

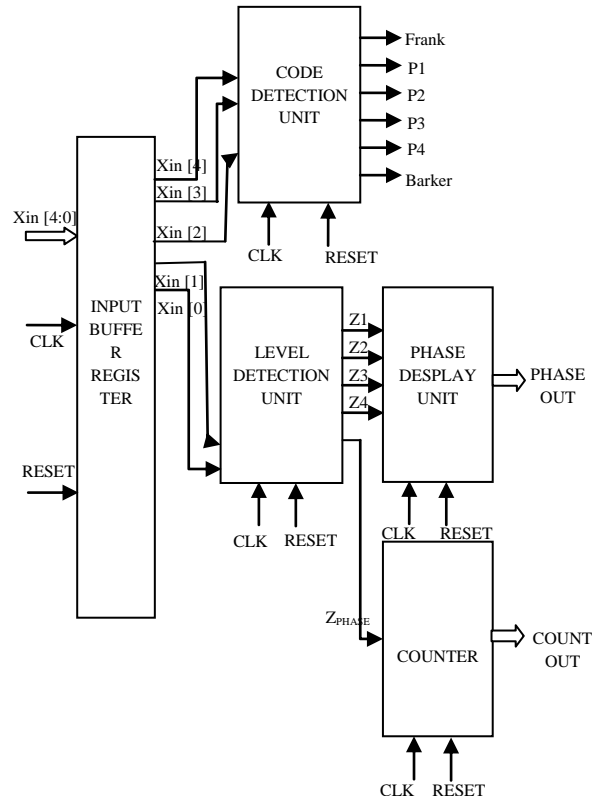


Fig 6 Top Module of the system

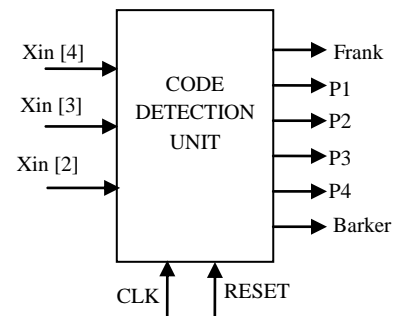


Fig 7 Code Identification Unit

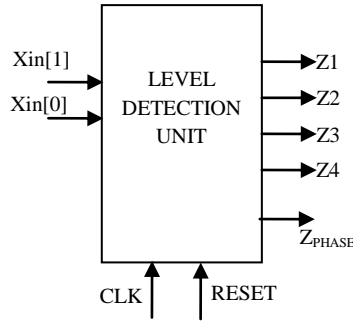


Fig 8 Level Detection Unit

Table 5 shows the level detection. For the phase identification bits shows 00 then it will give the output z1 similarly for 01, 10, 11 it gives z2, z3, z4 respectively.

Table 5 Level Detection Logic

Xin [1]	Xin [0]	Z1	Z2	Z3	Z4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig 9 shows the phase display unit where Z1, Z2, Z3 and Z4 are the inputs and phase out is the output of the phase display unit.

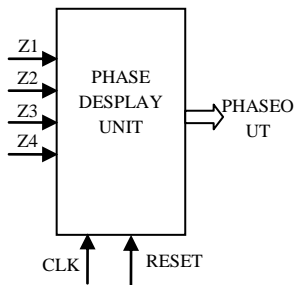


Fig 9 Phase Display Unit

Table 6 will give the phase display for the corresponding to the level detection output. For the output z1 it will give 0 similarly for z2, z3, z4 it will give 90,180,270 respectively.

Table 6 Phase Display Logic.

Z1	Z2	Z3	Z4	Phase out
1	0	0	0	0
0	1	0	0	90
0	0	1	0	180
0	0	0	1	270

Fig 10 shows the counter unit. For the counter unit Z_{phase} is the input and the count out is the output. The counter unit will give the number of phase changes among the phases.

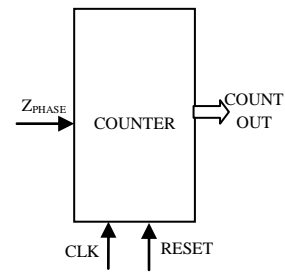


Fig 10 Counter Unit

The below table shows the logic for identifying the number of phase changes.

$$Z_{PHASE} = X_{in}(n) \oplus X_{in}(n-1) \quad (13)$$

Table 7 Number of Phase Changes Logic

Z_{phase}	COUNT OUT
1	Count=count+1b'1
0	Count=count

If $Z_{phase}=1$ then Count=count+1
 else
 $Z_{phase}=0$ then Count=count.

5. RESULTS AND DISCUSSIONS

Fig 11 gives the output for the code, amount of phase change and number of phase changes identification. The identified code enabled as logic '1'. It also gives the number of phase changes. The output will give the four phases $0^0, 90^0, 180^0, 270^0$. The count block will give the number of phase changes among the codes. The code is identified as p2 code and it is represented in Fig 11. the amount of phase change and numbers of phase changes are also shown in Fig 11.

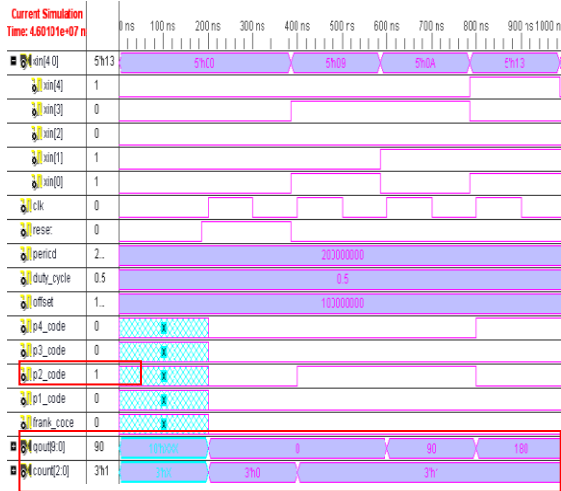


Fig 11 Simulated output waveform showing the identified code, phase angle and number of phase changes.

Fig 12 gives the photograph of the Field Programmable gate array (FPGA) results. The glowing LEDs show the logic '1' and the unglowing LEDs will give the logic '0'. The first three LED's are used for code identification and the remaining LED's are used for phase identification. The identified code is a four phase code.



Fig 12 Photograph of FPGA Showing the Identified Four phase Code along with the phase angle

6. CONCLUSIONS AND FUTURE SCOPE

An algorithm is proposed for the identification of radar codes. The proposed algorithm is able to identify the code type, amount of phase and number of phase changes also the algorithm is implemented using FPGA. Using such a system in electromagnetic wave radar will lead to a reduction on the required microwave power supplied to the radar or extending the detection range of the radar. By knowing the coded signal

parameters like code, phase, number of phase changes we can reguide and retransmit those signals to the transmitter without effecting our systems.

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