PERFORMANCE EVALUATION OF FULL ADDER AND ITS IMPACT ON RIPPLE CARRY ADDER DESIGN

Gulivindala Suresh[1], Ch. Srinivasa Rao[2]

[1]*Assistant Professor, Dept. of E.C.E, GMR Institute of Technology, RAJAM-532 127, AP, India.*
[2]*Professor & Head, Dept. of ECE, JNTU-K UCE, Vizayanagaram, A.P, India*

Abstract

Full adder is an essential module in the design and development of all types of processors such as digital signal processors (DSP), microprocessors etc. Adders are the nucleus element of composite arithmetic operations like addition, multiplication, division, exponentiation etc. The various full adders available are conventional CMOS full adder, parallel prefix adders, hybrid full adders, and mirror full adders, adders using transmission gates and multiplexer logic. The main goal is to compare the existing full adder circuit's performance and to identify a Low Power Full Adder and to analyze its impact on 8-bit, 16-bit, 32-bit ripple carry adder design. Mentor Graphics IC studio tool in 180 nm technology is used to design and implement the proposed full adders and ripple carry adders.

Keywords— *Delay; Full adder; Logic Impact; Low Power; Performance Analysis; Ripple carry adder*;

----------***----------

1. INTRODUCTION

The full adder is a basic building block of all VLSI circuits and has been undergoing a considerable improvement makes us to come out of our illusion that everything was done to the full adder. The secret behind this improvement is that the designers always targets on three basic design goals such as minimizing the transistor count, minimizing the power consumption and increasing the speed. In most of cases, the full adder is inevitably forms part of the critical path. So as a whole the full adder performance affects the system performance. A wide variety of full adders form the conventional to hybrid and in different logic styles have been reported in the literature [1]-[12].

With the same motivation, our work involves the study of various popular adder structures and explores the performance parameters such as power dissipation and delay at different power supply voltages. The adders that are considered for this work include the conventional CMOS full adder [1], 16T full adder[2], 14T FA [3], 10T FA [4], 8T FA [5], mirror adder [6], multiplexer based adder [7], transmission based adder [8], conventional D3L [9], sp-D3L all three versions as in ([10],[12]), BBL-PT full adder [11]. The Ripple carry adders (RCA) of different sizes like 8-bit, 16-bit, 32-bit are designed with the above full adders.

2. INTRODUCTION TO FULL ADDERS

The updated literature survey discloses very wide range availability of adder designs over the past few decades. The literature also reveals about several designs of low power and high speed adder cells. The conventional full adder performance is discussed in [11]. The contemporary designs include transmission gate (TGFA) [8], mirror FA [11], mux based FA [7], and spi-D3L [12] are explored. The full adder cell realization of the circuit using 16 T, 14T, 10T and 8T are available in [5].

3. PERFORMANCE ANALYSIS AND COMPARISON

The performance of a full adder circuit depends greatly on the type of design used for implementation and also on the logic function realized using the particular design style. A conventional CMOS design allows circuits to have a reasonable power delay product (PDP) but dynamic design styles gives fast design with high power consumption. Hence, an analysis and its impact on other logic functions are very much in demand. All the adder circuits described in [1]-[12] were implemented in Mentor graphics 180-nm CMOS technology process.

3.1 Power Dissipation Comparison

Table 1 shows the performance comparison of the adder circuits operated at 1V, 1.5V, 2V, 2.5V supply voltage and 1GHz measurement frequency. The table indicates the average power consumption when executing the set of all possible input combinations to the adders.

3.2 Delay Comparison

Table 2 presents the delay comparison of all the full adder circuits operated at 1V, 1.5V, 2V, 2.5V supply voltage and 1GHz measurement frequency. The delays reported correspond to the worst case delays observed in every adder.

3.3 Power Delay Product

Table 3 shows the power delay product of all the full adder circuits operated at 1V, 1.5V, 2V, 2.5V supply voltage and 1GHZ measurement frequency. The power delay product reported is multiplication of the average power consumption when executing the set of all possible input combinations to the adders and worst case delays observed in every adder.

Table 1: power dissipation comparison of full adder at different supply voltage

FA	1V	1.5V	2V	2.5V
28T	15.82	43.98	56.21	91.66
16T	13.2	31.76	50.92	85.04
14T	11.6	27.81	106.7	207.4
10T	10	22.49	39.99	62.49
8T	8.3	18	28.61	32.51
Mirror	15.82	31.76	56.21	91.66
TGFA	16.97	28.36	48.23	51.82
Spi1	37.88	78.48	142.3	236.4
Spi2	38.03	78.44	141.9	235.3
Spi3	46.88	97.42	177.1	294.5
ConD3L	19.84	40.68	73.2	120.7
Mux	13.56	23.83	31.99	49.99
BBLPT	26.17	54.75	100.1	167.0

Table 2: delay comparison of full adders at different supply voltage

FA	1V	1.5V	2V	2.5V
28T	19.84	19.88	24.07	35.35
16T	19.61	19.73	19.83	19.85
14T	19.53	19.66	19.85	21.53
10T	19.49	24.23	26.34	28.31
8T	19.30	19.40	19.60	19.70
Mirror	20.01	22.16	23.72	29.99
TGFA	49.99	51.35	54.27	55.36
Spi1	20.89	25.06	33.64	39.33
Spi2	20.18	24.22	25.01	29.99
Spi3	19.46	22.16	23.73	29.99
ConD3L	29.91	31.38	34.79	39.93
Mux	29.70	31.70	34.80	38.00
BBLPT	49.98	49.85	49.70	49.52

Table 3: power delay product comparison of full adders at different supply voltages

FA	1V	1.5V	2V	2.5V
28T	313.9	631.3	1352	3240
16T	258.8	548.6	1009	1688
14T	226.5	864.2	2117	4465
10T	194.2	544.9	1053	1769
8T	160	349	560	640
Mirror	316.0	703.8	1333	2748
TGFA	848.3	1417	2411	2590
Spi1	791.3	1967	4790	9300
Spi2	794.8	1899	3551	7059
Spi3	912.28	2158.3	4201.2	8832.9
ConD3L	593.41	1276.6	2545	4822.5
Mux	402.08	755	1113	1899
BBLPT	1308	2729	4976	8273

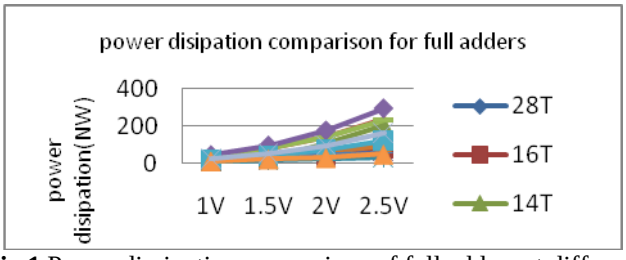

Fig 1 Power dissipation comparison of full adders at different supply voltages

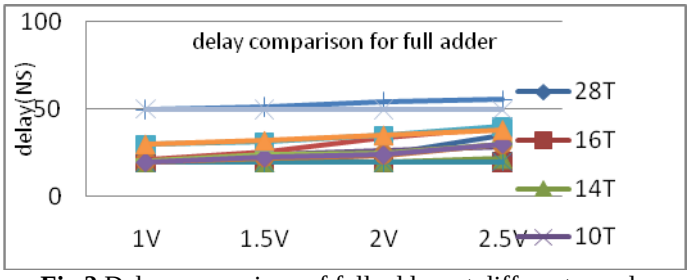

Fig 2 Delay comparison of full adders at different supply voltages

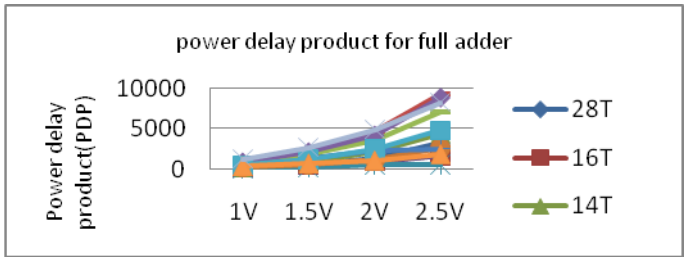

Fig 3 Power delay product (PDP) comparison of full adders at different supply voltages

4. IMPACT ON RIPPLE CARRY ADDER

Moreover, we constructed 13 different 8-bit, 16-bit, 32-bit ripple carry adders to evaluate the performance of full adders in a more realistic manner. The performance of a full adder circuit depends greatly on the type of design used for implementation and also on the logic function realized using the particular design style. a conventional CMOS design allows circuits to have a reasonable power delay product (PDP) but dynamic design styles gives fast design with high power consumption. Hence, an analysis and its impact on other logic functions are very much in demand.

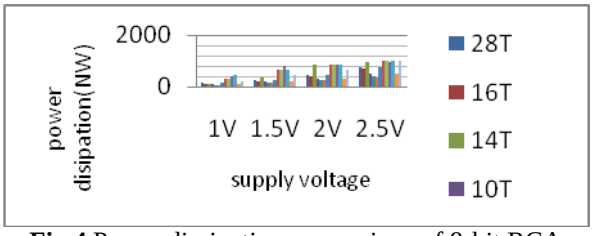

Fig 4 Power dissipation comparison of 8-bit RCA

Table 4: power dissipation comparison of 8-bit ripple carry adder at different supply voltages

FA	1V	1.5V	2V	2.5V
28T	126.6	254.1	449.7	733.2
16T	106.0	222.4	407.3	680.4
14T	92.82	351.8	853.6	953.1
10T	79.99	179.9	319.9	499.9
8T	64.00	135.8	226.8	359.5
Mirror	126.6	254.1	449.8	733.2
TGFA	74.18	144.0	255.9	399.9
Spi1	303.1	627.8	856.4	992.3
Spi2	304.0	627.5	849.2	989.8
Spi3	375.1	779.3	837.2	989.8
ConD3L	458.23	628.49	828.41	981.38
Mux	79.98	179.97	319.9	499.9
BBLPT	209.3	437.9	659.1	984.5

Table 5: delay comparison of 8-bit Ripple carry adder

FA	1V	1.5V	2V	2.5V
28T	34.53	34.71	34.76	44.50
16T	34.99	34.99	34.99	34.99
14T	34.76	34.92	34.99	34.99
10T	28.91	29.94	34.67	38.15
8T	22.51	28.19	32.41	34.76
Mirror	34.53	34.71	34.76	44.50
TGFA	34.96	34.99	34.99	34.99
Spi1	34.91	34.95	34.97	34.99
Spi2	26.05	34.93	34.93	37.02
Spi3	24.66	28.99	34.27	35.37
ConD3L	33.53	33.81	33.56	34.97
Mux	34.84	46.56	47.05	47.19
BBLPT	34.75	34.80	34.82	34.95

Table 6: power delay product comparison of 8-bit RCA

FA	1V	1.5V	2V	2.5V
28T	4371	8817	15631	32627
16T	3708	7781	14251	23807
14T	3226	12284	29867	33348
10T	2312	5386	11090	19071
8T	1440	4059	8293	13900
Mirror	4371	8819	15635	32627
TGFA	2593	4751	7935	12578
Spi1	10581	21941	29948	34720
Spi2	7919	40743	29662	36642
Spi3	9249	22591	28690	35009
ConD3L	15364	21249	27801	34318
Mux	2786	8319	15051	2359
BBLPT	7273	15238	22949	34408

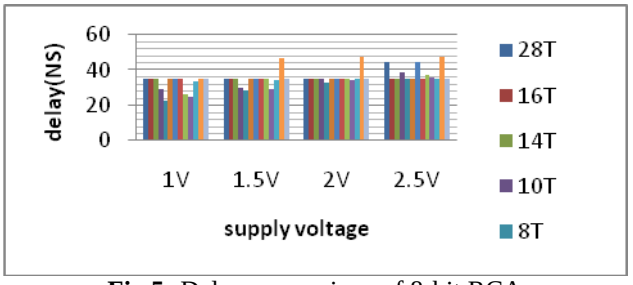

Fig 5: Delay comparison of 8-bit RCA

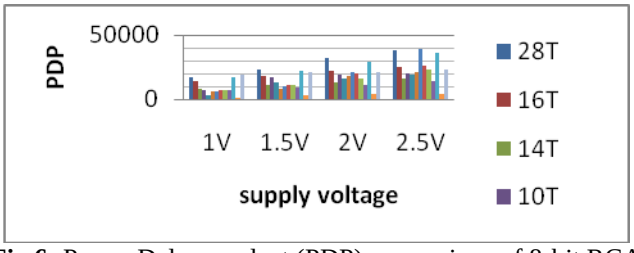

Fig 6: Power Delay product (PDP) comparison of 8-bit RCA

Table 7: power dissipation comparison of 16-bit RCA

Voltage	1V	1.5V	2V	2.5V
28T	253.2	508.2	899.5	983.5
16T	212.1	444.9	814.7	989.8
14T	185.6	703.7	873.1	998.4
10T	159.9	359.9	639.9	999.9
8T	128.0	271.6	453.7	627.2
Mirror	253.2	508.2	899.6	982.7
TGFA	148.3	287.9	511.9	799.9
Spi1	606.2	828.4	899.4	997.2
Spi2	608.0	798.1	846.8	982.1
Spi3	750.2	875.8	928.2	989.2
ConD3L	526.4	689.1	729.1	894.2
Mux	159.9	359.9	639.9	999.7
BBLPT	418.7	839.2	899.2	959.9

Table 8: delay comparison of 16-bit RCA

Voltage	1V	1.5V	2V	2.5V
28T	38.51	39.08	39.99	40.56
16T	36.24	36.98	37.28	37.99
14T	34.78	34.93	34.99	34.99
10T	30.53	32.49	32.99	34.89
8T	24.56	26.06	26.82	29.43

Mirror	34.75	34.99	34.99	34.99
TGFA	34.99	34.99	34.99	34.99
Spi1	34.94	34.95	35.01	35.92
Spi2	33.46	33.98	34.86	34.98
Spi3	26.55	28.35	28.97	33.58
ConD3L	34.04	34.76	35.29	35.99
Mux	33.54	34.36	34.67	34.71
BBLPT	34.80	34.86	34.86	43.82

Table 9: power delay product comparison of 16-bit RCA

Voltage	**1V**	**1.5V**	**2V**	**2.5V**
28T	9750	19860	35971	39890
16T	7686	16452	30372	37602
14T	6455	24615	30549	34934
10T	485	11693	21110	34886
8T	3143	7502	13729	23541
Mirror	8799	17781	31477	34384
TGFA	5189	9503	15874	21945
Spi1	21180	28952	31532	35819
Spi2	20343	27119	29519	34353
Spi3	19917	23791	26049	32233
ConD3L	17918	23953	25729	32182
Mux	5363	1236	2218	3469
BBLPT	14570	30530	32357	43784

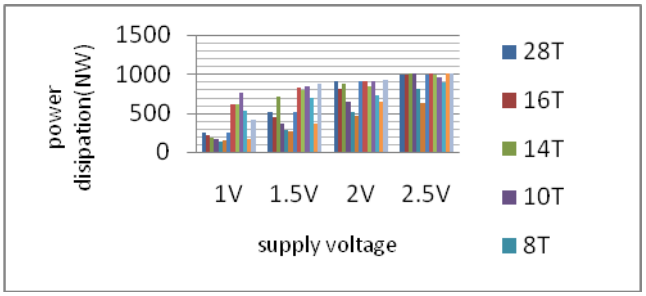

Fig 7: Power dissipation comparison of 16-bit RCA

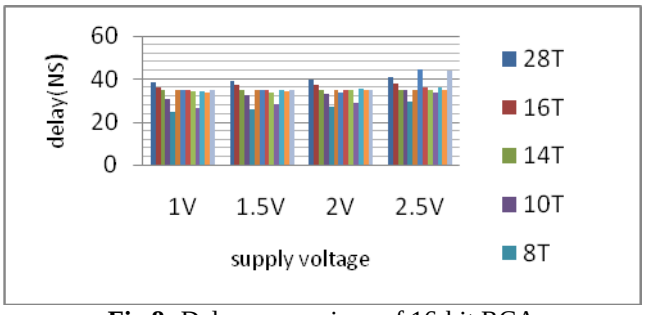

Fig 8: Delay comparison of 16-bit RCA

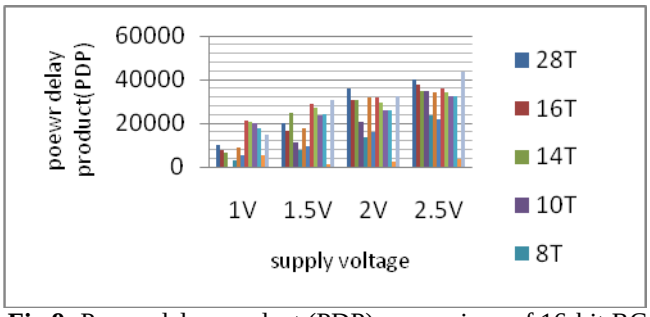

Fig 9: Power delay product (PDP) comparison of 16-bit RCA

Table 10: power dissipation comparison of 32-bit RCA

Voltage	**1V**	**1.5V**	**2V**	**2.5V**
28T	506.5	627.1	789.1	896.4
16T	424.3	520.2	643.1	729.5
14T	371.2	468.1	586.4	698.1
10T	319.9	719.8	843.1	876.3
8T	141.5	296.7	543.3	823.1
Mirror	506.5	634.1	783.2	899.1
TGFA	256.0	576.0	689.1	907.5
Spi1	689.1	753.1	853.5	984.1
Spi2	699.1	791.0	891.5	998.9
Spi3	837.5	898.1	938.1	999.1
ConD3L	453.1	589.1	792.1	983.1
Mux	319.9	719.8	893.1	998.1
BBLPT	725.1	781.6	910.1	956.8

Table 11: delay comparison of 32-bit RCA

Voltage	**1V**	**1.5V**	**2V**	**2.5V**
28T	33.79	33.97	40.04	42.49
16T	33.86	33.88	33.89	33.99
14T	22.76	22.86	22.97	22.98
10T	22.99	22.99	22.99	22.99
8T	22.77	22.78	22.94	22.94
Mirror	11.97	11.98	22.85	22.86
TGFA	22.99	33.99	38.28	42.49
Spi1	10.41	14.44	23.07	25.92
Spi2	10.08	13.73	18.28	23.51
Spi3	9.34	11.95	12.00	14.21
ConD3L	36.94	36.96	36.98	36.99
Mux	37.54	37.64	44.86	44.93
BBLPT	22.84	22.87	22.88	22.90

Table 12: power delay product comparison of 32-bit RCA

Voltage	**1V**	**1.5V**	**2V**	**2.5V**
28T	17114	22831	31595	38088
16T	14366	17624	21794	24795
14T	8448	10700	13469	16042
10T	7354	16548	19382	20146
8T	3221	13121	15704	18881

Mirror	6062	7704	17893	20553
TGFA	5885	10084	20797	38559
Spi1	7173	10874	19690	25507
Spi2	7046	10860	16296	23484
Spi3	6772	9340	10921	13596
ConD3L	16737	21773	29291	36364
Mux	1200	2660	3929	4391
BBLPT	19128	20539	21463	22879

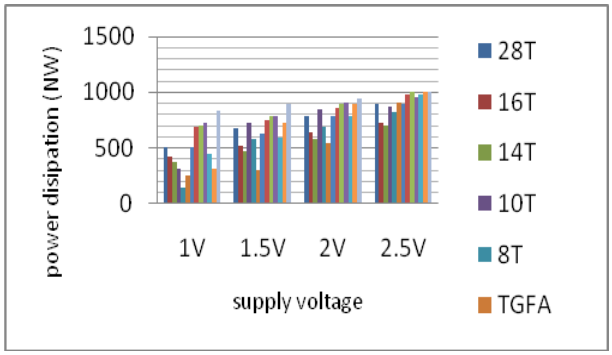

Fig 10: Power dissipation comparison of 32-bit RCA

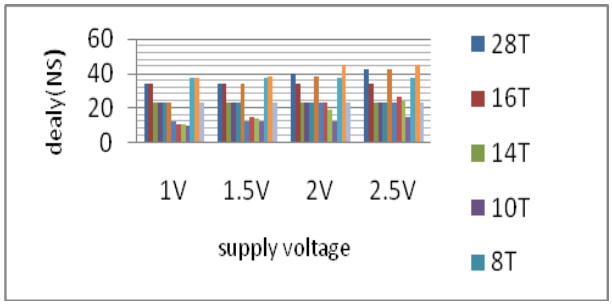

Fig 11: Delay comparison of 32-bit CA

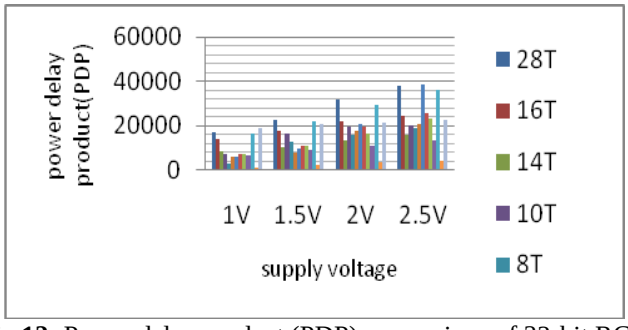

Fig 12: Power delay product (PDP) comparison of 32-bit RCA

5. PERCENTAGE OF POWER SAVING & DELAY IMPROVEMENT

From the performance tables of 8-bit, 16-bit, 32-bit RCA power saving is calculated. The table 13 below shows the percentage of power saving if the respective adder is replaced with the least power dissipating RCA. The same analysis is done to know reduction in delay as shown in Table 14.

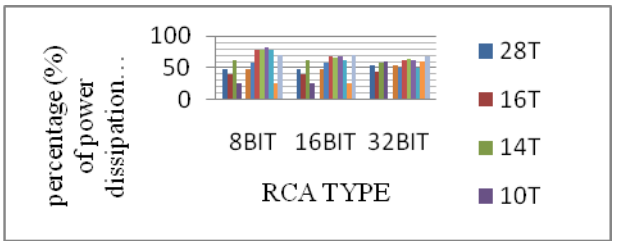

Fig 13: Percentage (%) of power saving

Table 13: percentage of power saving

FA	8BITRCA	16BITRCA	32BITRCA
28T	46.42	46.55	52.68
16T	38.93	38.95	42.96
14T	61.39	61.4	57.76
10T	24.51	24.53	58.78
Mirror	46.55	46.55	53.2
TGFA	56.94	56.61	48.48
Spi1	77.06	67.21	60.6
Spi2	78.35	65.96	62.49
Spi3	82.57	67.63	62.03
ConD3L	78.39	60.58	49.63
Mux	24.54	24.53	58.78
BBLPT	68.98	68.98	66.96

Table 14: percentage of delay saving

FA	8BITRCA	16BITRCA	32BITRC
28T	18.78	33.31	64.82
16T	19.43	29.52	64.72
14T	19.27	25.39	47.72
10T	5.84	5.84	48.02
8T	0	0	47.54
Mirror	18.78	18.78	0.25
TGFA	19.43	19.43	64.84
Spi1	19.34	19.34	17.24
Spi2	19.29	19.29	12.96
Spi3	2.75	2.75	0
ConD3L	16.62	16.62	67.66
Mux	39.45	39.45	68.25
BBLPT	18.99	18.99	47.74

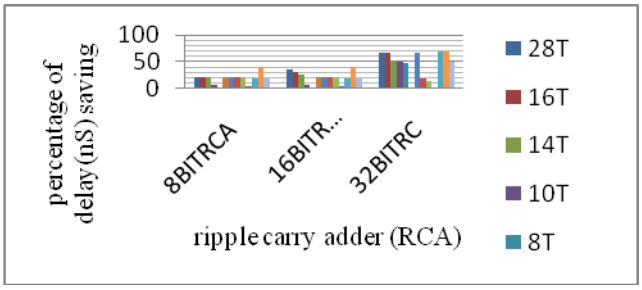

Fig 14: Percentage (%) of delay saving

6. CONCLUSIONS

Based on the performance analysis one can easily identify a low power dissipating Full Adder, 8-bit Ripple Carry Adder, 16-bit Ripple Carry Adder, 32-bit Ripple Carry Adder and as well percentage of power saving from the tables. Hence one can choose 32-bit Ripple Carry Adder of spi-3 implementation for better speed and the least power dissipating Ripple Carry Adder is 8T model irrespective of the number of stages.

REFERENCES

[1] F. Frustaci, M. Lanuzza, P. Zicari, S. Perri, and P. Corsonello, "Low power split-path data driven dynamic logic," *IET Circuits, Devices, Syst.*, vol. 3, no. 6, pp. 303–312, 2009.

[2] H.Eriksson, P.L.Edefors, T.Henriksson, C.Svensson, "Full Custom Versus Standard Cell Design flow: an adder case study" in Proceedings of 2003Asia and South Pacific Design Automation Conference, 2003, pp.507-510.

[3] H.T.Bui, Y.Wang, and Y.Jiang, "Design and Analysis of Low Power 10 transistor Full Adders using XOR/XNOR gates" IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, Vol.49, no.1, Jan. 2002, pp.25-30.

[4] I.Hassoune, A.Neve, J.Legat, and D.Flandre, "Investigation of Low Power Circuit Techniques for a Hybrid Full Adder cell" in Proc. PATMOS, 2004, pp.189-197, Springer-Verlag.

[5] M.Hossein, R.F.Mirzaee, K.Navi and K.Nikoubin, "New High Peerformance Majority function based full adder" 14th International CSI conference 2009, pp.100-104.

[6] N. Weste and K. Eshragian, *Principles of CMOS VLSI Design: A Systems Perspective*, 2nd ed. Boston, MA: Addison Wesley, 1993.

[7] Pardeep Kumar "Existing full adders and their comparision on the basis of simulation result and to design a improved LPFA (Low Power Full Adder)", International Journal of Engineering Research and Applications, ISSN:2248-9622, 2012, Vol.2, Issue-6, pp.599-606.

[8] Sohan Purohit, Martin MArgala "Investigating the impact of logic and circuit Implementation on Full Adder Performance", IEEE Transactions on VLSI Systems, Vol.20, No.7, July 2012, pp-1327-1331.

[9] T.Sharma, K.G.Sharma, B.P.Singh, "High Performance Full adder cell: A Comparative Analysis" in Proceedings of the 2010 IEEE Students' Technology Symposium, 3-4 April, 2010,pp.156-160.

[10] T.Vigneswaran, B.Mukundhan, P.Subbarami Reddy, "A Novel Low Power and High-Speed Performance 14 Transistor CMOS Full adder cell" Journal of Applied Science, 6(9); 1978-1981, 2006.

[11] W. R. Rafati, S. M. Fakhraie, and K. C. Smith, "Low-power data-driven dynamic logic (D3L)," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*,2000, pp. 752–755.

[12] Y. Jiang, A. Al-Sheraidah, Y. Wang, E. Sha, and J. Chung, "A novel multiplexer based lowpower full adder cell," *IEEE Trans. Circuits Syst.II, Exp. Briefs*, vol. 51, no. 7, pp. 345–348, Jul. 2004.