DESIGN OF LOW POWER HIGH SPEED LEVEL SHIFTER

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Abstract

The leakage power consumption increases with the scaling of the devices and it is expected that the leakage power consumption is important design constraint of total power consumption. In this proposed work, a new configuration of level shifter for low power high speed application has been presented. The proposed circuit have no cross coupled connection, by which there will be reduction in delay. In this work a new level shifter design has introduced at an ultra low core voltage and has wide range of Input/output voltage. This Low power high speed level shifter allows wide Input/output interface voltage applications in CMOS Technology. On an average it shows an improvement of 8% on average power consumption and 77.2% on delay compared with conventional level shifter with a little bit area overhead.

Keywords - *Average Power consumption, scaling, level shifter, Transmission gate, level shifter, I/O interface.*

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1. INTRODUCTION

The shrinkage in size and addition of more function on digital integrated circuits [5] has given rise to large power dissipation per unit area. The power consumption of IC is one of the most important design constraints out of area and speed. Power consumption in VLSI circuit includes dynamic, static power and leakage power consumption [7]. Dynamic power consumption results from switching of load capacitance between two different voltages and dependent on frequency of operation. Whereas static power is contributed by direct short circuit paths between supply (VDD) and ground (VSS). Leakage power results from leakage currents that arise from substrate injection and sub-threshold hence more attention can paid on leakage power reduction. Power consumption can be reduced by scaling supply voltage, but the problems like small voltage swing, insufficient noise margin and leakage currents start to originate with the power supply voltage scaling[4],[5] and The speed or delay depends on circuit topology. In view of handheld and portable devices the power consumption has become most important design constraint for VLSI circuit designers as the battery back point of view. With increase in power consumption, reliability problem also rises and cost of packaging goes high [7]. Level shifters are I/O interface devices [1] and Leakage power depends on the total number of transistors and their operating condition in spite of their switching activity. And total leakage power of any circuit is given by

$$P_{Leakage} = \sum P(MP1 + MP2 + MP3 + - - - MPn) + P(MN1 + MN2 + MN3 + - - - MNn) \quad (1)$$

Where –MP1, MP2, - - - MPn are the no. of PMOS transistors, and MN1, MN2, - - - MNn are the no. of PMOS transistors.

The leakage power of CMOS circuits is determined by the leakage current [12], [13] when the input voltage is less than threshold voltage and transistor is off state (standby mode) but there is leakage of current from Drain to ground. With the development of technology leakage power has become significant component of total power dissipation [8], [9]. Most of the given power is consumed during operation in the form of leakage. This is surely a big obstacle in integration process. So leakage power component must be given as a major design constraint if present trends of scaling to be achieve.

2. CONVENTIONAL LEVEL SHIFTER

Level shifter is an interfacing circuit which can interface low core voltage to high input-output voltage [2],[3],[6]. The level shifter allows communication between different modules without adding up any extra supply pin. The conventional level shifter using cross-coupled PMOS load[1] is shown in Fig.1.The cross-coupled two PMOSs in pull up provide positive feedback action which results full VDD at output node. The conventional level shifters have drawback of delay variation due to cross-coupled connection and different current driving capabilities of transistors, large power dissipation and failure at low supply core voltage [4].A very important phenomena in integration process is sub threshold current. Sub threshold current is the drain-source current when the gate-source voltage is under the transistor threshold voltage. MOS transistor models predict that when gate-source voltage is at just threshold voltage or below the threshold voltage the transistor does not conduct and there should be is no current flow ideally but practically there is leakage of current [13] will constitute the power called leakage power[11] can it be called as wastage power.

This leakage is continuous and we cannot avoid it but by using suitable leakage minimizing circuit we can minimize this. Circuit diagram of conventional level shifter is shown in fig 1. If we have logic 0 at input terminal then MN1 and MN4 are in saturation region and MP1 and MP4 are in cut-off region. This will cause VDD at output node, so by using level shifter we can interface low core voltage to high output voltage, but during this operation the Leakage power dissipation occurs in MP1 and MN2 i.e. there is continuous flow of current from VDD to ground, and this cross-coupling will produce more delay. The delay and average power dissipation of existing level shifter can be viewed in Fig. 4 and 6.We should adopt a technology to reduce this delay. For this we have to adopt different technology like transmission gate based circuit instead of cross-coupled or DCVSL.

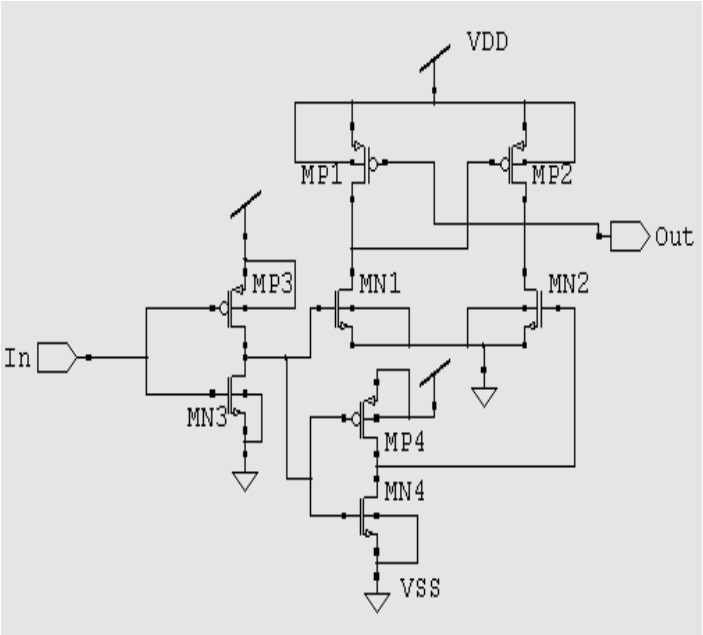

Fig. 1 conventional level shifter

3. PROPOSED LEVEL SHIFTER

The proposed design is totally different from the conventional designs. The conventional designs are based on current mirrors but the proposed design is based on multiplexer. So the proposed level shifter is a combinational circuit. The pair of transistors MP1-MN1, MP2-MN2 and MP5-MN5 forms inverters. The pair of transistors MP3-MN3 and MP4-MN4 forms transmission gates. The combination of transmission gates and MP1-MN1 inverter forms the multiplexer. The input for the multiplexer is the output of the MP2-MN2 inverter. The output of the multiplexer is given as input to the MP5-MN5 inverter. The input to the level shifter is B given as input to the MP2-MN2 inverter. The output of the MP5-MN5 inverter is Vout1 and it is the output of the level shifter. The supply voltage VDD is 1 and the input for A is always 1V.

The principal part of the design is operation of transistors MP3, MP4, MN3 and MN4. Here MP3 and MP4 are always in ON state while MP4 and MN4 are always in OFF state. If the input of the level shifter in is low MP2 conducts and wire2 becomes high. The transmission gate MP3-MN3 always in ON state, so wire2 logic is transmitted to the input of the MP5-MN5 inverter and the output of the inverter out becomes low. So the output of the level shifter is low. If the input of the level shifter in is high MN2 conducts and wire2 becomes low. The transmission gate MP3-MN3 always in ON state, so wire2 logic is transmitted to the input of the MP5-MN5 inverter and the output of the inverter out becomes high. So the output of the level shifter is high.

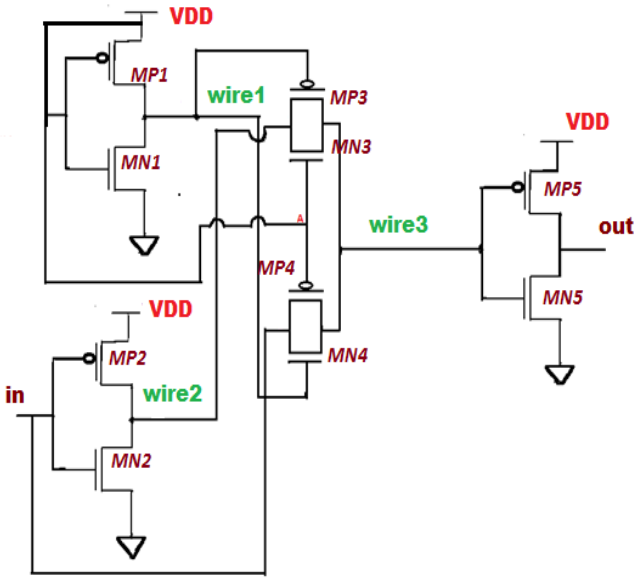

Fig.2 Proposed level shifter

4. SIMULATION RESULTS

Simulation of any design facilitates verification of overall system level operation. The schematic of level shifter is built using Tanner S edit schematic editor and the circuit is simulated using Hspice simulator and CosmosScope W edit. The simulation is performed using the 45nm model files. The basic operation of the proposed level shifter circuit is shown in Fig.2. The Fig. 3 shows the voltages at input and output. The input rise and fall times are set to 10 ns, and a load capacitance of 100 fF. The proposed level shifter consumes 4.48 nW of average power (Figure 5) whereas it is 5.40 nW in conventional method (Figure 4), and 4.21nSec delay(Figure 7) and it is at 18.4nSec in conventional method, refer figure 6.The VLSI constraints like delay, power consumption and area of both conventional and investigated level shifters are summarized in the table 1.

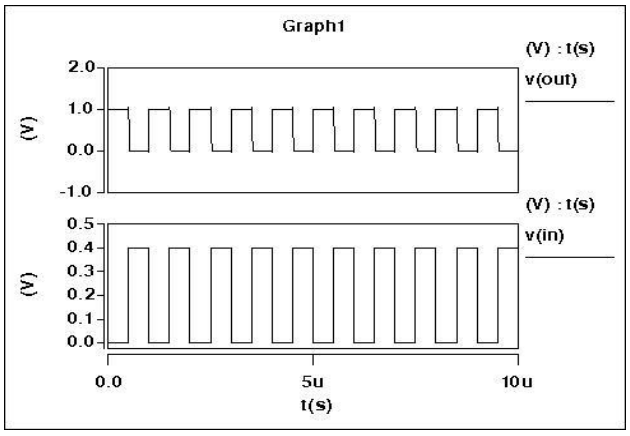

Fig: 3 Proposed Level shifting input and output

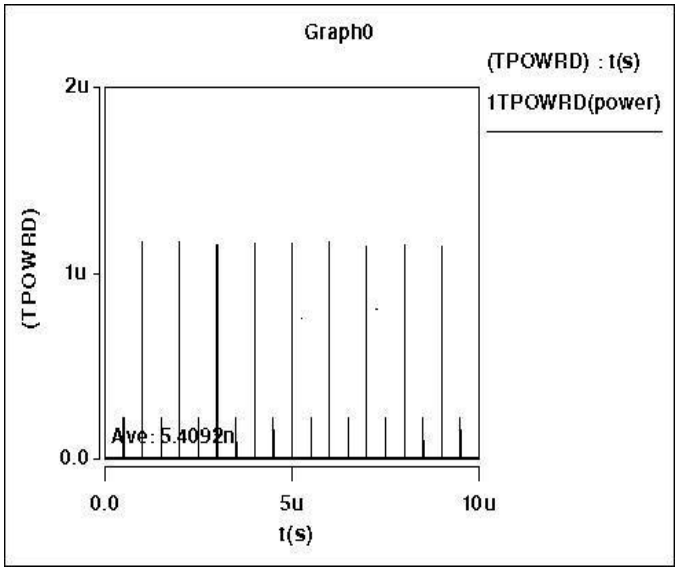

Fig: 4 Average Power consumption conventional method

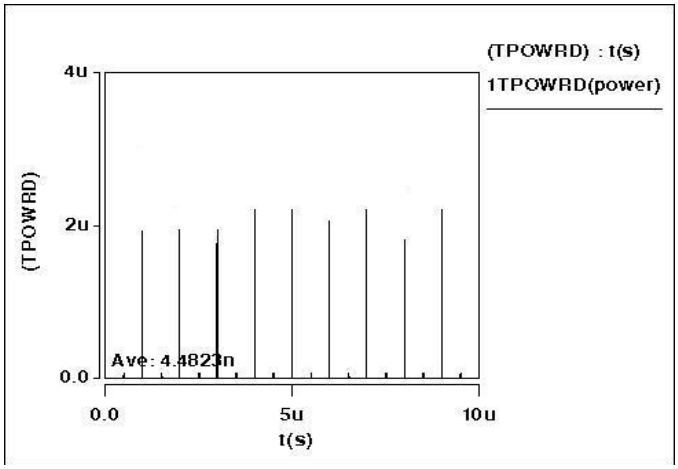

Fig: 5 Average power consumption Proposed method

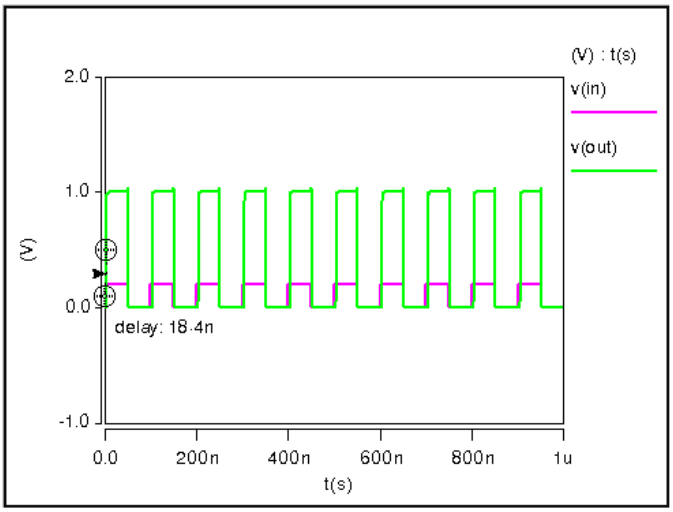

Fig.6: Delay of conventional level shifter

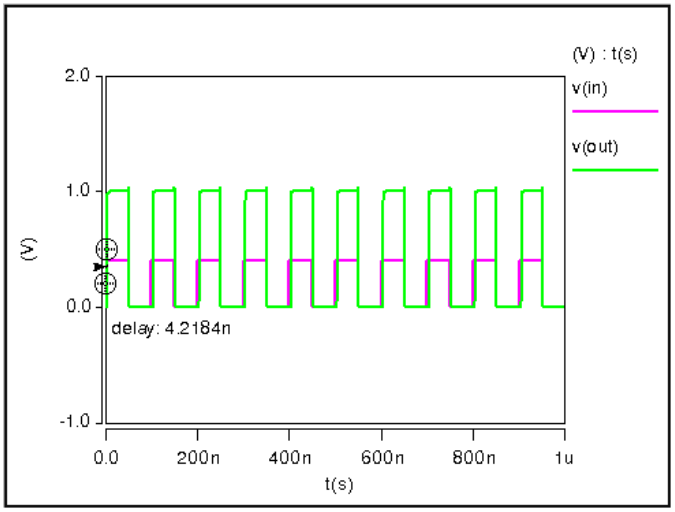

Fig.7: Delay of proposed level shifter

Table 1

Constraints	Conventional	Proposed
Ave. Power consumed	5.40nW	4.48nW
Delay	18.4nSec	4.21nSec
No. Of transistors	08	10

5. CONCLUSIONS

The simulation results of the level shifter in a 45nm process Technology show that this circuit topology offers good performance and low power dissipation. The proposed design exhibits lower delay with low power consumption with respect to conventional Level Shifters that use similar design parameters. The proposed level shifter circuit operates properly and output level of 1.1V has been obtained with input pulse of 0.4V. It is designed using a 45nm CMOS process in

HSPICE tool. The novel level shifter has a average power dissipation of 4.48nW and propagation delay of 4.21 ns. On an average it shows an improvement of 8% on average power consumption and 77.2% on delay compared with conventional level shifter and it has negligible static power consumption. This high-speed performance and stable duty ratio make this level shifter suitable for wide I/O interface voltage applications in ultra-deep sub-micron.

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