IMPLEMENTATION OF GPS SIGNAL ACQUISITION AND TRACKING IN FPGA

G.Kavya[1], V.ThulasiBai[2]

[1]*Research Scholar, Sathyabama University, Assistant Professor, Prathyusha Institute of Technology and Management, Thiruvallur, Chennai, India*

[2]*Dean (R&D), Prathyusha Institute of Technology and Management, Thiruvallur, Chennai, India*

Abstract

GPS Receivers are used for both military and civilian applications. This paper presents the GPS Receiver for System on Chip (SoC) application. In this paper the GPS Receiver is been implemented as System on Chip in FPGA board. VHDL modeling for the back end of GPS Receiver is designed. As baseband signal processing is the main aspect in the GPS receiver, it is achieved by this software GPS Receiver. Here the acquisition and tracking of the GPS signals is been designed and the data is recovered. MODEL SIM simulator is used here to validate the VHDL modeling. Hence the software defined GPS Receiver is simulated and implemented in FPGA for navigation purpose along with an analog front end.

Key Words: *Acquisition, GPS, FPGA, MODEL SIM, SoC, Tracking, VHDL*

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1. INTRODUCTION

GPS satellites broadcast the signals in the same frequencies using direct sequence spread spectrum (DSSS) but use different ranging codes with low cross correlation properties. The satellites that broadcast the signals consist of CDMA ranging codes(to determine the propagation time),navigation data (to provide the satellite position), and transmission time. These ranging codes and navigation data are modulated with the carrier signal using Binary Phase Shift Keying (BPSK).

The ranging codes broadcasted by the GPS satellites are C/A codes (coarse acquisition code) and P(Y) code (military code). The C/A code signal frequency is 1.023 MHz and carrier frequency [L1] is 1575.42 MHz In this paper as the GPS Receiver is used for civilian purpose, only C/A codes are considered, as P(Y) codes are used for military application.

The overall block diagram of this paper is shown in fig 1. The right hand circular polarization antenna is used to receive the signals from GPS satellites. RF front end is used to convert the signal frequency into intermediate frequency (IF).The intermediate frequency is much lower so that it can be sampled by ADC. The IF signals is given as input to the software GPS receiver.

The Global Positioning System (GPS) is provided as a System on Chip (SoC) inside a FPGA using VHDL implementation. The output of the GPS receiver is in NMEA format, which is displayed in the LCD screen used in the board.

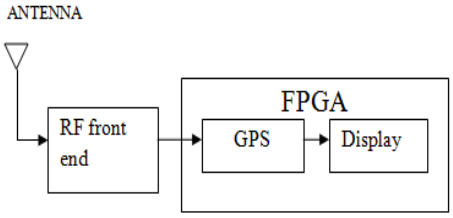

Fig -1: Basic Block diagram

This paper deals with the implementation of software GPS Receiver using VHDL. Section I deals with the basic block diagram of this paper. Section II deals with the important definitions and terms used in the paper. Section III discusses about the system architecture which explains the function of GPS Receiver. Section IV discusses the analog front end which is used to convert the RF signal into IF signal. Section V discusses about the acquisition of the signal. Section VI discusses about tracking the acquired signal .Section VII discusses about the data recovery. Section VIII discusses the FPGA implementation and section IX shows the experimental results and its discussion.

2. TERMS AND DEFINITIONS

The following terms are vital to understand the operation of the GPS receiver.

2.1 C/A Code

The coarse acquisition code is provided by the GPS satellites. It is generated as a sequence of 1023 chips. This code is repeated every milli second with chipping rate of 1.023 MHz and modulated only in L1 frequency.

2.2 Doppler Effect

Doppler Effect is a type of error where the Doppler frequency shift occurs because of the radiative motion from transmitter and receiver. it affects both acquisition and tracking of the signal. It is the change in carrier frequency.

2.3 C. PRN code

PRN code is abbreviated as pseudo random noise which is determined for 32 satellites. This code determines the C/A code replica of different 1023 chips using a shift register. it is compared with the satellite code using correlator.

2.4 Ephemeris Data

It is the precise information needed for a GPS receiver to calculate the exact position (of the satellite) in the sky.

2.5 Almanac Data

Information about the change in satellite over the orbit is provided by this almanac data.

3. SYSTEM ARCHITECTURE

The system architecture of the software GPS receiver implemented in FPGA along with a hardware analog front end is shown in figure 2

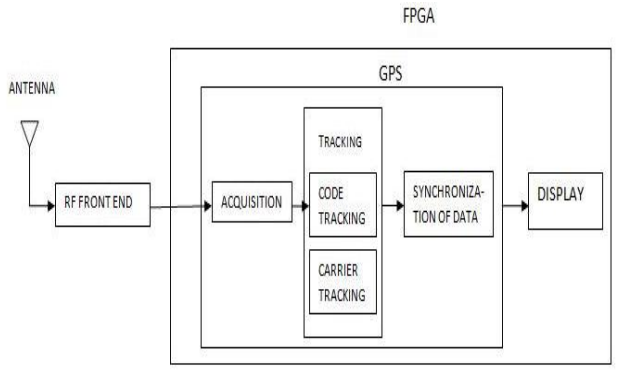

Fig 2 System architecture of SoC GPS receiver

The main aspects performed by the GPS receiver are

1. Acquisition
2. Tracking
3. Data processing

Acquisition is a coarse synchronization process used to acquire the signal for removing code phase and Doppler Effect. Tracking is the next step carried out to remove code and carrier frequency, this is a fine synchronization process. At last data processing is done to recovery the GPS data. The output of the GPS is displayed in LCD screen provided in FPGA.

4. ANALOG FRONT END

In the normal design process for a software GPS receiver inside a FPGA, some care is needed to integrate the FPGA and the RF components. The incoming GPS signal is of the order of 160dBW which can easily be disturbed by the radiated harmonics found in digital area of the receiver. Normally when the RF front end chips interface with the baseband processing FPGA, it leads to interference problems.

In this paper Zarlink GP2015 RF front end chip is used, this RF front end chip is connected to general purpose FPGA by minimizing the risk of interference to the GPS signals [2]. In order to provide minimum noise in spread spectrum application like GPS, Low noise Amplifier (LNA) is used. The LNA used in this paper is Agilent MGA 87563 which mainly used for its availability and low minimum order quantity.

5. ACQUISITION

Acquisition is the process by which the receiver determines the satellites are in view such that it can track them and begin to navigate. To track the transmitted signal, the receiver must remove the carrier frequency and C/A code. It is used to identify the satellites for the users and determine the coarse values of the carrier frequency and the code phase of the signal.

As discussed in section I all satellites transmit the C/A code with carrier frequency equal to GPS L1 frequency. The receiver does not receive the signal exactly modulated by L1 frequency [1], but receive the signal which is slightly shifted due to Doppler Effect. Hence in order to demodulate the signal and to remove the carrier frequency, the receiver must determine the Doppler shift of the satellite.

There are three standard methods of acquisition: serial search acquisition, parallel frequency space search acquisition, and parallel code phase search acquisition.

The goal of acquisition is to perform a correlation with the incoming signal and a PRN code. Here the PRN code is generated using the linear feedback shift registers(LFSR).

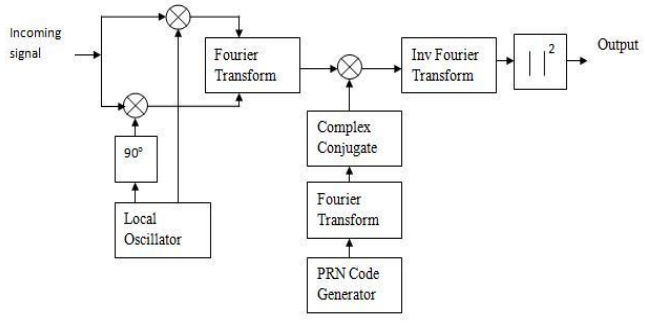

Fig -3: Block Diagram of Parallel Code Phase Search Algorithm

Compared to the three methods, the parallel code phase search acquisition method reduces the search space to only the possible carrier frequencies. The accuracy of the carrier frequency is similar to the serial search method but the code phase is more accurate as it gives a correlation value for each sampled code phase.

6. TRACKING

Satellites constantly move in the orbit. Hence the distance between the transmitter and receiver vary a lot. Hence once if the signal is acquired, the tracking must be started by synchronization method of locally generated carrier and locally generated code Two types of tracking methods are

1) Code tracking
2) Carrier tracking

The tracking is running continuously to follow the changes in frequency as a function of time. If the receiver loses track of a satellite, a new acquisition must be performed for that particular satellite.

6.1 Code Tracking:

Code tracking is the process of advancing or delaying the local replica code. Early code, Late code, Prompt code are the three replica been generated. These three types of code are compared with the transmitted signal.

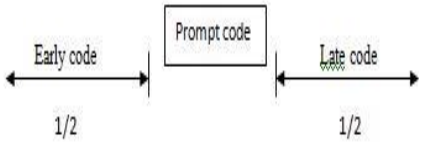

Fig – 4: Replica codes

The code must be half of the chip distance from prompt code such that if the early or late code is increased than the incoming code then it correlates with other PRN chip, hence error occurs. Code tracking method is thus done using Delay Locked Loop(DLL).

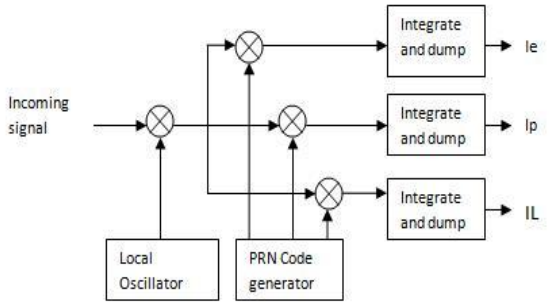

Fig - 5: Code tracking loop

The code tracking method is to generate an exact code replica and it is correlated with the incoming signal. In figure 5 it shows that the incoming signal is multiplied with the local replica carrier wave. After that the signal is multiplied by three replica codes. After this second multiplication, the three outputs are integrated and dumped giving a numerical value indicating how much the specific code replica correlates with the code of the incoming signal.

6.1.2 Carrier Tracking:

To demodulate the navigation data successfully, an exact carrier wave replica has to be generated. To track a carrier wave signal, phase lock loops (PLL) or frequency lock loop (FLL) are often used. The problem with using an ordinary PLL is that it is sensitive to a 180° phase shift of the input signal carrier wave. Due to navigation bit transitions, the PLL used in a GPS receiver has to be insensitive to 180° phase shifts.

Figure 6 shows the Costas loop for carrier tracking process. Costas loop is insensitive to 180° phase shifts. Hence both frequency and phase offset are removed by this tracking loop.

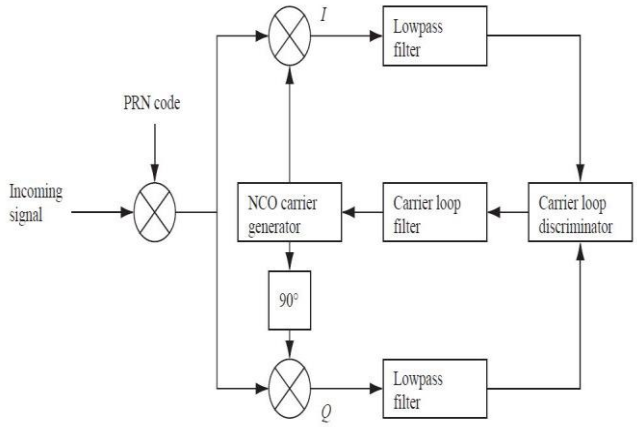

Fig – 6: Costas loop used to track the Carrier wave

7. DATA PROCESSING FOR POSITION

After removing carrier and PRN code (gold codes) the remaining bits are given as data. The data is divided into frames. An entire frame is transmitted within 30 seconds. The data's are been encoded as ± 1. The GPS data structure is shown in figure 7. Each sub frame starts with 30-bit telemetry word (TLM). The TLM word consists of 22 preamble bits it is followed by telemetry message and ended up with parity bits.The receiver considers the preamble data to determine the start of sub frame. Sub frame provides the ephemeris data (satellite orbital position), satellite constellation information, atmospheric modeling parameters (for correcting positioning errors) and almanac data of long term coarse satellite orbital parameters. From the data output the following results which are obtained are:

1. Data receiver gets its date information.
2. Approximate time is provided.
3. Position of satellites is determined.

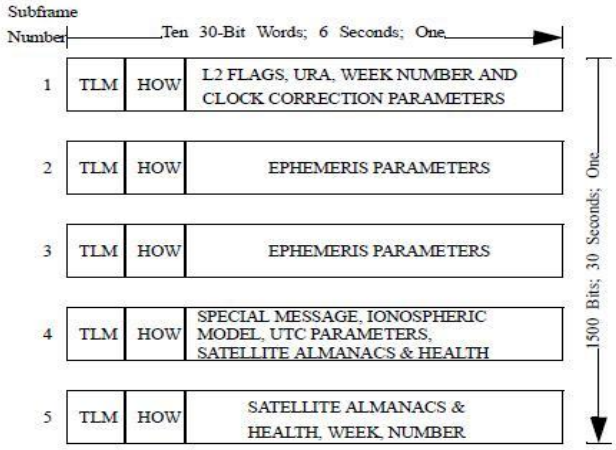

Fig- 7: GPS navigation message data frame structure

8. FPGA

Altera DE0 Nano Board is used in this paper for implementing the software GPS receiver along with analog front end. Figure 8 depicts the photograph of FPGA board. 40 pin GPIO header is used to place the LCD screen through which GPS data output is displayed. The DE0 Nano development board is perfect for implementing GPS receiver inside the Nios II processor. A NiosII soft-core processor residing in the FPGA chip hosts the application software that interfaces with the user and controls the custom logic[14].

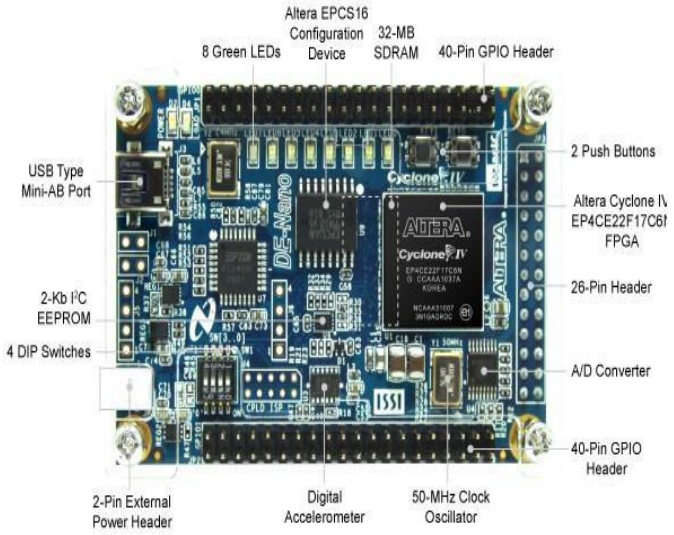

Fig.-8: Altera DE0 Nano Board

9. EXPERIMENTAL RESULTS

9.1 Acquisition Output

The acquisition output for removing the code phase and Doppler Effect is developed and simulated output is given in figure 9.

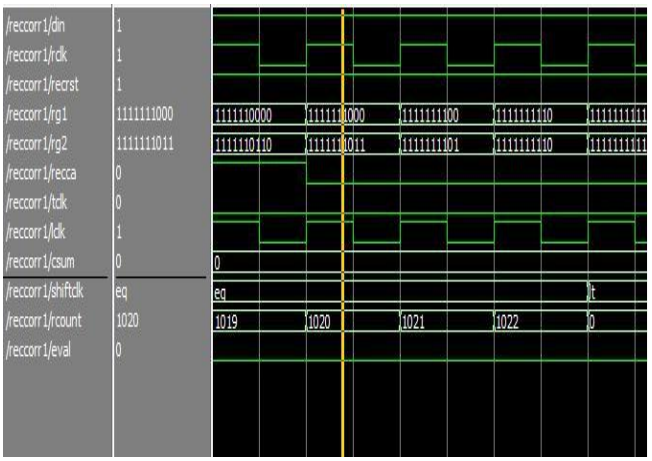

Fig – 9: Acquisition output

9.2 Tracking Output

The acquisition output is given as input to the tracking process for fine synchronization process. The tracking process is developed and simulated output is provided which is shown in figure 10.

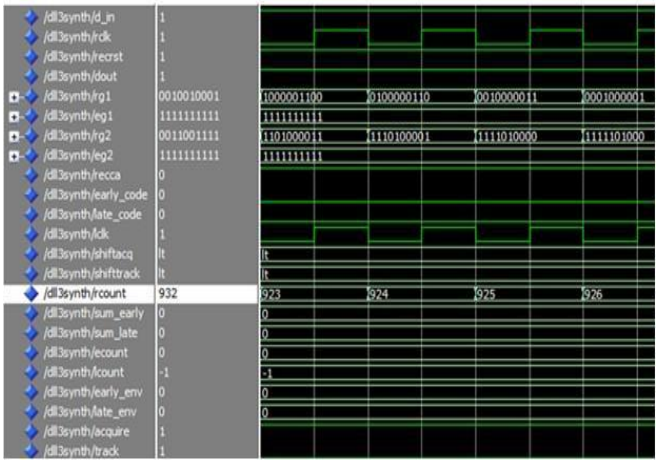

Fig -10: Tracking output

9.3 Data Output

The data is been recovered after removing the code and carrier frequency. The overall simulated output is shown in figure 11.

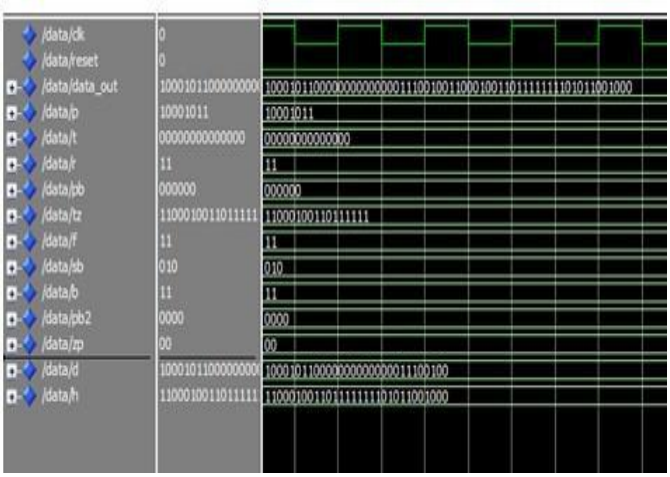

Fig -11: Data Output

10. CONCLUSIONS

This paper outlined the implementation of a GPS receiver. It dealt with VHDL implementation of the digital backend of a GPS receiver. Different functional blocks and communication blocks were implemented as part of this paper. The scope of this paper is to develop a working code acquiring and tracking module, capable of acquiring a GPS signal and tracking it. Synthetic data was generated at the required rate. MODEL SIM simulator is used to simulate the software GPS receiver.

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