MULTI BAND, MULTI MODE DIGITAL RF RECEIVER FRONT-END MODULE FOR M-WIMAX

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Abstract

A digital RF receiver front-end employing a DT filter is proposed for application to m-WiMAX & The SAW-less receiver architecture, where the large out-of-band interferer can be rejected selectively by using a scalable frequency response property of FIR filter. In addition to the flexibility of the DT filter, the new non-decimation finite impulse response (NDF) filter can be cascaded to a conventional FIR filter without the decimation effect. Thus, we can easily increase the order of the function-type filtering response and the signal processing bandwidth and the designed receiver front-end is implemented using an IBM 130- nm RF CMOS process. The fabricated chip satisfies the m-WiMAX specification of an 8.75 MHz channel bandwidth and the total system power consumption is 26.63 mA from a 1.5-V supply voltage. The chip shows unwanted blocker rejection over 80 dB, with good linearity of +3.94 dB IIP3.

Keywords: *Radio Frequency (RF), discrete time filter (DT), Finite Impulse Response (FIR), and Non Decimation Filter (NDF) etc…*

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1. INTRODUCTION

As the number of wireless communication standard grows rapidly, the demand for mobile radio receivers is also increasing. In order to process various wireless standards, several single chip solutions which provide multimode/multi-band operation have been proposed recently [1]. The digital RF concept, which involves processing the signal in the discrete-time and the charge domain, has become a useful technique in the development of SDR or reconfigurable RF [6]–[14]. The elimination of the SAW filter makes it possible for the receiver system to operate with wide frequency bands. Without the SAW filter, however, in-band signals may be disturbed by large out-of- band interferers. What is even worse is the receiver may be saturated by these signals. Consequently, a method for rejecting out-of-band interferer near the in-band signal is needed. In order to reject arbitrary interferer, the switched-capacitor based FIR filters have been actively researched. The filtering response can be flexibly adjusted using the control of clock signals to prevent aliasing due to the analog-to-digital converter (ADC) sampling operation. The DT filter, which employs a switched-capacitor circuit has a function filtering response with a limited bandwidth and its applications are limited to narrowband wireless communication standards [6], [7].

To overcome the bandwidth problem, we have proposed a non-decimation finite impulse response (NDF) filter. The NDF filter has the moving average characteristic, but without the decimation effect. This characteristic enables the NDF filter to be cascaded with another DT filter and allows us to increase the order of the function-type filtering response. The clock generator is an important block in the digital RF receiver front-end. To generate the complicated clock signals required for the DT filter, a complex and large-sized clock generator is needed. The finite impulse response (FIR) filter con- figuration has been modified to reduce the number of required clock signal and to improve the noise performance of the filter chain. The NDF filter has also been designed to share the same clock signal with the FIR filter. Through this optimization, the clock generator can be simplified, reducing the chip area and the noise figure [15].

2. RECEIVER ARCHITECTURE

The proposed digital RF receiver architecture is shown in Fig-1. The signal received by an antenna passes through low noise amplifier (LNA) and is amplified. The amplified voltage signal is fed to the Trans conductor amplifier stage and converted to the current domain. The current-commutating passive mixer down converts the current domain signal to baseband and generates the differential I and Q quadrature signals. The current then flows into the FIR filter stage. The low-pass type FIR filters are based on the switched-capacitor circuits. The FIR filter response presents notch frequency controlled by the sampling frequency of the filter, so the unwanted out-of-band interferer can be rejected. The new NDF filter to increase the order of the sinc function filtering response through cascading

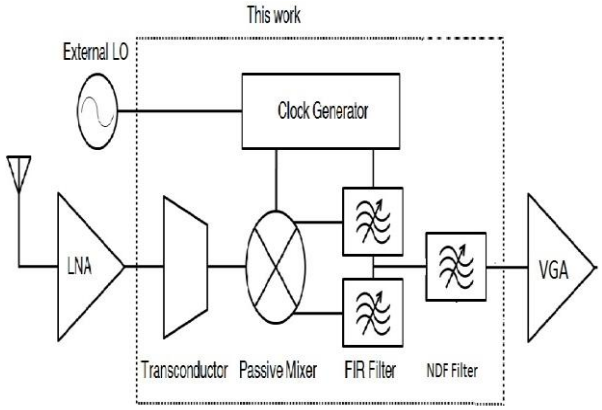

Fig-1: Receiver Architecture

Each filter block of our RF receiver front-end contains a cascaded NDF filter and FIR filter [17]. The filtered signal is amplified by the variable gain amplifier (VGA) and finally sampled by the ADC, converted to the digital domain without any aliasing problem. The clock generator, which is circuit fed with external LO, supplies the LO signal to the mixer and the operating clock signal to the FIR filter.

3. CIRCUIT IMPLEMENTATION

3.1 Transconductor and Passive Mixer

Followed by an LNA, the Transconductor stage converts the input voltage to current domain. By employing a simple inverter-based structure with a self-biasing resistor, the transconductor in Fig-2a can convert both the input in-band signal and the out-of-band interferer linearly.

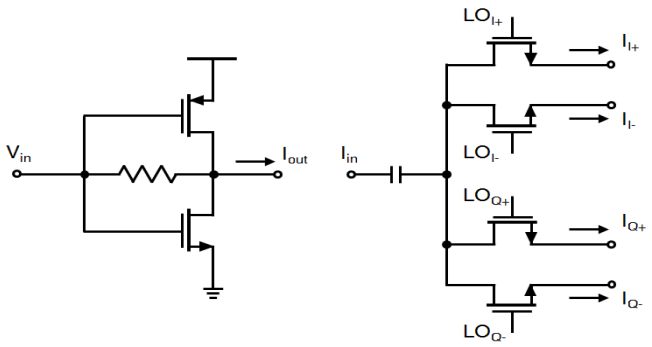

Fig-2a: Trans Conductor **Fig-2b:** Passive Mixer

The current-commutating passive mixer in Fig-2b down converts the RF signal to the baseband. This mixer consists of four nMOS transistors operating as switches, which is turned on and off by four-phase clock generator signal. Using this zero-IF passive mixer, down conversion can be done with high linearity.

3.2 Current-Mode FIR Filter

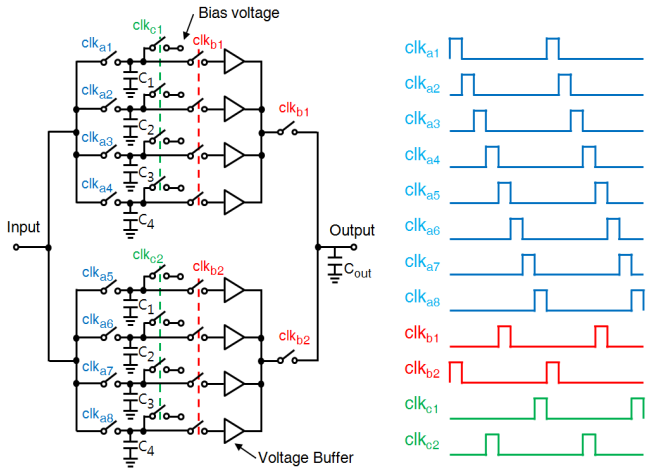

Fig-3: Current Mode Fir Filter

The differential I and Q baseband signals from mixer are filtered in the current-mode FIR filter stage. Unlike the other FIR filter structure; this proposed FIR filter operates in current domain. To compare the structure of the two filters, the conventional filter is checked firstly. Conventional FIR filters operating in voltage domain use a charge sharing method for filtering. When the input voltage is sampled by the switched-capacitor pair, the charge sharing operation produces the output voltage in *Cout*.

In contrast, the current mode FIR filter shown in Fig-3 operates differently. In other words, the voltage mode filter generates charges on each capacitor, which depends on the amplitude of the input voltage, whereas the current mode filter generates voltages on each capacitor, which depends on the amount of the input current. Thus, to implement the current-mode FIR filter, the voltages on the capacitor, not the charges on them, need to be averaged.

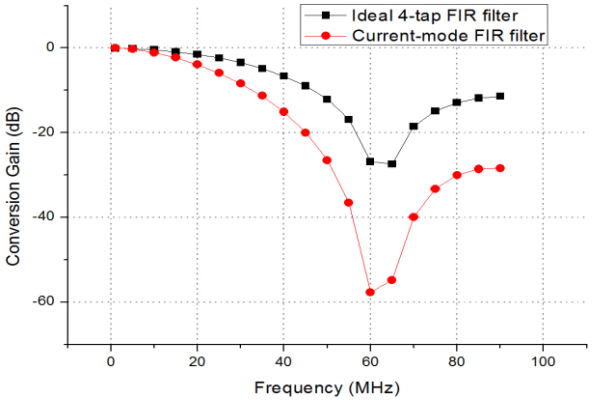

Fig-4: Frequency Response of FIR Filter

To accomplish voltage averaging, the voltage buffer circuit is applied in each sampling path. When the current integration on each sampling path is complete, the average voltage of four paths is stored in the output capacitor. The ideal 4-tap FIR filter frequency response and the designed 4-tap current-mode FIR filter frequency response are shown in Fig-4. The comparative results show that the current-mode filter can effectively reject the unwanted interferer.

3.3. Non-Decimation FIR (NDF) Filter

To overcome the limitations of the conventional FIR filter, we proposed an NDF filter [17]. In this filter, the moving-average output is re-sampled at the original sampling rate. For example, the Div-4 FIR filter needs six sub blocks to make up its 4-tap filter block: four for the sampling operation, one for the transfer operation, and one for the reset operation. A schematic of the NDF filter is shown in Fig. , there are all six sub-blocks in an NDF filter. Each sub-block sequentially performs the first through fourth charge sampling, transfer, and reset operations with delays of the clock duration.

As a result, the NDF filter can process the signal without any decimation effect. The filtering response of the NDF filter is the same as that of the FIR filter. Therefore, the order of the filtering response can be increased by cascading the NDF filter to an FIR filter. The filtering response of the cascaded NDF and FIR filters can be presented as Furthermore, a filtering response of $\mathrm{sin}\,c$ is possible through the cascading of (n-1) NDF filters to a FIR filter. Simulated filtering responses of only the FIR filter and of the cascaded NDF+FIR filter are shown in Fig. 11. By cascading the filters, we can achieve a higher attenuation level and a wider bandwidth at the null points of the filtering response.

$$\begin{aligned} |H_{NDF+FIR}(f)| &= |H_{NDF}(f)| \cdot |H_{FIR}(f)| \\ &= sinc(fmT_S) \cdot sinc(fmT_S) \\ &= sinc^2(fmT_s). \end{aligned}$$

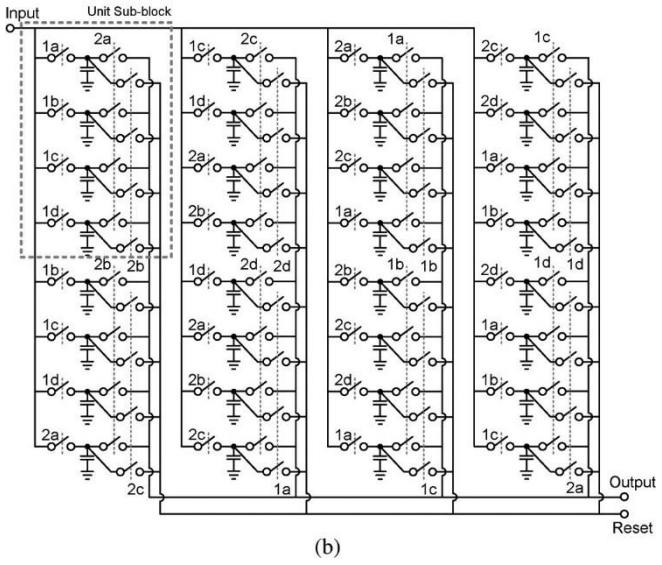

Fig-5: NDF Filter

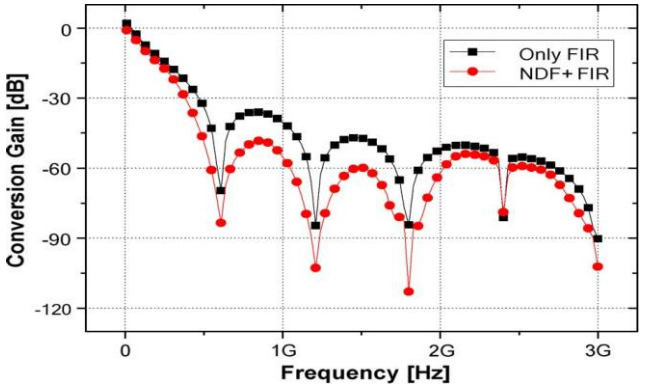

Fig-6: Frequency response for NDF+FIR Filter

4. MEASUREMENT RESULTS

The designed digital RF receiver front-end was fabricated using an IBM 130-nm RF CMOS process, and a photograph of the fabricated die is shown in Fig-7. The die size is 2200μm × 1200μm including pads, and its active area without pads is 1100μm × 800μm which is mainly occupied by the capacitors of the DT filter chain. For the test, a single-tone RF input near the carrier frequency with the fixed 2.3 GHz LO frequency is swept, and the low-frequency output of the DT filter after the external VGA is measured. As shown in Fig. 7, the measured filtering response matches the simulation result very well. Harmonic suppression of the DT filter from the second harmonics of at 143.75 MHz is measured to be less than 60 dB.

Fig. 8 shows the attenuation level at the first harmonic of. The measured result is about 90 dB, far below the required attenuation level of 67 db. The null point slightly deviates from the theoretical value, because the real buffered clock

signal is slightly different from the ideal clock signal. The in-band signal bandwidth for 3 dB is about 30 MHz, and the attenuation bandwidth at the harmonics is wider than 30 MHz.

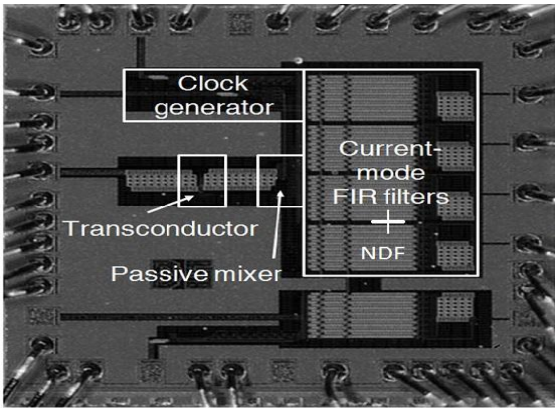

Fig-7: RF Cmos Chip

The noise figure is obtained using the following equations:

$$NF = P_{cold} - (-174) - 10\log B - G$$

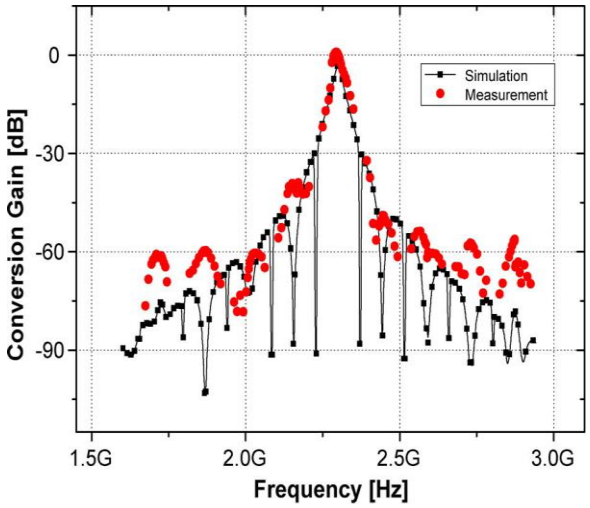

Fig-8: Conversion Gain of RF Receiver

Thus, the calculated is 5.79 dB considering the connection loss, the real noise figure is less than this value. A two-tone test and single-tone test are conducted to measure the linearity of the designed receiver front-end. Two-tone signals at 2.302 GHz and 2.303 GHz are used as RF input, and the fundamental IF output power at 2MHz (or 3 MHz) and IM3 power at 1 MHz (or 4 MHz) were measured. For the single tone test, the IF output power at 2 MHz was measured with a 2.302 GHz RF input. The in-band was measured to be 6.6 dBm and was 14.5 dBm. The measurement results for the designed digital RF receiver front-end are summarized in Table I.

Table I: Measurement Results For the Designed Digital RF Receiver Front-End For M-Wimax

Parameter	Value
Gain (@ 1 MHz) [dB]	0-30 dB
Bandwidth [MHz]	30 MHz
Attenuation [dB]	>80 dB
IIP3 [dBm]	+ 3.94 dBm
Noise Figure [dB]	5.79 dB
Power Consumption [mW]	26.63 mA
Active Area [mm2]	1100*800

5. CONCLUSIONS

We described a digital RF receiver front-end with wideband operation capability for m-WiMAX. The designed system employs a passive sampling mixer and a DT anti-aliasing filter. By controlling the LO signal, the filtering response of the DT filter can be changed flexibly. The modified FIR filter architecture is further optimized to reduce the number of required clock signals, simplifying the clock generator and improving the noise performance. In particular, the NDF filter, which has no decimation effect, is able to be cascaded to the conventional FIR filter. The new filter achieves function-type filtering response and can handle a wideband signal. A digital RF receiver front-end with a current-mode FIR filter for blocker filtering is proposed. The frequency response scalable FIR filter is introduced to reject the unwanted out-of-band interferer. In order to the filter operate in current domain to prevent the receiver from being saturated, an FIR filter that uses a voltage buffer is designed. The fabricated receiver system consists of a Transconductor, a passive mixer and the FIR filter stage. The measurement results show high blocker rejection with good linearity.

REFERENCES

[1]. B. Razavi, RF Microelectronics. Upper Saddle River, NJ: Prentice Hall, 1998.

[2]. K. Muhammad, R. B. Staszewski, and D. Leipold, “Digital RF processing: Toward low-cost reconfigurable radios,” IEEE Commun.Mag., vol. 43, no. 8, pp. 105–113, Aug. 2005.

[3]. T. Nguyen, N. Oh, V. Le, and S. Lee, “A low-power CMOS direct conversion receiver with 3-dB NF and 30-kHz flicker-noise corner for 915-MHz band IEEE 802.15.4 zigbee standard,” IEEE Trans. Microw. Theory Tech., vol. 54, no. 2, pp. 735–741, Feb. 2006.

[4]. S. O. Tatu, E. Moldovan, K. Wu, R. G. Bosisio, and T. A. Denidni, “Kaband analog front-end for software-defined direct conversion receiver,” IEEE Trans. Microw. Theory Tech., vol. 53, no. 9, pp. 2768–2776, Sep. 2005.

[5]. M. L. Psiaki, S. P. Powell, H. Jung, and P. M. Kintner, “Design and practical implementation of multifrequency RF front ends using direct RF sampling,” IEEE Trans. Microw. Theory Tech., vol. 53, no. 10, pp. 3082–3089, Oct. 2005.

[6]. K. Muhammad, Y. Ho, T. L. Mayhugh, C. Hung, T. Jung, I. Elahi, C. Lin, I. Deng, C. Fernando, J. L. Wallberg, S. K. Vemulapalli, S. Larson, T. Murphy, D. Leipold, P. Cruise, J. Jaehnig, M. Lee, R. B. Staszewski, R. Staszewski, and K. Maggio, "The first fully integrated quad-band GSM/GPRS receiver a 90-nm digital CMOS process," IEEE J. SolidState Circuits, vol. 41, no. 8, pp. 1772–1783, Jul. 2006.

[7]. H. Bagheri, A. Mirzaei, S. Chehrazi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. A. Abidi, "An 800-MHz—6-GHz software-defined wireless receiver 90-nm CMOS," IEEE J. Solid-State Circuits, vol. 41, no. 12, pp. 2860–2876, Dec. 2006.

[8]. K. Muhammad and R. B. Staszewski, "Direct RF sampling mixer with recursive filtering charge domain," in Proc. Int. Symp. Circuits Syst. 2004, May 2004, vol. 1, pp. 577–580.

[9]. D. Jakonis, K. Folkesson, J. Dabrowski, P. Eriksson, and C. Svensson, "A 2.4-GHz RF sampling receiver front-end 0.18-um CMOS," IEEE J. Solid-State Circuits, vol. 40, no. 6, pp. 1265–1277, Jun. 2005.

[10]. R. B. Staszewski, K. Muhammad, and D. Leipold et al., "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio 130-nm CMOS," IEEE J. Solid-State Circuits, vol. 39, no. 12, pp.
2278–2291, Nov. 2004.

[11]. S. Karvonen, T. A. D. Riely, S. Kurtti, and J. Lostamovaara, "A quadrature charge-doma sampler with embedded FIR and IIR filtering functions," IEEE J. Solid-State Circuits, vol. 41, no. 2, pp. 507–515, Feb. 2006.

[12]. M. A. T. Sanduleanu, M. Vidojkovic, V. Vidojkovic, A. H. M van Roermund, and A. Tasic, "Receiver front-end circuits for future generations of wireless communications," IEEE Trans. Circuits Syst. II, Exp Briefs, vol. 55, no. 4, pp. 299–303, Apr. 2008.

[13]. J. Craninckx, M. Liu, D. Hauspiel, V. Gianninil, T. Kim, J. Lee, M. Libois, B. Debaillie, C. Soens, M. Ingels, A. Baschirotto, J. Van Driessche, L. Van der Perre, and P. Vanbekbergen, "A fully reconfigurable software-defined radio transceiver 0.13mCMOS,"inProc. IEEE ISSCC Dig. Tech. Papers, Feb. 2007, pp. 346–347.

[14]. A. A. Abidi, "The path to the software-defined radio receiver," Proc. IEEE J. Solid-State Circuits, vol. 42, no. 5, pp. 954–966, May 2007.

[15]. H. Seo, I. Choi, C. Park, J. Yoon, and B. Kim, "Digital RF receiver front-end with wideband operation capability for m-WiMAX," in Proc. IEEE Radio Freq. Integr. Circuits Symp., Baltimore, MD, Jun. 2011, pp. 21–24.

[16]. IEEE Standard for Local and Metropolitan Area Networks, IEEE Std. 802.16e-2005, IEEE, Feb. 2006.

[17]. C.Park,J.Yoon, and B.Kim,"Non-decimation FIRfilter for digital RF sampling receiver with wideband operation capability," in Proc. IEEE Radio Freq. Integr. Circuits Symp., Boston, MA, Jun. 2009, pp. 487–490.