DESIGN OF A 5 PORT ROUTER FOR NOC USING VERILOG

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Abstract

Multiprocessor system on chip is emerging as a new trend for System on chip design but the wire and power design constraints are forcing adoption of new design methodologies. Researchers pursued a scalable solution to this problem i.e. Network on Chip (NOC). Network on chip architecture better supports the integration of SOC consists of on chip packet switched network. The proposed design of router is simulated and synthesized in Xilinx ISE 9.2iand the source code is written in Verilog.

Keywords: *Network on Chip, 5 port router, Xilinx ISE 9.2i.*

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1. INTRODUCTION

As per Moore's law the density of chip doubles every 18 months, so the parameters of a single chip get affected due to increase of processing elements on a chip. NOC is a packet switched on-chip data transfer network that solves challenges faced by SOC of bus based communication. The basic ingredients of NOC are topology which defines the communication architecture, routing technique which decides how the data is routed from sender to receiver, routers and switching technique which determines when the data flow through the routers.

NOC used only point to point wires for all network sizes and it increases the utilization of wires. The focus of paper is design of Network on chip five port routers. The effective on chip communication is achieved by router's routing functionality and efficient arbitration [1]. The main goal of this paper is the design of power and area efficient on chip router.

2. ROUTER BASICS

Advanced fabrication technologies and scaling have made it possible to integrate a large number of processor cores onto a single die, allowing us to obtain an entire Network-on-Chip (NoC). An example of a NoC with DRAM memory controllers and Dual Inline Memory Modules are shown in Fig 1, where a system consisting of 16 cores is shown. Arriving data is stored at the input buffers, which are divided into Virtual Channels (VC) to prevent deadlockand increase throughput. The VC allocator selects one VC for each input, and the switch allocator decides where each input will be routed to at the output port.

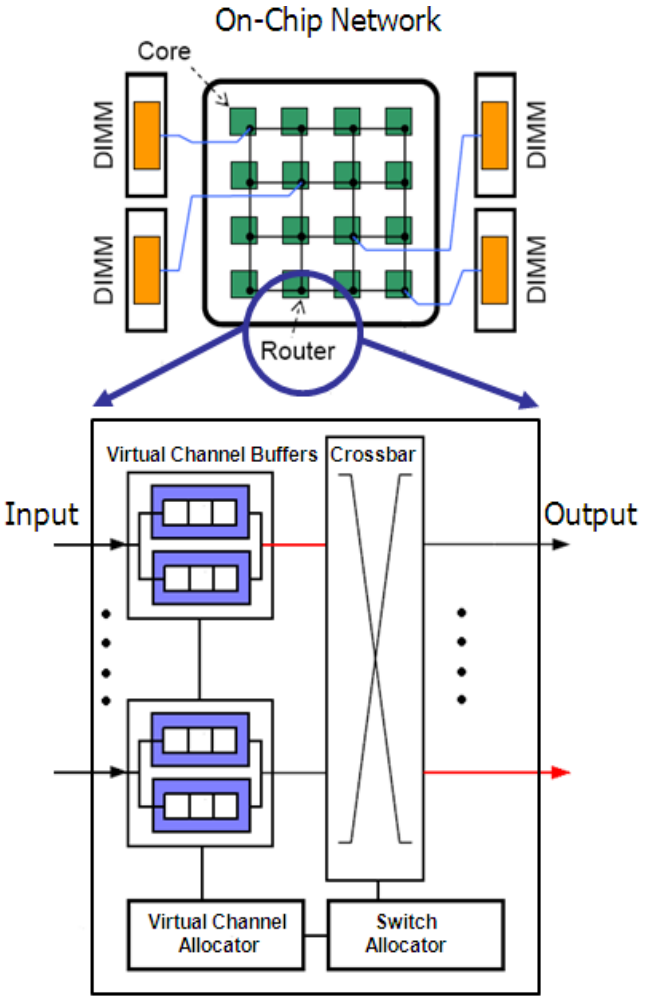


Fig 1: Network on chip-Router

3. BLOCK DIAGRAM OF 5 PORT ROUTER

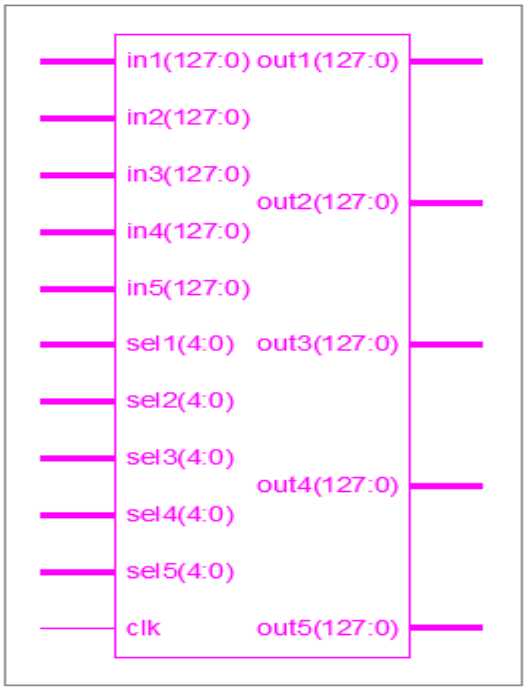
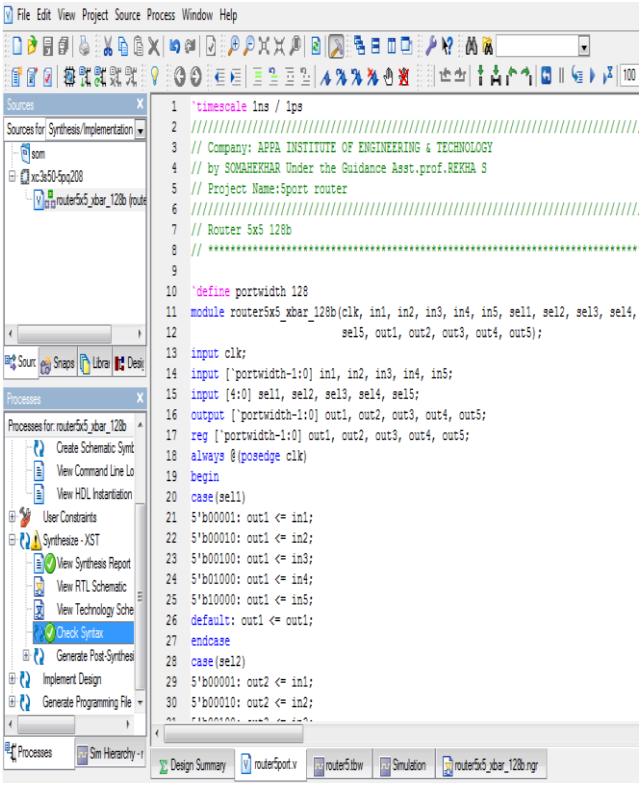


Fig 2: Block diagram of 5 port router

Source Code Written in Verilog



```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company: APPA INSTITUTE OF ENGINEERING & TECHNOLOGY
// by SOMAHEKHAR Under the Guidance Asst.prof.REKHA S
// Project Name:5port router
//////////////////////////////////////////////////////////////////////////////////
// Router 5x5 128b
// ***************************************************************************

`define portwidth 128
module router5x5_xbar_128b(clk, in1, in2, in3, in4, in5, sel1, sel2, sel3, sel4,
                           sel5, out1, out2, out3, out4, out5);
input clk;
input [`portwidth-1:0] in1, in2, in3, in4, in5;
input [4:0] sel1, sel2, sel3, sel4, sel5;
output [`portwidth-1:0] out1, out2, out3, out4, out5;
reg [`portwidth-1:0] out1, out2, out3, out4, out5;
always @(posedge clk)
begin
case(sel1)
5'b00001: out1 <= in1;
5'b00010: out1 <= in2;
5'b00100: out1 <= in3;
5'b01000: out1 <= in4;
5'b10000: out1 <= in5;
default: out1 <= out1;
endcase
case(sel2)
5'b00001: out2 <= in1;
5'b00010: out2 <= in2;
```

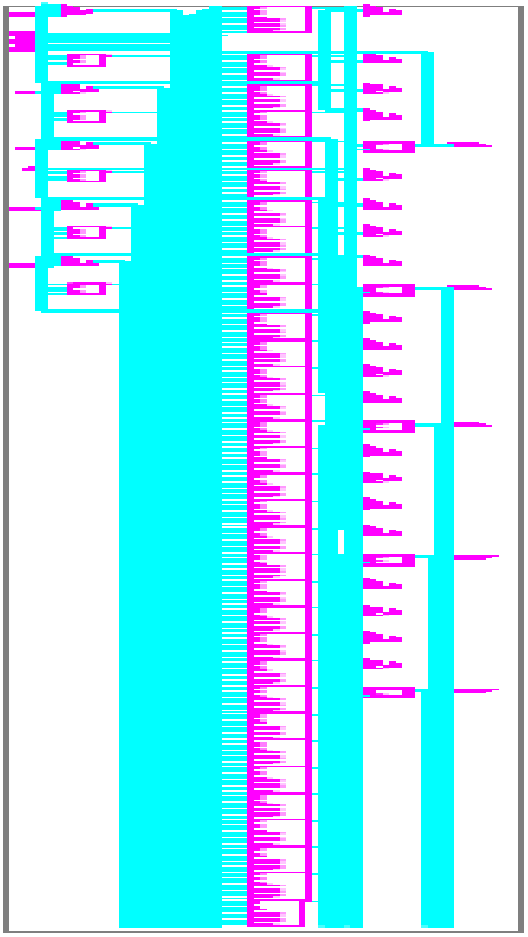
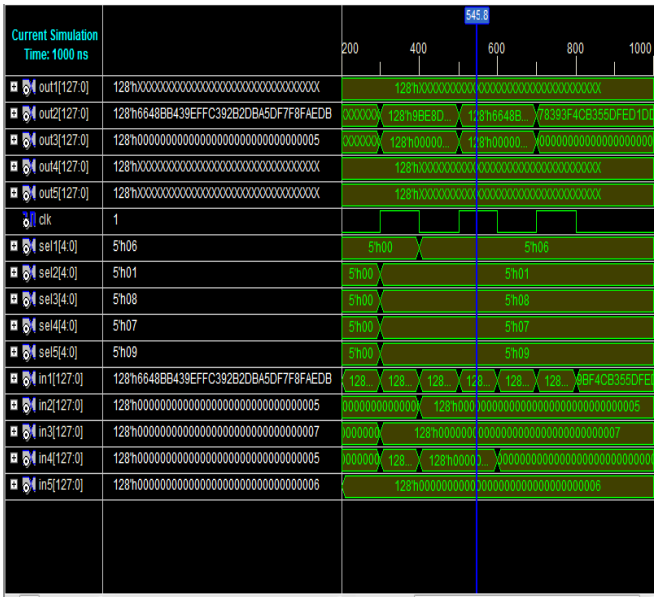


Fig 3: Schematic of 5 port router

4. SIMULATION RESULTS



5. CONCLUSIONS

The proposed design of 5 port router is simulated and synthesized in Xilinx ISE 9.2i and the source code is written in Verilog. This proposed design has high speed and less delay.

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