FPGA BASED: DESIGN AND IMPLEMENTATION OF NOC TORUS TOPOLOGY

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Abstract

The fundamental unit of building a Network on Chip is the router , it directs the packets according to a routing algorithm to the desired host. In this paper ,a router is designed using VERILOG language and implemented on Spartan 3E FPGA with the help of Integrated software environment (ISE10.1) . The utilization of the Spartan 3E resources is excellent (for example the number of slices required doesn't exceed 3%) .After that a (2×2) mesh topology and a (2x2) torus topology network is designed and implemented using FPGA . An example is applied on the designed Network on Chip (NoC) which validates the design successfully.

Keywords: *Router, SoC, NoC, VERILOG, FPGA, MESH, TORUS*

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1. INTRODUCTION

Advantages of Network-on-Chip (NoC) over traditional bus based architecture have been proposed in many researches.The NoC architecture has advantages in both scalability and flexibility thus it can be organized to run homogeneous cores in parallel to improve performance for specific purposes [1]. Such approach on NoC is a suitable method to realize a high throughput computational system on FPGA.

The real start of the NoC technology was in 2003 (S. Kumar and A. Jantsch and etc.)[2] discus the design of NoC based on packet switching technology,(R.Pau)[3]in his M.sc thesis designed a router using dual crossbar to connect the input and output ports , the disadvantage of this design was the large number of slices required on FPGA . (A. Shaabany and F. Jamshidi) [4] design a NoC router using handshaking flow control , they implemented the design on FPGA and ASIC, the result of this work is compared with the results of the proposed router of this paper, while the result of the designed NoC is compared with the result of Ref.[5]
In this paper , a proposed NoC router is designed such that all input ports are connected to the output ports yielding a lattice connections between the input and output ports. Using this router architecture a 2x2 mesh and 2x2 torus noc topologies are designed. The results show that NoC based on this router will minimize the number of slices and maximize the speed of flits flow.

2. DESIGN OF A NOC ROUTER

The design of a NoC Router is based on the following assumptions:-
1. It can work with XY routing algorithm
2. Each router has four bi-directional ports.
3. Handshake protocol is used for the interconnection between different routers.
4. Round robin protocol is used for the interconnection between the input and output ports.
5. Routers have input buffers only, this is due to the fact that wormhole switching mode of operation is chosen in this study.
6. The packets have variable number of flits and each flit size is equal to 8 bits.
7. The header length of the packet is one flit, which the payload can be any number of flits .The header contains all the necessary information to be used by the routing algorithm (such as XY) to direct a packet between two routers.
Fig1.shows the structure of Router architecture

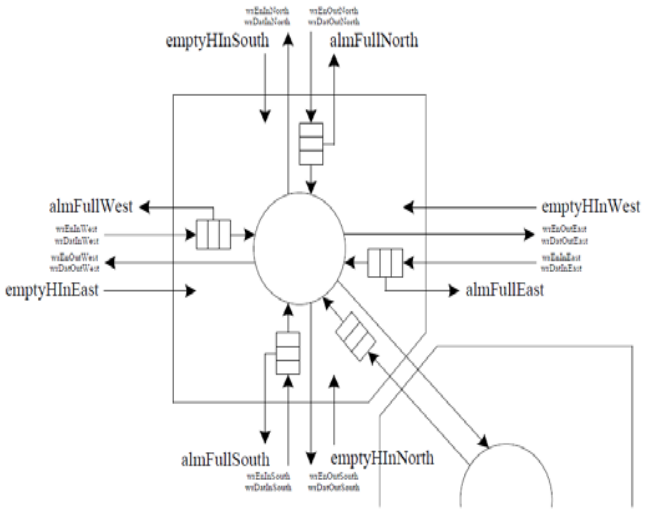

Fig 1. Router Architecture

Router is a packet based protocol. Router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet. The router has a one input port from which the packet enters. It has three output ports where the packet is driven out. The router has an active low synchronous input resetn which resets the router.

2.1 Packet Format

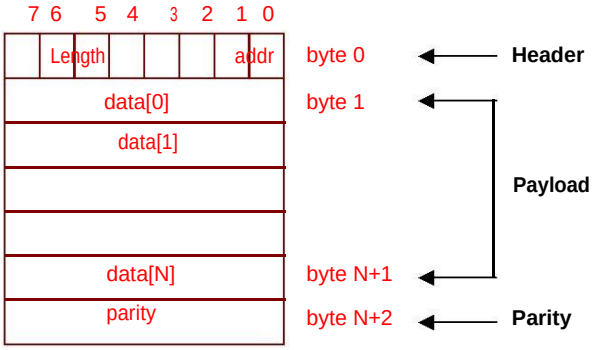

Fig2 Data Packet Format

Packet contains 3 parts. They are Header, payload and parity. Packet width is 8 bits and the length of the packet can be between 1 bytes to 63 bytes.

Fig3 shows the four port router architecture

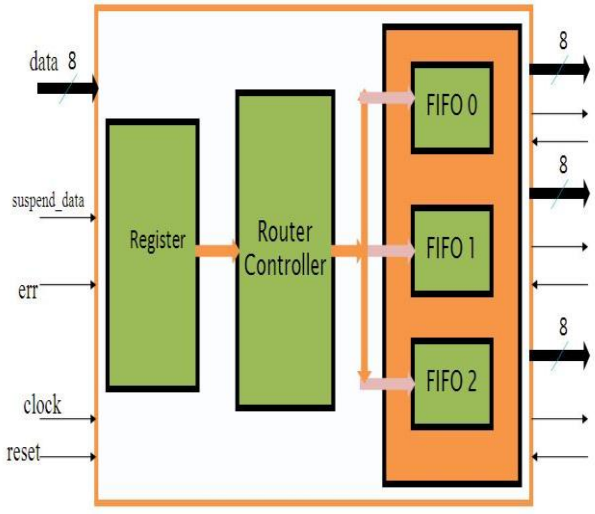

Fig 3 Four port router architecture

3. DESIGN OF A NETWORK ON CHIP

Different from other works use end-to-end traffic or only few input nodes as packet injecting points, our work takes input traffic from North, East, West and South and returns packets to all directions. In order to keep NoC low-cost and scalable, the NoC is constructed based on following principles:
1) No virtual channel or pipeline is used.
2) All PEs are designed for data processing only.
3) Architectures of all tiles are identical.
4) Unfinished packet should not leave NoC.

The design of a (Network on Chip (NoC)) is based on the following assumptions:-
1- Routers are arranged in mesh and torus topology and Fig4 and 5. shows this type of topologies. The routers being used is equal to (4) or (2×2).
2- (XY) or (YX) routing algorithms are applied to direct packets, between the routers of the (NoC) .Fig.5 shows an example of how to route a packet within the torus routers. Flow control of data between routers is based on handshaking protocol
3- Wormhole switching technique is adopted in this study.
4- because of wormhole switching model, buffering at the input of the router becomes sufficient to control the flow of data .
5- Round Robin arbitration is selected to provide a fair dynamic granting schemes
Figure (5) shows a block diagram of the designed (2×2) NoC.

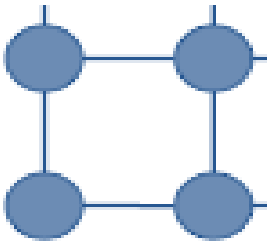

Fig 4 2x2 mesh topology of network

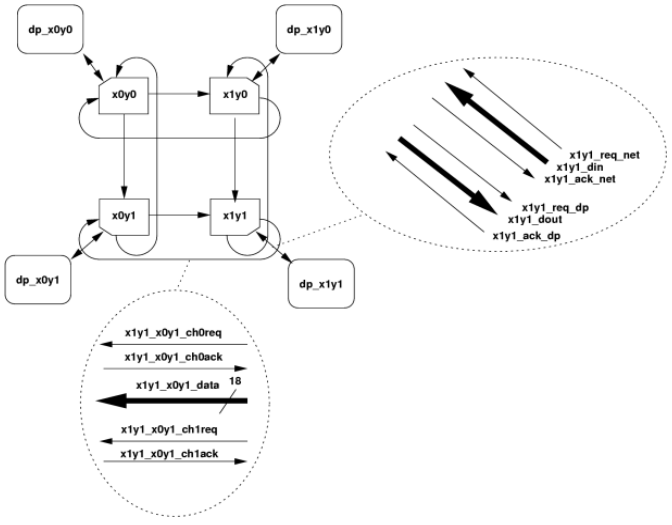

Fig 5 2x2 torus topology of network

4. RESULTS

4.1 The Simulation Results of a Router on Chip, 2x2 Mesh Topology and 2x2 Torus Topology

Design of a router and 2x2 mesh and 2x2 torus topologies are first simulated using ISE 10.1 software and the waveforms of the simulated are shown in Fig6, 7, 8

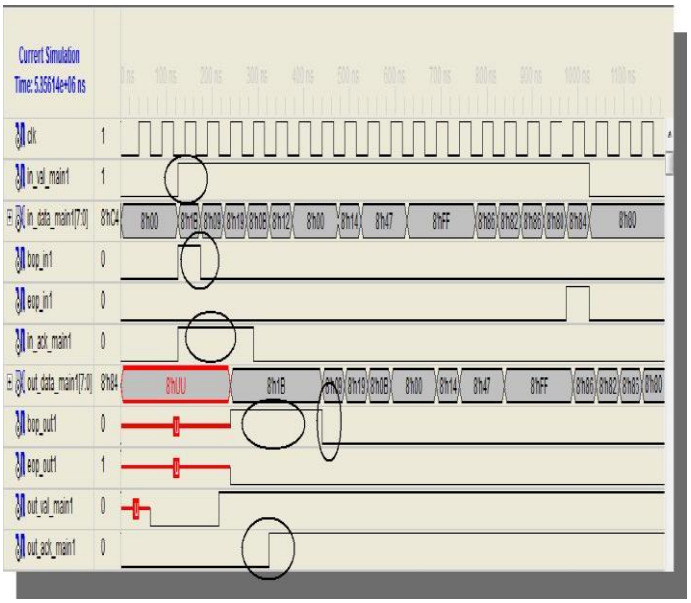

Fig 6 Simulation result of a router of network

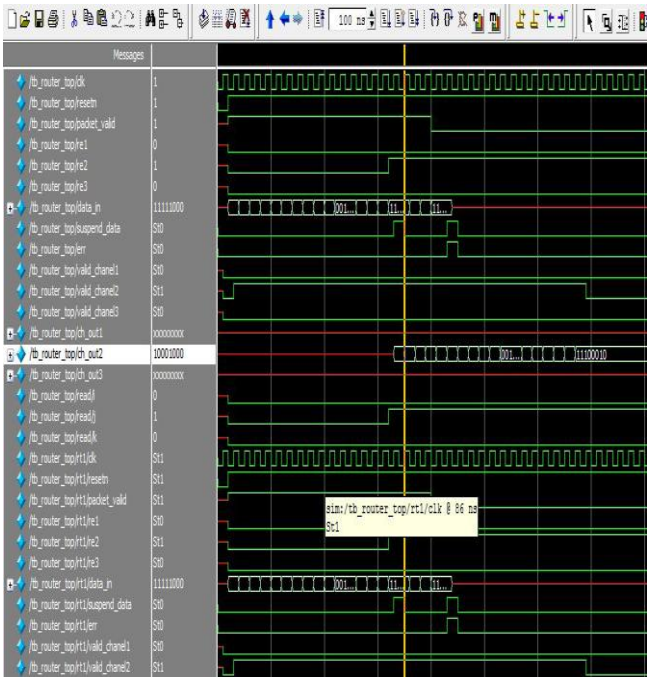

Fig 7 Simulation result of a 2x2 mesh topology of network

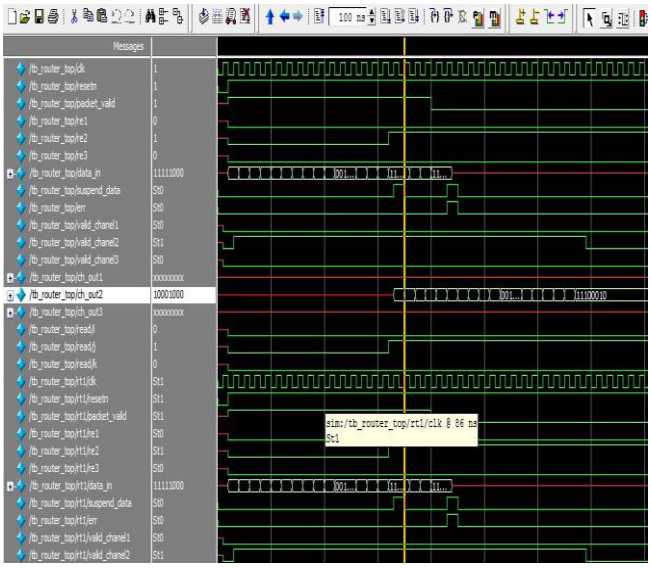

Fig 8 Simulation result of a 2x2 torus topology of network

Table 1: The Routers Results Using Xilinx Spartan 3E

	The Proposed Router			Asyn.router[8]		
Resource	Used	Avail	Utilization	Used	Avail	Utilization
CLB Slices	185	8672	2%	274	8672	**3.16%**
IOs	97	194	50%	101	194	**52.06%**
DFF or Latch	148	22100	0.66%	176	22100	**0.80%**

5. CONCLUSIONS

The designed router which is based on the lattice connections between its input and output ports consumes only 2% of the total number of slices of Spartan 3E FPGA ,while the nearest router which is designed in Ref.[8] consumes 3.16% of the total number of the slices of Spartan 3E.This types of routers reduces to a large extend the number of slices required to design a 2×2 NoC . It is found that the number of slices required to design a 2×2 NoC using the traditional router is almost four times the number required using the proposed router. The flexibility of the designed router facilitates the design of larger NoC like 4×4 easily. On the other hand , the practical example conducted in this study using FPGA technique validates the designed router and network on chip. Using this router 2x2 mesh and torus topologies are successfully designed.

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