DESIGN OF HIGH SPEED AREA OPTIMIZED BINARY CODED DECIMAL DIGIT ADDER

Deepak Rao[1], Anuradha[2]

[1]*Department of ECE, VLSI Design & Embedded System, Appa Institute of Engineering &Technology, Gulbarga*
[2]*Department of ECE, VLSI Design & Embedded System, Appa Institute of Engineering & Technology, Gulbarga*

Abstract

Decimal arithmetic is necessary for computations in the field of banking systems,tax calculations,telephone billings etc. The main problem in the prevailing decimal arithmetic is the requirement of the correction of the result in its binary form. This results in larger area and implementation delay. The proposed adder is improved for less delay and area requirement as a correction free mechanism provides the result without adding any correction values.

Keywords:*BCD Adder, Verilog code, Xilinx 9.2i.*

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1. INTRODUCTION

Inthe era of electronic computing, decimal arithmetic plays a vital role in commercial, financial, internet and industrial control applications. Most of the computing applications are based on binary arithmetic, but the real problem is that binary approximation does not produce accurate result. For example if a telecommunication company approximates a 5% sale tax on an. Binary decimal arithmetic is required to avoid such incorrect approximations. Also, in most of the applications, decimal software runs on custom binary hardware in order to produce precise decimal results, leading to another problem of excessive delays. Software implementation of decimal arithmetic is about 100 to 1000 times slower than the binary implementation in hardware. In a survey of IBM corporation showed that almost 55% of the numeric data columns, used by 51 major organization's databases, were decimal data types and 43.7% were integer types which can be stored as decimals. In order to meet the need for growing evolution of decimal arithmetic, it's necessary to develop efficient algorithms.Decimal digit adders and decimal digitmultipliers are the building blocks of anydecimal hardware to support decimalarithmetic.Here is a proposed high speed and area optimized decimal digit adder. The design is described and simulated using verilog hardware description language.

2. LITERATURE SURVEY

A combined binary and decimal adder was introduced by I.S.Hwang[3]. The binary carry look ahead adder adds two input operands which are either binary or decimal. Also a reduced delay bcd adder with improved delay was proposed by AlpArslaBayrakci and Ahmet Akkas[1]. Here a parallel prefix network was used to generate carry thereby reducing the delay in multi digit addition. Decimal Multiplication via carry-save addition was introduced by Mark A.Erle and Michael J.Schulte[5] where carry save addition was used to reduce critical path delay.

3. PROPOSED BCD ADDER

Here an optimized correction free BCD digit adder is proposed. The 2 decimal input digits of the BCD adder are A_{ϵ} {0, 9} and B_{ϵ} {0, 9} and the decimal carry input is C_{in}. We can represent the decimal sum and the decimal carry as as S_{ϵ} {0, 9} and C_{out} respectively. The decimal value of A, B, and S can be used to obtain their 8421 BCD representation. In general, we can write A =$a_3a_2a_1a_0$, B = $b_3b_2b_1b_0$, and S =$s_3s_2s_1s_0$, where a_i, b_i, and s_i € {0, 1} ∀ i € {0, 1, 2, 3}. A and B can be expressed in terms of two integers m = $a_3a_2a_1$and n = $b_3b_2b_1$as:

A = $2 \times m + a_0$and B = $2 \times n + b_0$, where $0 \leq m \leq 4$ and $0 \leq n \leq 4$.This implies that the output of the BCD adder can be expressed as

{COUT, SUM} = A+B+CIN

We can rearrange the above expression for BCD adder output as:

{COUT,SUM} = (2 x m + a0) + (2 x n + b0) + Cin
=(2 x n +m) + (a0+b0+Cin)

Using the above formula, BCD digit adder is designed that consists of two stages: Stage1 and Stage2. The inputs to Stage1 are m and n. Stage1 generates the partial decimal sum: Z = $z_3z_2z_1z_0$0 = 2 × (n + m). It should be observed that this decimal partial sum consists of an even decimal digit ($z_2z_1z_0$ 0) and a decimal carry z_3 that can be either 1 or 0 based on the values of m and n.

4. BLOCK DIAGRAM.

This block diagram consists of two stages wherein the first stage computes the n and m values from the given input values. Stage 1 generatespartial decimal sum Z = Z0Z1Z2Z3 =2 x (n + m). This partial sum consists of even decimal digit z2z1z00 and a decimal carry z3 based on m & n. The second stage generates the required sum. Since result of stage1 is always even, only z2z1z00 are passed to stage2. The outputs of Stage1 along with a0, b0, and Cin are given as input to Stage2. In order to design Stage2, the values of Cout, s3, s2, s1, and s0 are calculated for all possible combinations of z3, z2, z1, z0, a0, b0, and Cin and optimized boolean equations for Stage2 are derived.

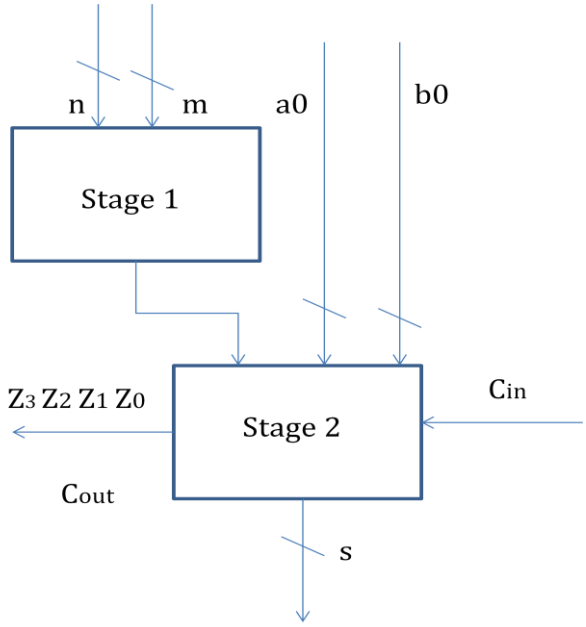

Fig 1 Block Diagram of proposed Adder

5. SIMULATION RESULTS

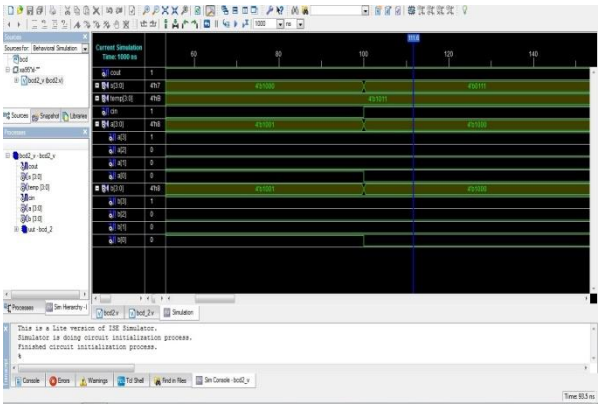

Fig 2 Simulation result of correction free BCD Adder

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	15	3584	0%
Number of 4 input LUTs	27	7168	0%
Number of bonded IOBs	18	141	12%

Fig 3 Design Summary

Figure 2 here shows the simulation result of the proposed BCD adder. Two decimal numbers less than 9 are added. Figure 3 shows the device utilization summary iwhich shows the number of LUT's required, number of slices and number of IOB,s sequentially.

6. CONCLUSIONS

In this report, direct Boolean expression binary coded decimal digit adder will produce the output in the BCD form. As a result a correction free BCD digit adder is obtained when compared with the existing system which needs an analyzer circuit for determining the whether the output value is greater than 9.Here the Boolean expression is obtained using two-level logic optimization is modified to multilevel logic optimization for reducing the area and delay. The design is synthesized, verified and tested for correct functionality using verilog coding and simulation.

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