DESIGN AND VERIFICATION OF PIPELINED PARALLEL ARCHITECTURE IMPLEMENTATION IN FPGA FOR BIT ERROR RATE TESTER

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Abstract

The principle measure of performance of a data transmission link is Bit Error Rate (BER). A BER testing scheme is introduced to describe the quality of communication interfaces for multi-channel. Bit errors results due to the improper design and implementation of the link or external noisy environment. We present a parallel pipelined architecture which is efficient in power as well as cost. The Universal Asynchronous Receiver/Transmitter (UART)-RS232 standard communication is employed for all the data logging and on/off line analysis. In electronic packaging systems, the signal quality of channels is determined by eye diagram simulation. The tester incorporates a setup of Pseudo Random Binary Sequence (PRBS) generator, detector and error computation block. Point-to-point serial optical link setup is used for measuring the performance of the tester. At the receiver, the data is compared with the local sequence generator. Synchronization is maintained throughout the transmission with the assistance of pilot sequence. The functions of tester are implemented in FPGA virtex5 device by Xilinx. The quality factor of measured error rate is determined using eye-diagram simulation for more than one channel.

Keywords— *Bit-error rate (BER), Universal Asynchronous Receiver/Transmitter (UART), Pseudo Random Binary Sequence (PRBS), eye diagram.*

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1. INTRODUCTION

In a communication system, the data signal is sent from transmitter to receiver using the channel which acts as the medium of communication. The transmitted signal is corrupted by the channel in random manner [1]. Error free data transmission is essential in this decade due to its wide application in both military and commercial communication systems. The Bit Error Rate (BER) test acts as the fundamental measure for assessing the performance of the channel. The BER is the unit less ratio of the number of bit errors divided by total number of transmitted bits during a given time interval [2]. For example, a BER is measured for 1 billion bits means that 1 bit out of billion bits is, on average, read incorrectly. The amount of damage to the data is decreased and accuracy is increased by reducing the BER. The sequence generator is used for generating random data and is also known by the receiver in order to obtain accurate error free result. Pseudo Random Binary Sequence (PRBS) is commonly used for generating a random input data stream at the rate of 2^n-1. Initially, synchronization is achieved and as the data propagates the synchronization is lost due to delay occurrences in channel. In order to maintain the synchronization throughout the communication, pilot sequence is used at both transmitter and receiver side. The error rate is determined by comparing the received sequence with original sequence. In case of mismatch between the patterns, the error counter is increased. The result of the error rate measurement may be presented in many ways: As number or diagrammatic format. The number of bits being error is measured for each and every second. Mostly, the communication is focused on single channel not on multi-channel due to its complexity in testing the platform. Here, a multi-channel (i.e., for more than one channel) BER is introduced in order to minimize the computation time and power. In practice, the balance between the bandwidth and Signal to Noise Ratio (SNR) is maintained to maximize the channel capacity for an acceptable BER performance. They are designed to be interfaced with the Universal Asynchronous Receiver Transmitter (UART) of a host via RS-232. The received data is used for simulating eye diagram and quality factor are analysed.

2. BER BACKGROUND AND RELATED WORKS

BER is an important parameter in communication systems for achieving accuracy and reliability. In a digital communication system, either the channel or the communicating devices (sending and/or receiving end) can introduce distortion or cause errors. As modern communication interfaces are quite complex, besides inherent device and timing imperfections, the correctness and performance of communication interfaces depend on many design choices, such as types of waveforms used to transmit the information over the channel, the transmitter power, the characteristics of the channel (i.e., the amount of noise, the nature of the interference), and the method of demodulation and decoding.The results closely related to our work are explained in this section.

Yongquan Fan et.al, proposed a versatile BER testing procedure which is suitable to both presilicon and postsilicon method to characterize the quality of the communication. Both Bit Error Rate Tester (BERT) and Additive White Gaussian Noise (AWGN) are incorporated in a single FPGA, which is suitable for the testing and characterization of a wide range of signal communication interfaces and the results obtained are analyzed [1]. Ronald Holzlöhner et.al presented a novel linearization method to calculate accurate eye diagrams and bit error rates (BERs) for arbitrary optical transmission systems and apply it to a Dispersion-Managed Soliton (DMS) system and the results are verified [3]. Further, the optical noise distribution at the receiver is calculated and from that accurate eye diagrams and bit error rates (BERs) are obtained. Stefan Erb et.al identified that timing jitter is a major limiting factor for data throughput in serial high-speed interfaces, which forces an accurate analysis of the impact on system performance [4]. Further, Histogram-based methods have been developed for this purpose, and can directly relate collected jitter distributions with the bit-error rate (BER).A powerful class of tail fitting methods for jitter and BER analysis implemented and results are analyzed. Dongwoo Hong et.al analyzed that high-performance serial communication systems often require the bit error rate (BER) to be at the level of 1012 or lower. The excessive test time for measuring such a low BER is a major hindrance in testing communication systems. Jitter spectral information extracted from the transmitted data and some key characteristics of the clock and data recovery (CDR) circuit is used to estimate the BER effectively without comparing each captured bit for error detection [5].This thesis is efficient by means of power consumption due to parallel pipelined architecture.

3. ARCHITECTURE

The BER architecture as shown in Fig.4 is valid only for long number of bits. BER is an indication of how often data has to be retransmitted because of an error. The master clock provides a frequency of about 50MHZ and is supplied to the clock manager. It increases or decreases the frequency according to the individual block needed. Multiplier increases the frequency and decimator decreases the frequency.

3.1 PRBS

The basic setup for measuring bit error rate includes the Pseudo-Random Bit Stream (PRBS) generator and an error detection comparator. The information source generates a PRBS at the rate 2n-1, where n is the total number of bits. PRBS is generated using Linear Feedback Shift Register (LFSR). LFSR is a shift register whose input bit is a linear function of its previous state. Here linear function used is XOR. The bit positions that affect the next states are called Taps. The Taps are XOR sequentially with the output bit and then fed back in to the leftmost bit. LFSR has finite number of states and repeats its cycle until a state which contains all zeros is obtained [1]. Appropriate time management reduces the number of errors over the communication channel. The output of the shift register bank, which is either 0 or 1, is purely at random, whereas the sequence length and shift clock frequency (i.e., the bit rate) are both limited. In this sense, the sequence is pseudorandom generator consist of n-tap shift register bank. A pseudorandom sequence will be generated, if the initial states of the shift registers are not wholly zeroed [6]. Five shift register is taken into account for generation of random data. The bit positions that affect the next states are called Taps. The output of last flip flop is tapped with the previous flip flop output and so on as shown in Fig.1. The Taps are XOR sequentially with the output bit and then fed back in to the leftmost bit. The LFSR architectures can also face fan-out issues due to the large number of nonzero coefficients especially in longer generator polynomials. A maximum-length LFSR produces an m-sequence (i.e. it cycles through all possible $2^n - 1$ states within the shift register except the state where all bits are zero), unless it contains all zeros, in which case it will never change.

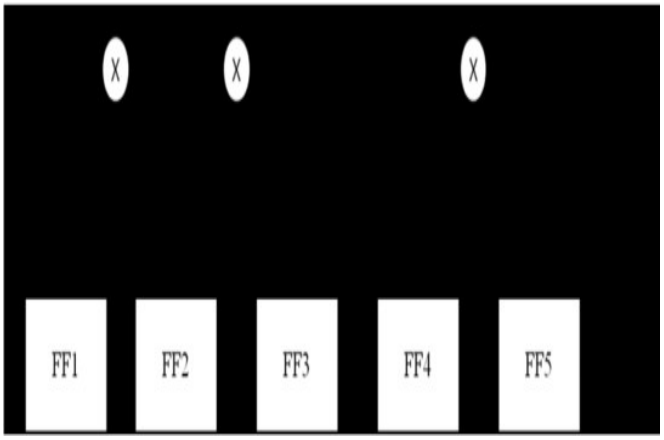

Fig 1 Structure of LFSR

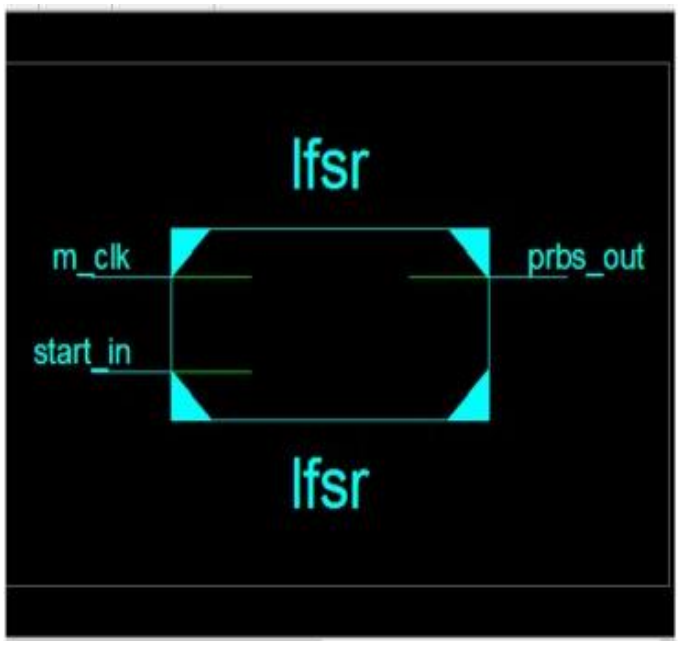

Fig 2 RTL Schematic of PRBS Generation

The Register Transfer Level (RTL) shows the input and output of the generation of the data as shown in Fig.2. The m_clk and start_in acts as the input and prbs_out acts as the output. As the clock signal goes high, the ‗lfsr_reg' starts to generate the random data by shifting the last bit of every data sequence to the front end as shown in Fig.3. The ‗clk_sig' is generated from the master ‗m_clk' to reduce the speed of the process and to interface with the processor.

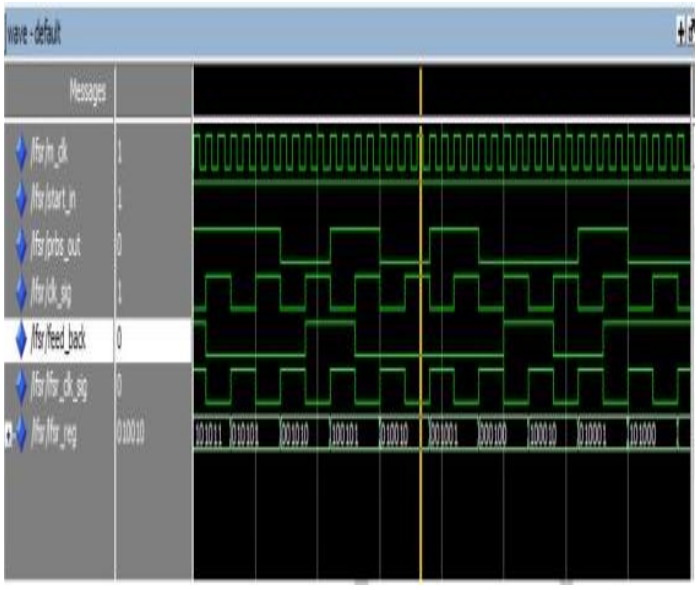

Fig 3 PRBS Sequence

3.2 Transmitter

Line encoding technique helps to convert the Unipolar Non-Return to Zero (NRZ) sequence into Unipolar Return-to-Zero (RZ) sequence. As the channel bit rate increases, the optical modulation becomes essential. To maintain the synchronization between sender and receiver, noise and jitter parameters should be avoided. The voltage and current controller provides the power needed for the optical modulation. The modulated signal is send to the communication channel through Optic Cable. i.e., Single Mode Fiber Optical Channel (SMFOC). The data is passed through the channel as single ray of light.

3.3 Receiver

At the receiver, optical detector converts the optical signal into electrical signal. The results are passed into the Trans Impedance Amplifier (TIA) for decoupling. It acts as matching network for line decoding. It also used to increase the gain of the input. The part of TIA output is given to the high speed Analog to Digital converter. The converted data is send to Data Sampling Architecture according to the control signal provided by the architecture. The sampling part has an enable signal which controls the start as well as end of conversion. The remaining part of output is sent to the line decoder which converts the RZ into NRZ. The error computation part has numerous inputs namely 1 sec clock counter, local sequence generator and line decoder. The output is given to the Bit error (BE) data and data sampling architecture. The data is given to the data sampling provided in the RAM. Now, both Bit error data and sampled data are passed in to the circuit through 2x1 mux. A select line is provided in order to send both the data alternatively. The device controller receives the data and passes it to General Purpose Interface (GPIF). It verifies whether the First In First Out (FIFO) receiver is empty or filled with data. A Phase Locked Loop (PLL) is used to lock the particular data which is going to be sent. The received data is passed to the MATLAB for eye diagram simulation. The various parameters are analyzed from eye diagram and ensure the quality of the communication.

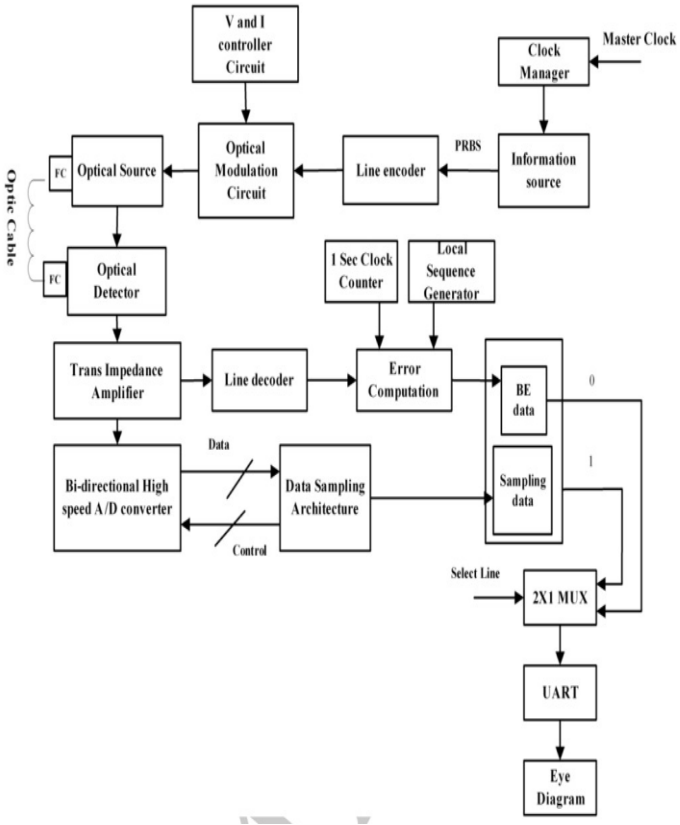

Fig 4 Architecture of BERT

3.4 UART

A Universal Asynchronous Receiver-Transmitter (UART) is developed with RS232 protocol in FPGA for data acquisition. UART is the important component for serial communication in computer. The Universal Asynchronous Receiver/Transmitter (UART) takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes. Transmitting and receiving UARTs must be set at the same baud rate, character length, parity, and stop bits for proper operation. The data which is generated using LFSR is sent through this communication and received using the same architecture as shown in Fig.5 with the help of the FPGA. Further, FPGA helps in faster communication of data rather than the normal speed. The data which is to be transmitted is initially stored in a data buffer and later transmitted to communication frame planer for every rising edge of the ‗data_rd'. Each byte is split into bits for transferring purpose. The data are forwarded into the ‗mux1' and then to Parallel In serial Out Shift Register (PISOSR). The shift register transmits one bit at a time to the output ‗txd' through ‗mux2'. The transmitted output data is ‗sdata(0)' for every rising edge of the ‗clk_sig'. ‗stop bit' is used for stopping the communication. The master clock signal is referred as ‗m_clk'.The high speed baud rate counter module generates the baud rate clock at the rate of 9600 for data acquisition to update the real-time performance of the system and generates ‗clk_sig' from the master clock. The bit shift controller provides necessary information to the byte shift controller through ‗cnt2' regarding the status of the shifting data. Byte shift controller intimates the ‗mux1' regarding the transmission completion of a byte through ‗cnt3'. Hence, the ‗mux1' initiates the second byte transmission. Once, all the data transmission is completed, ‗data_rd' terminate the communication and return to its original state. The same process takes place for all transfer of data using this application.

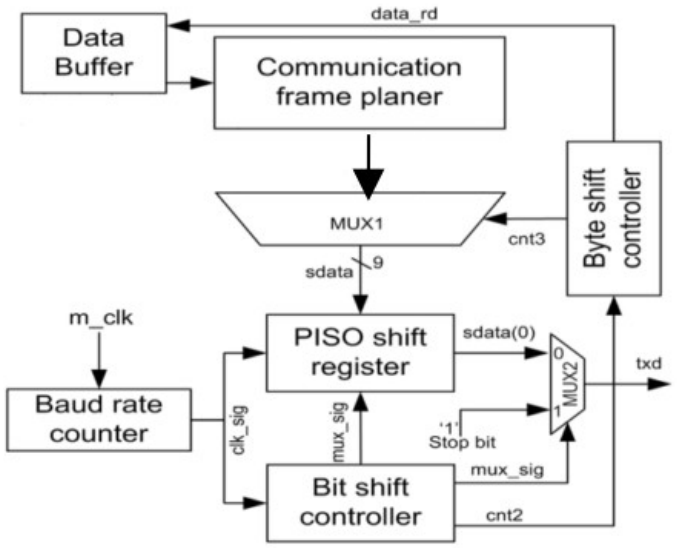

Fig 5 UART-RS232 communication protocol

As the clock is set to high and input data is set the shifting process takes place for the given data. The data which is sent to the receiver is shifted to the front end. A complete ‗8' shift indicates that one byte is sent to the receiver. Followed by data bits, arrival of ‗1'indicates that the data transmission is terminated.

4. DESIGN FLOW

The basic concept of BER measurement is sending a data stream to a Device Under Test (DUT), compare the output ofthe DUT with its input, and differences are registered as errors and evaluated [8].

4.1 Outline

The measurement process consists of transmitter, receiver, Fiber Optic Cable (FOC), and pilot sequence for synchronization. This pilot sequence is present in input PRBS generator and in receiver. It consists of two mode of operation namely synchronizing mode and monitoring mode. The PRBS generator at the transmitter is configured such that it senses synchronization sequence upon reset (or) power up.

Once the valid synchronization is detected, then BERT is tuned to the monitoring mode. Once synchronization is achieved, there won't be any response to the receiving data. Both the states should be monitored continuously in order to check the mode of operation.

4.2 Confidence Level

The confidence level is defined as the probability, basedon a set of measurements, that the actual probability (Measured BER) of an event is better than some specified level (Error BER) as shown in Fig.6. Many components in digital communication systems must meet a minimum specification for the probability of bit error. The probability can be estimated by comparing the output bit pattern with a predefined pattern applied to the input.

$$CL = 1 - e^{-N_{bits} * BER}$$

Where N_{bits} is the number of bits and BER is the ratio of error bits/no of bits transmitted. If the transmission system had a BER of 1012 and running at 155Mb/s, the average time between errors would be 10,000 seconds. At 3600 seconds in an hour, the average time between errors would be nearly 3 hours. There is a need of more than just one ―error event‖ to have any confidence at all in stating an error rate‖.

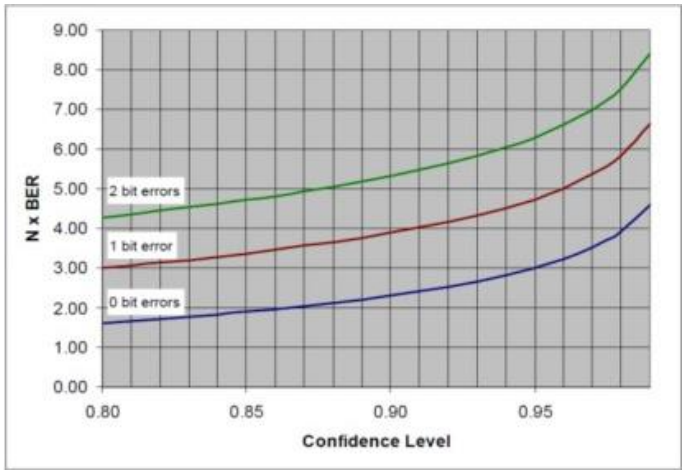

Fig. 6 Transmitted bits (normalized to the BER) Vs confidence level for 0, 1, 2 bit errors

4.3 Eye Diagram

The sampled data can be displayed on a device without alteration, in the order in which the data were sampled. In such a case, instead of arranging every sampled point in a time series, the sampled points may be superposed from the time zero over a specified interval. An eye diagram can be displayed by repeating this process for every sampled point [7]. Since a digital communication system suffers from a wide variety of effects that are difficult to accurately analyze, gaining confidence by software simulation is an essential part of the development stage. The Q-factor is obtained by measure of eye opening [9].

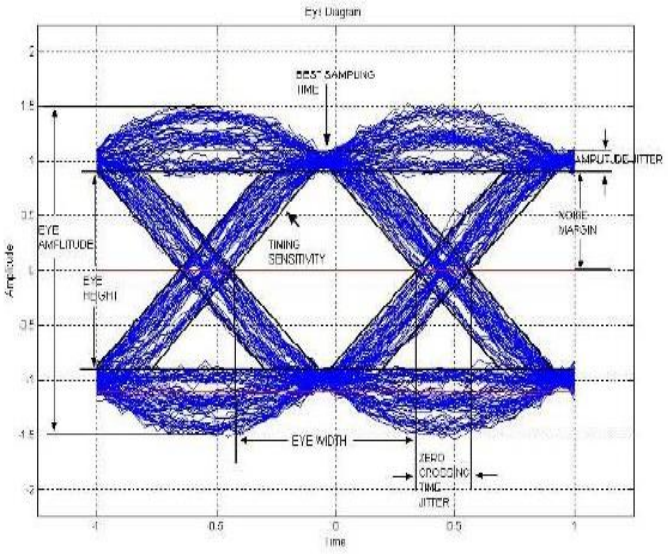

Fig. 7.Eye diagram

Eye width is the time interval over which the received signal can be sampled without error. Eye height is the vertical opening of the eye and defines the noise margin of the system. Eye amplitude represents the power in the eye actually carrying information and does not account of any noise that may be present in the signal. Timing errors is the rate of closure of the eye as shown in Fig.7. Best Sampling Instant is that time in the eye where the vertical width of the eye is at maximum. Noise margin is the difference between the 1 level and amplitude level that divides the eye in two equal halves in the vertical direction. Bit Rate is the inverse of a bit period. Jitter is the measure of deviation of a signal from its ideal time position. Eye Opening Factor is the measure of actual eye opening to the ideal noise free eye. Crossing Percentage is the location of zero crossing as a percentage of the eye opening. Quality factor is the vertical opening of the eye relative to the noise present.

5. EXPERIMENTAL RESULTS & DATA ANALYSIS

For the optical communication, the passage of data is ray of single light and hence, the error free communication is essential. For 1 billion bits one error is acceptable. The BER usually specifies the average incorrect bit identification. In digital communication there are many effects that are not easy to investigate; software simulation and FPGA implementation of the system makes us to understand more clearly about the development of the system. The data which

is received through UART communication is received and checked for error. The corresponding data logging is provided. The confidence level ensures that the communication is more efficient.

Table 1 Real time data logging data id 1

Data ID 1
Date 22-Jan-2014 09:40:20
Error Bit 33016
Bit Error Rate 2.064E+003
Confidence Level1.000E+000
==========

Data ID 2
Date 22-Jan-2014 09:40:20
Error Bit 0
Bit Error Rate 0.000E+000
Confidence Level0.000E+000
==========

Data ID 34133
Date 22-Jan-2014 09:41:59
Error Bit 0
Bit Error Rate 0.000E+000
Confidence Level0.000E+000
==========

Data ID 34134
Date 22-Jan-2014 09:41:59
Error Bit 0
Bit Error Rate 0.000E+000 Confidence Level0.000E+000
==========

The data logging table contains data id, data acquisition time, total number of error bits /sec, BER / sec and confidence level. The BER is calculated from the number of error bits and bit rate of the communication link and it is widely recognized in digital communication [10]. The value of the BER is substituted to calculate the confidence level. Regardless of the generation scheme, going down to low error rates requires many samples just to exhibit errors for BER = 10−12 at a 1-GHz data rate, it takes 3 h (assuming running 1013 bits to guarantee a 10−12 BER level). In production, the normal practice to qualify the BER performance at such low levels is through extrapolation [11]. The error bits logged on 22 January 2014 is shown in Table 1 and the corresponding graph is shown in Fig.9. The plot is between the BER Vs time and it shows that the number of the errors reduced with respect to the time (in seconds).

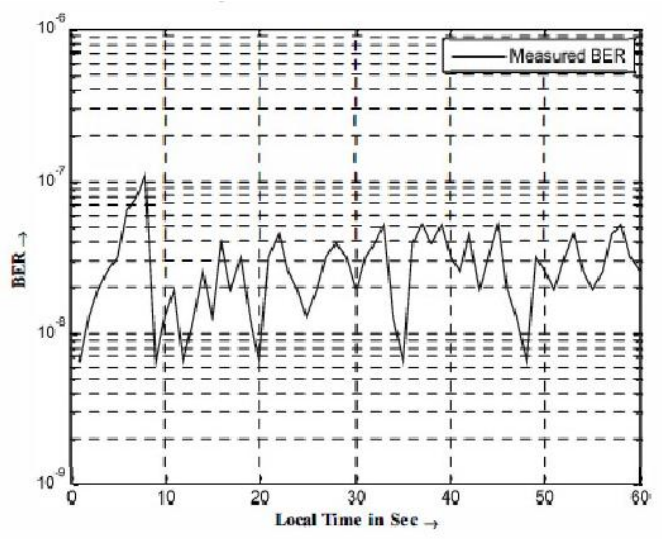

Fig 8 Bit Error Rate

6. CONCLUSIONS

BER of digital communication system is an important figure of merit used to quantify the integrity of data transmitted through the system. Testing for a finite length of time yields the estimate of the probability that a bit will be received as error. Thus, a BER is measured by performing the test for the limited duration and calculating the number of errors encountered in the known number of transmitted bits. The data rate at which bits enter the transmission channel is 155mbps. Timing is a most critical task in the designing phase leads to a reduction in the number of the transmission errors. Detecting timing problems early in the design process not only saves time but also permits much easier implementation of design alternatives. FPGA used here makes the data transfer faster as well as error free communication. The eye diagram which is generated shows that the synchronization between the transmitter as well as the receiver is good. Further, parallel operation and serial communication helps in reducing the error to greater extent.

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