POWER REDUCTION THROUGH MERGED FLIP-FLOPS

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Abstract

Optimization of power is always one of the most important design objectives in the modern ICs. In that maximum power is consumed by clock, the power is reduced using multi-bit flip-flops. This process is achieved by merging some of the flip-flops used in the circuit, based on the timing and capacity constraints. Merging of flip-flops is done with help of co-ordination transformation and combination table. We can achieve better area minimization, wire length reduction and power reduction by 75%.The experimental results are shown through the above parameter achievements.

Keywords: *Multi bit flip-flop, Merged flip-flop, Combinational table, Binary tree.*

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1. INTRODUCTION

Nowadays in VLSI design power is a major issues. In the maximum power was consumed by the clock used in integrated circuits. If power consumption is more it leads to issues in packaging, battery life ,over heating problem. There are many techniques to reduce the clock power in the integrated circuits. Optimization of power is based on the below techniques, power reduction during leakage power using optimization and dynamic run time[2].Power reduction during sleep and idle mode using novel energy recovery clocked flip-flops[4].We can also achieve power reduction through several techniques[3].Also there are several methodologies[6][7] for area reduction.

1.1 Multi-Bit Flip-Flops

Multi-Bit Flip-Flops are capable of reducing the power consumption because they have shared inverter inside the flip-flop. It also minimizes the clock skew at the same time. Both single and multi-bit flip-flop have the same clock condition and same set and reset condition. Fig. 1 shows the example of multi-bit flip-flops. By replacing the two 1-bit flip-flops as one 2-bit flip-flop it share the clock buffer based on that we can achieve the power reduction.

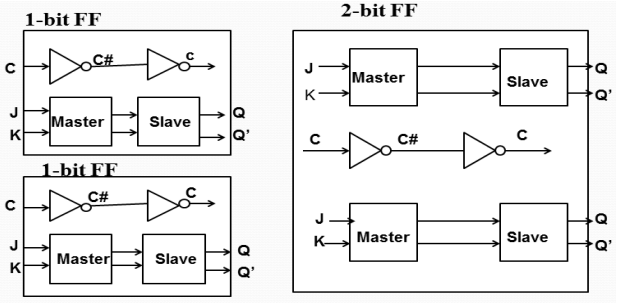

Fig-1 Example of merging two 1-bit JK flip-flop into one 2-bit JK flip-flop

Advantages of flip-flop
1. Avoid the duplicate inverters.
2. Total area contributing to flip-flop can be reduced.
3. Power optimization through shared invertors.

Based on the number of minimum size inverters that it can drive on a given rising or falling time we can calculate the driving capability of a clock buffer. Based on this shown in Fig.1 it share the clock buffer by replacing the two 1-bit flip-flop as one 2-bit flip-flop so it reduce the power consumption.

2. OUR ALGORITHM

Our algorithm is split into three stages as,First stage is to identify the merged flip-flops. In second stage we can build the combination table according to the identified overlapped region in the first stage. We can build the combination table in binary tree representation for easy representation. In the third stage, performing the merging flip-flops based on the combinational table.

2.1 Identifying Mergeable Flip-Flop

Identification of flip-flops used for mergeable is identified based on the flip-flops used in the digital circuits. During identifying the flip flops each have its separate clock.

2.2 Combinational Table

To perform the efficient process we build the combinational table. If without performing the combinational table we merged the flip-flops it will not be efficient because mergeable flip-flops is not in intersection value, it also time waste of designing. Building of combinational table is based on the library initialization value.

In combinational table we build possible combination of flip-flops based on library bit values. The initializations in algorithm are library is denoted as L, the combinational table

is denoted as T, ni denote the one combinational in T and b (ni) is denote the bit width. Maximum library size is initialized by library and minimum size is denoted as 1 bit because we are going merge the number of one bit flip-flops.

From the below example we can implement the six 1-bit flip-flops as one 6-bit flip-flops. We can implement the four 1-bit flip-flops in two ways as illustrated in Fig.2 and Fig.3 as,

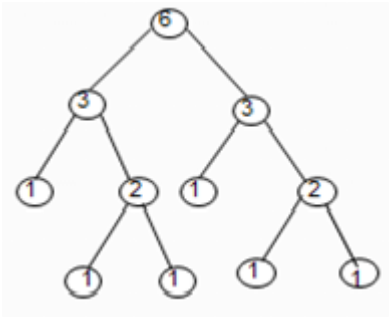

Fig-2 Efficient combination tree

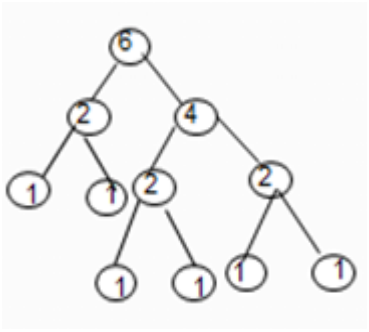

Fig-3 Inefficient Combination Tree

To represent the combination of flip-flops simple using the binary tree model. In the tree structure each node represents the one type of flip-flop. In the binary tree representation the summation of flip-flops in the leaves gives bit width of the root node. Since we need to consider only one combination of flip-flop at a time, it reduces the search time gradually.

Algorithm 1 Efficient combinational Table
InsertPseudoType (L):
1 for eachtypej in L do
2 PseudoTypeVerifyInsertion (typej, L) ;
PseudoTypeVerifyInsertion (typej, L):
1 if (mod (b(typej) /2) == 0)
2 b1 = [b(typej)/2], b2 = [b(typej)/2];
3 else
4 b1 = $\lfloor$ b(typej)/2$\rfloor$, b2 = b(typej) - $\lfloor$ b(typej)/2$\rfloor$;
5 for i = 1 to 2
6 if ((bi > bmin) &&
(L does not contain a type whose bit width is equal to bi))
7 insert a pseudo type typej with bit width bi to L;
8 Pseudo Type Verify Insertion (type j, L);

Based on the algorithm 1we can build the efficient combination table as shown in Fig.2. This algorithm gives as the equal representation of binary tree in both sides. So in increase the performance of the operation

2.3 Merging Flip Flop

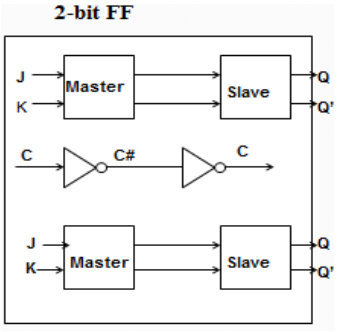

Fig-4 Merged two 1-bit flip-flops as one 2-bit flip-flop

Merged the flip-flops is based on the combinational table.After merging the flip-flops a single clock is shared by the number of flip-flops as shown in Fig.4.

4. EXPERIMENTAL RESULTS

This section shows the experimental results. We implemented our algorithm in VHDL language.various reductionas are shown here,Table-1 shows the area reduction for 12-bit flip-flops using the algorithm Delay reduction is when we merged flip-flop based on the algorithm.Table-3 shows the delay reduction and Table-4 shows the thermal reduction.

Table 1-Area Reduction For 12-Bit Flip-Flop

Specifications	**Seperate Clock**	**Merged Clock**
Number of bonded IOBs	26 out of 180 (14%)	24 out of 180 (13%)
IOB Flip Flops	12	12
Number of GCLKs	4 out of 4 (100%)	1 out of 4 (25%)
Number of GCLKIOBs	4 out of 4 (100%)	1 out of 4 (25%)
Total equivalent gate count for design	96	96
Additional JTAG gate count for IOBs	1,440	1,200
Peak Memory Usage	158 MB	155 MB

Table 2-Power Reduction Ratio

Specifications	Case 1	Case 2	Case 3	Case 4	Case 5
Flip-flop number	6	5	4	3	2
Total estimated power original (mW)	145	144	141	113	84
Total estimated power merged (mW)	36	36	36	36	35
Total estimated Power Reduction ratio(%)	75.17	75	74.46	68.14	58.33
Total estimated clock power original(mW)	108	108	107	80	53
Total estimated clock power merged(mW)	28	28	27	27	27
Total estimated clock power Reduction ratio(%)	74.07	74.07	74.76	66.25	49.05

Clock power reduction as well as the total power estimated also reduced through merged flip-flops.shown in Table-2. Power reduction ratio is calculated based on the following equations,

Power reduction ratio(%)=(power original-power merged/power original)*100(%)

Based on the power reduction ratio power reduction are achieved shows in Table 4

Table 3-Delay Reduction For 12-Bit Flip-Flop

Specifications	Separate Clock	Merged Clock
Average Connection Delay	1.102 nsec	0.634 nsec
Maximum Pin Delay	4.348 nsec	1.410 nsec
Average Connection Delay On The 10 Worst Nets	1.724 nsec	0.944 nsec
Peak Memory Usage	129 MB	123 MB

Table 4-Thermal Reduction For 12-Bit Flip-Flop

Specifications	Separate Clock	Merged Clock
Estimated junction temperature	29 c	26 c
Ambient temperature	25 c	25 c
Case temperature	29 c	26 c

5. CONCLUSIONS

This paper we achieve the power reduction through merged flip-flop by reducing the clock power. Clock power reduction is achieve based on the merging flip-flops using combinational table. Based on the algorithm the experimental results shows achievement of that power reduction, the thermal reduction, delay reduction as well as power reduction as 75%.

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BIOGRAPHIE

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