NOVEL FPGA DESIGN AND IMPLEMENTATION OF DIGITAL UP CONVERTER

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Abstract

In our world, communication systems play an important role in day to day life. In wireless and wired communication systems, signals are to be upsampled at the transmitter. Digital up converter (DUC) is a sample rate conversion technique which is widely used to increase the sampling rate of an input signal. The digital up converter converts low sampled digital baseband signal to a pass band signal. In this paper, we are going to design and implement a low noise digital up converter on a FPGA (Field Programmable Gate Array). In digital up converter, the input signal is filtered and converted to higher sampling rate and then it is modulated with the carrier signal generated from the direct digital synthesizer (DDS). This system consists of a cascaded integrator comb (CIC) interpolation filter, cascaded integrator comb compensation filter, multiplier and a direct digital synthesizer. The cascaded integrator comb interpolation filter performs upsampling of the input signal and the cascaded integrator comb compensation filter is used to compensate the losses of CIC filter by filtering the input signal. The multiplier is used for multiplying the upsampled signal from CIC filter with the carrier signal generated from DDS and gives the DUC output. In this DUC, the input signal is upsampled at the rate of eight. Here, two digital up converters are used and connected with an adder in order to obtain a low noise output signal. The coding of this work is done in VHDL. The simulation and functional verification is carried out using Xilinx ISE and FPGA implementation is carried out using Virtex 5.

Keywords: *Digital Up Converter, Cascade Integrator Comb Filter, Field Programmable Gate Array, Direct Digital Synthesizer.*

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1. INTRODUCTION

The digital up converter (DUC) is a device which converts digital baseband signal to a pass band signal [8]. The input signal is sampled at a relatively low sampling rate. This baseband signal is filtered and converted to a higher sampling rate and then modulated with a carrier signal generated from the direct digitally synthesizer (DDS) [9]. The DUC can be extensively used in wireless and wire line communication systems. A DUC system consists of a Cascaded Integrator Comb (CIC) interpolation filter, CIC compensation filter, multiplier and a direct digital synthesizer. The input signal is first fed to CIC compensation filter for filtering input signal, then it is given to CIC filter for upsampling the filtered signal and finally it is multiplied with the carrier signal generated by DDS [8].

In the CIC compensation filter, the programmable finite impulse response (PFIR) filter and the compensation filter is present. The PFIR filter is used for pulse shaping the input signal and upsample the input signal by factor two [9]. Compensation filter is also type of finite impulse response (FIR) filter used to compensate for loses in cascaded integrator comb (CIC) filter [7]. A CIC compensation filter is used to provide ideal pass band and narrow transition region for the input signal and upsample the input signal by factor two [7]. After filtering, signal is fed to CIC interpolation filter for larger upsampling. Here, CIC interpolation filter will upsamples the signal by factor four. The DDS is used for generating carrier signal and the multiplier is used for multiplying upsampled signal with carrier signal [9]. The upsampled signal is given to multiplier. The multiplier multiplies upsampled signal with carrier signal generated from DDS and gives DUC output. In this paper, two digital up converters are used and they are connected with an adder. This is performed in order to produce a low noise output signal. Then this system is implemented on Virtex 5.

2. METHODOLOGY

The block diagram of digital up converter (DUC) is shown in the figure1. A DUC system consists of a Cascaded Integrator Comb (CIC) interpolation filter, CIC compensation filter, multiplier and a direct digital synthesizer. These blocks are described as following.

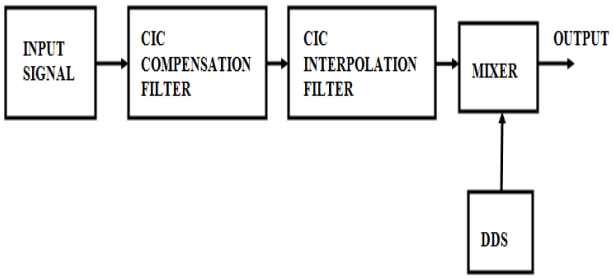

Fig-1: Block Diagram of Digital Up Converter

2.1 CIC Compensation Filter

The CIC compensation filter consists of programmable finite impulse response (PFIR) filter and the compensation filter. The PFIR filter provides pulse shaping the input signal and upsample the input signal by factor two. The pulse shaped input signal will given to compensation filter. Compensation filter is just a FIR filter which is used to in order compensate the losses of CIC filter. A CIC compensation filter provides ideal pass band and narrow transition region for the input signal. These properties are not provided by the CIC filters. After filtering, compensation filter upsample the input signal by factor two.

2.2 CIC Interpolation Filter

Cascaded Integrator Comb (CIC) filter is first introduced by Eugene Hogenauer. Hence these filters are also called Hogenauer filters. CIC filter consists of N number of cascaded combs and integrator sections. The main advantage of this filter is it does not use any multipliers. This filter consists of only adders, subtractors and registers. Hence they are typically employed in applications that have a large excess sample rate. The CIC filter consists of two types. They are interpolating CIC filter and decimating CIC filer. The interpolating CIC filter is used for upsampling the input signal and the decimating CIC filter is used for down-sampling the input signal. Unlike FIR filters, the decimator or interpolator can be built into the CIC filter architecture.

Cascaded Integrator Comb (CIC) interpolating filter can be widely used for up-sampling the input signal in digital up converter. In the case of interpolating CIC filter, cascaded comb sections comes first, then an up-sampler and followed by integrator sections. The detailed structure of a CIC interpolator filter is shown on figure 2. In this work, the CIC filter upsamples the filtered signal at the rate of four.

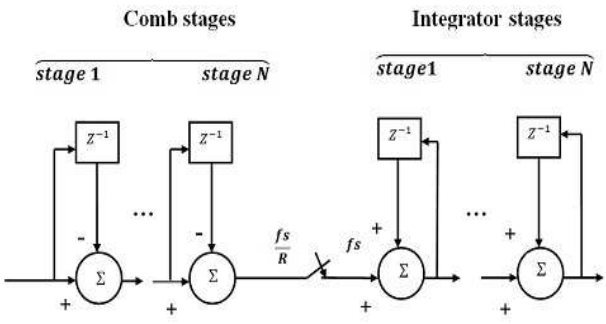

Fig- 2: Structure of CIC Interpolator Filter

2.2.1 Comb

The each comb filter consists of a delay element and a subtractor. The detailed structure of a comb filter is shown on figure 3.

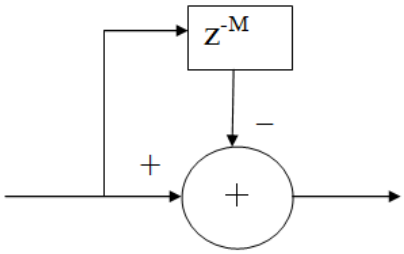

Fig-3: Structure of a comb filter

A comb filters with a sampling rate fs/R and has a rate change of R can be described by

$$y(n) = x(n) - x(n - RM)$$

Where M is the differential delay

After taking z transform

$$y(z) = x(z) - z^{-RM}x(z)$$

$$y(z) = x(z)[1 - z^{-RM}]$$

Then transfer function for comb filter at fs is given by

$$HC(z) = \frac{y(z)}{x(z)} = [1 - z^{-RM}]$$

2.2.2 Integrator

The each integrator filter consists of a delay element and an adder. The detailed structure of a integrator filter is shown on figure 4

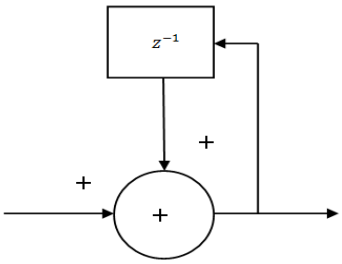

Fig- 4: Structure of an Integrator Filter

Here, $y(n) = y(n-1) + x(n)$

After taking z transform

$$y(z) = z^{-1}y(z) + x(z)$$

$$x(z) = y(z)(1 - z^{-1})$$

The corresponding transfer function for integrator is given by

$$HI(z) = \frac{y(z)}{x(z)} = \frac{1}{(1 - z^{-1})}$$

Then transfer function for a CIC filter at fs is given by

$$H(z) = \frac{(1 - z^{-RM})^N}{(1 - z^{-1})^N}$$

2.3 DDS and Multiplier

Direct digital synthesizer (DDS) is used to generate a carrier signal in order to modulate with the upsampled signal. Here, multiplier is used for modulating upsampled signal with the carrier signal and gives the DUC output. Then two digital up converters are connected with a ripple carry adder in order to obtain a low noise output signal.

3. RESULTS

The simulation and functional verification of this work is done in Xilinx ISE and the FPGA implementation is carried on virtex 5. The figure 5 shows the design summary of this work. For this design, number of slice registers used is 23%, number of slice look up tables used is 21%, number of flip flops used is 11% and number of input output bounds used is 11%.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	2946	12480	23%
Number of Slice LUTs	2729	12480	21%
Number of fully used LUT-FF pairs	606	5069	11%
Number of bonded IOBs	19	172	11%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig- 5: Design summary

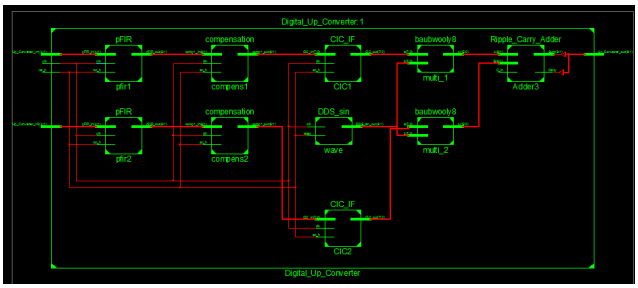

Fig- 6: RTL schematic view of this work

The figure 6 shows the RTL schematic view of this work. Here in this design in order to obtain a low noise output signal, two digital up converters are connected with a ripple carry adder. The figure 7 shows the output of the low noise digital up converter.

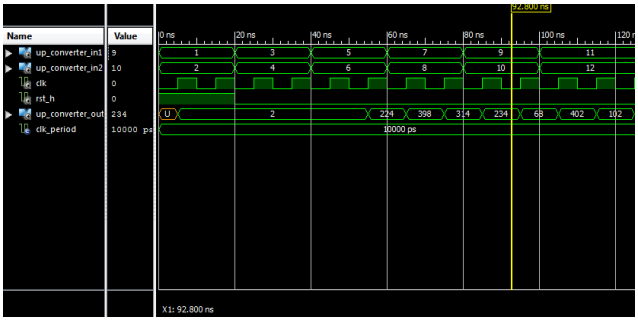

Fig- 7: Output of DUC

4. CONCLUSIONS

This paper deals with novel FPGA design and implementation of digital up converter. By this design, we successfully designed a digital up converter and then it is implemented on a FPGA. The coding of each block is done in VHDL. The outputs of each blocks is simulated and synthesized in Xilinx ISE. The FPGA implementation of this design is done in virtex 5.

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BIOGRAPHIES

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