CLOCK-GATED AND ENABLE-CONTROLLED 64-BIT ALU ARCHITECTURE FOR LOW-POWER APPLICATIONS

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Abstract

The Arithmetic Logic Unit (ALU) design is very important in any Integrated Circuit based processing system. An ALU is also called the brain of any computing system. The Arithmetic operation and Logic operations are processed by ALU to serve the execution of hardware computing. In the proposed design a 64-bit ALU with clock gating is implemented on FPGA for low power and high speed applications. A low power consuming system offers the benefits like device portability, long battery life, good performance criteria, etc. To achieve low power operational performance various techniques have been proposed in previous works. Modification of hardware design provides the desired low power feature up to some extent of desired performance. The power consumption can also be affected by controlling the duration of the operation of the circuit. The circuit enable control logic provides transition signals to the operational circuit only for the duration until the results are calculated by the circuit. Once the results are generated the circuit activity is disabled. This saves the power consumption during the extra clock operations that is used after the generation of result by the circuit in the signal transition by the intermediate circuit. The Clock gating reduces power by controlling the clock signal activity that in turn controls the transition of logic values in the sub-blocks of the ALU. The power required in the undesired transitions is thus saved. The proposed design is implemented and simulated on Xilinx XC3S500E FPGA and its software simulation is performed on Xilinx ISE Test-bench Simulator.

***Keywords**: ALU, Clock Gating, Dynamic Power, FPGA, Opcode, Operand, Xilinx ISE etc.*

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1. INTRODUCTION

The basis requirement of any Integrated Circuit based system is high speed and low power processing of the signals to perform the desired execution. Clock-Gating provides a better solution to achieve low power performance. E. Arbel, C, Eisner and O. Rokhlenko [1] propose a low power technique used as post-processing phase in intelligent clock-gating. T. Lam, X. Yang. W. C. Tang and Y. L. Wu [2] shows valid clock gating, observability don't care based clock gating, and Idle state based clock gating techniques. J. Shinde and S. S. Salankar [3] propose latch-free clock gating, latch based clock gating and flip-flop based clock-gating techniques. M. P. Dev, D. Baghel, B. Pandey, M. Pattanaik and A. Shukla [4] shows summary of comparison between various clock-gating techniques. P. Pandey and M. Pattanaik [5] propose a Clock-gating Aware Low power ALU. Ramalatha, M.Dayalan, K D Dharani, P Priya, and S Deoborah [6] propose high speed Energy Efficient ALU architecture.

The Arithmatic Logic Unit is the main operational block of any operational / processing control system. It is also called the brain of the control / processing system. An ALU basically performs the arithmetic and logic operations like subtraction, addition, multiplication, modulus calculation, increment, decrement, AND, OR, NAND, NOR, XOR, rotate, logical shift, 1's complement, 2's complement, etc.

2. ALU ARCHITECTURE IN PROPOSED DESIGN

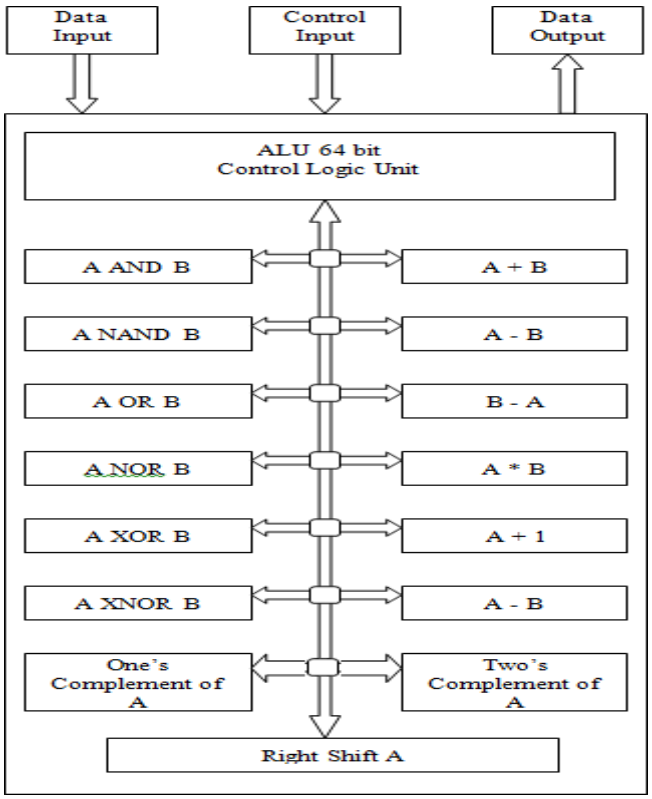

Fig -1: RTL Block of Proposed ALU Design

The ALU generally consists of basic building blocks as AND gate, OR gate, inverters, flip-flops, multiplexers and registers for various arithmetic and logical operation execution and control. A dedicated ALU operates on a fixed length of the input data. The performance of ALU is the main criteria to access the performance of any processing circuit or system. The utilization of different hardware units of ALU varies depending on the application of the system in which ALU is used as processing logic.

The architecture of ALU for performing logical operations requires logic gates as operational hardware. It is simple to design and control. Whereas, design of arithmetic operations are proposed by various researchers in different architectures to provide desired performance to the processing circuits. S. Venkateshwara Reddy [7] propose a ROM based multiplier. Vaijyanath Kunchigi, Linganagouda Kulkarni and Subhash Kulkarni [8] propose a Multiply and Accumulate Architecture for multiplier design. P. Saha, A. Banerjee, A. Dandapat and P. Bhattacharyya [9] propose a Transistor Level Multiplier Design.

3. PROPOSED ALU DESIGN

Table -1: Proposed ALU Operations

Opcode Value	*Operation*
0000	NOP
0001	AND
0010	NAND
0011	OR
0100	NOR
0101	XOR
0110	XNOR
0111	Addition (A + B)
1000	Subtraction (A – B)
1001	Subtraction (B – A)
1010	Multiplication (A * B)
1011	Increment A
1100	Decrement A
1101	1's complement of A
1110	2's complement of A
1111	Shift A

Clock is one of the critical signal which runs throughout the entire circuit at each step, thus controlling the clock can be a great deal in low power consumption circuit[10]. In the proposed ALU design, the gated-clock signal is transferred to the logic circuit. The clock-gating is controlled using logic "Enable" input. Reset" input initializes all outputs and registers of the hardware to low logic values. An asynchronous "Reset" control is used in the design. A pulse enable control is used to perform the circuit operation. For a logic 'high' value of "Enable" input, the operational circuit will be active to perform the processing of input operand A and operand B. The operational circuit will go de-active after the generation of result of operation. The proposed design performs fifteen arithmetic and logic operations. The opcode used for the operation is summarized in Table 1.

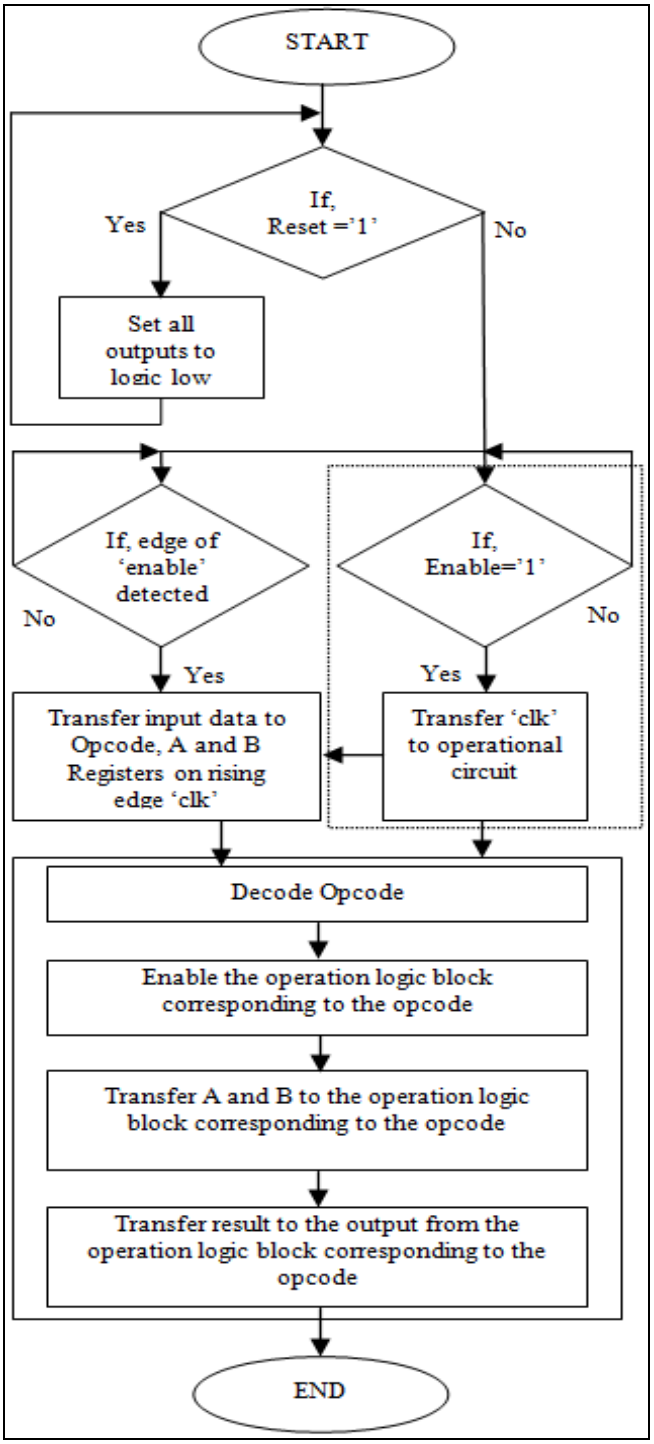

Fig -2: Logic Flow Chart of Proposed ALU Design

Operations are performed on 64-bit input operand values namely A and B. On the basis of the value of input opcode a particular operational logic block will be enabled to perform the logic operation. The output of the logic operation is transferred to the output signal register. The operation by the ALU is performed on the edge of the input clock signal. Once the result value is generated, the next operation can be initialized only when the "Enable" input is given a logic high value followed by a logic low value. The registers and output can be reset to logic low values at any time of operation.

4. CONCLUSION

The proposed logic is implemented using Verilog Hardware Description Language on Xilinx ISE Tool. The RTL block diagram of the design is shown in Fig. 3.

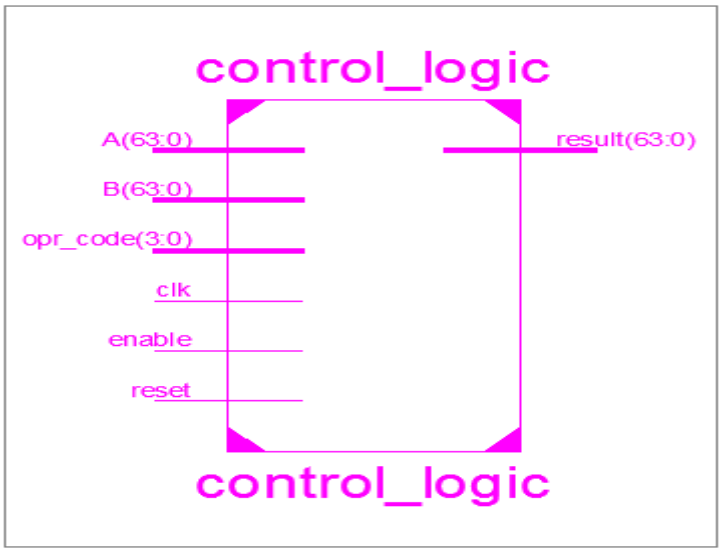

Fig -3: RTL Block of Proposed ALU Design

Proposed ALU design is simulated using VHDL Test Bench on Xilinx iSim Simulation Tool [11]. The Simulation Input-Output values are given in Table-2 and the waveform of input and result of the design are shown in Fig. 4 with following vector values of inputs and output.

Table -2: Simulation Input-Output Values

Literal Name	***Direction***	***Value***
Opcode	Input	4'b0111 (Addition Operation)
Operand A	Input	64'h4400000000004321
Operand B	Input	64'h3300000000001234
Reset	Input	1'b0
Enable	Input	1'b1
Result	Output	64'h7700000000005555

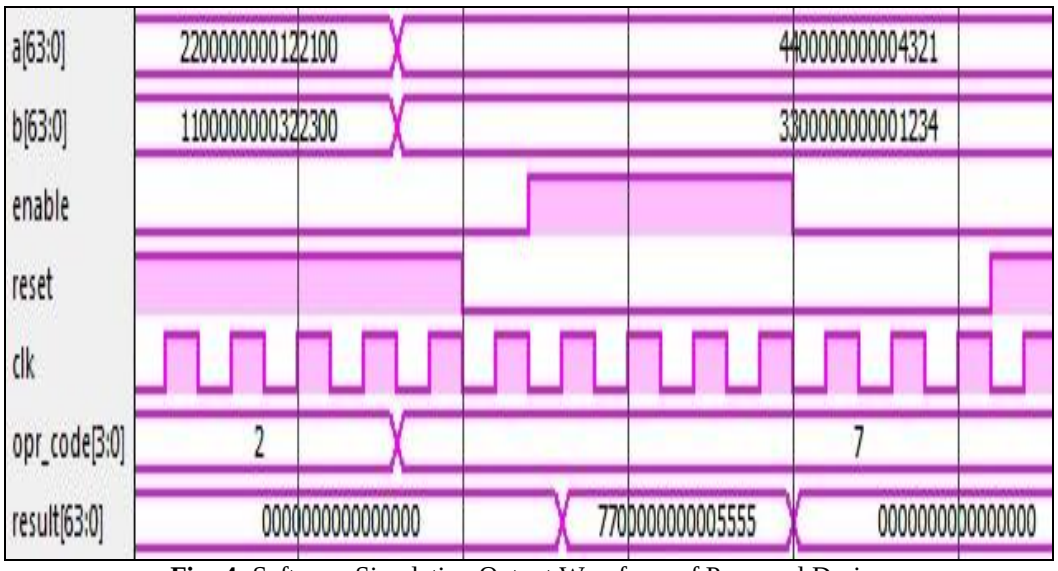

Fig -4: Software Simulation Output Waveform of Proposed Design

The on-board available clock frequency is 50 MHz. The proposed design is simulated using X-Power tool of Xilinx ISE for power performance at various frequencies. The Summary of Dynamic Power consumption versus Operational Clock Frequency is summarized in Table-3.

Table -3: Clock Frequency Vs Dynamic Power Consumption

Frequency (MHz)	*Dynamic Power (Watt)*
500	0.395
600	0.474
700	0.553
800	0.632
900	0.711
1000	0.790
1100	0.869
1200	0.948
1300	1.027
1400	1.106
1500	1.186

Table -4: Hardware Resource Utilization Summary

Hardware Resource	*Available*	*Utilized*	*Utilization %*
Slices	4656	982	21
Slice Flipflops	9312	135	1
4-input LUTs	9312	1796	19

The device that is used for implementing the design is Xilinx Spartan3 XC3S500-4PQ208 FPGA. The hardware resource utilization summary is presented in Table-4. An amount of 1% of available flip-flops of the FPGA is utilized by the proposed logic to implement the design circuit.

Table-5 shows a comparative reduction in power consumption of the proposed design with respect to the ratio of the amount of hardware flip-flop utilization.

Table -5: Dynamic Power and Hardware Resource Utilization Comparison Summary

	Proposed	*[4]*
Logic Design	64-bit ALU	16-bit Register
Device	XC3S500E	Virtex6
Slice Flipflops	135	16
Frequency (MHz)	1000	1000
Dynamic Power (Watt)	790	175

This design proposes a low-power FPGA implementation of 64-bit Arithmetic Logic Unit architecture using gated-clock and pulse enabled operation control logic. The design can be easily interfaced with the existing hardware logic designs. There is a scope for the improvement of the proposed design in future to meet the complex design demand for future applications.

ACKNOWLEDGMENTS

The authors wish to thank Manish Trivedi (HOD, Department of Electronics and Communication Engineering, RKDF IST, Bhopal, India) and Piyush Jain (Director ITDTC, Bhopal, India) for sharing technical ideas inline with the proposed work.

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