A REVIEW ON VARIOUS TYPES OF SOFTWARE DEFINED RADIOS (SDRS) IN RADIO COMMUNICATION

Vigneswara Rao Gannapathy[1], Ahamed Fayeez Bin Tuani Ibrahim[2], Zahriladha Bin Zakaria[3], Abdul Rani Bin Othman[4], Nur Qalbi Binti Jalaudin[5]

[1]*Lecturer, Faculty of Electronic & Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), 76100 Melaka, Malaysia*
[2]*Lecturer, Faculty of Electronic & Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), 76100 Melaka, Malaysia*
[3]*Lecturer, Faculty of Electronic & Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), 76100 Melaka, Malaysia*
[4]*Lecturer, Faculty of Electronic & Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), 76100 Melaka, Malaysia*
[5]*Student, Faculty of Electronic & Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), 76100 Melaka, Malaysia*

Abstract

Software Defined Radio (SDR) promises to deliver a cost effective and flexible solution by implementing a wide variety of wireless protocols in software. The SDR became more popular in recent years because of its abilities to realize many applications without a lot of efforts in the integration of different component. This software based radio device allows engineers to add more features to the communication system and implement any number of different signal processing elements or protocols without changing the original system hardware and its architecture. It provides a customizable and portable communications platform for many applications, including the prototyping and realization of wireless protocols and their performances. It is also able to interface with a separate hardware module to communicate over a real channel. In this article we described and compared the various SDRs that currently has been using by the researchers to study the performance of wireless protocol. Among the SDRs that we focused in this article are USRP, SORA, Air blue, SODA, and WARP.

Keywords: *Software Defined Radio, USRP, SORA, Air blue, SODA, WARP*

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1. INTRODUCTION

In 1992, Joseph Mitola proposed the basic concept of Software Defined Radio (SDR). SDR is the current radio communication which is implemented from the previous radio components, such as filters, modulation, de-modulation, detectors, amplifiers, and mixers in software[1]. The motherboard is placed between the daughter board (RF front-end) and host computer at both transmitter and receiver. ADC/DAC changes the data format from analogue to digital and vice versa. Field Programmable Gate Array (FPGA) is used to execute high bandwidth mathematical calculations such as decimation, modulation/demodulation, and digital down conversion, digital up conversion and interpolation signal processing process. The wired is used to transmit and receive data between motherboard and host computer [2]. The architecture of SDR at the receiver and transmitter are shown in Figure 1.

The programmable hardware SDR has three approaches such as embedded digital signal processors (DSPs), Field Programmable Gate Arrays (FPGAs) and General-Purpose Processor (GPP)[3].

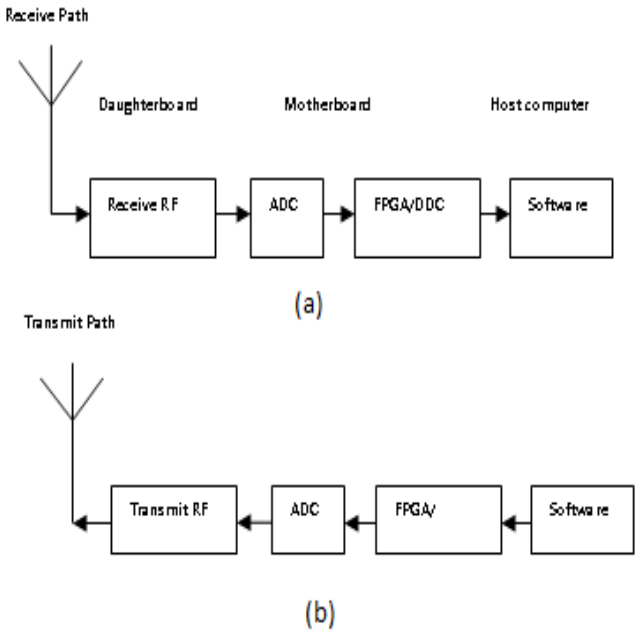

Fig -1: Basic SDR Architecture (a) Receiver (b) Transmitter

The specialized processor in SDR is called DSP. The processing of these signals is needed to extract the information from the signal and it represents the signals digital as a sequence of numbers or symbols. The basic operations of the processor include some processes such as filtering, transformations, modulation, correlation and convolution[4].

FPGAs are semiconductor devices which consist of logic components and interconnect that are both programmable. The element can be combined to perform simple gate level logic operations such as AND, XOR, etc. The advantages of the architecture of an FPGA allow the designs to perform multiple computational operations in parallel. Parallelism enable substantial data throughput at relatively low lock rates [5].

The GPP are designed for computers which is personal computer /workstation. It is easier to program the platform and makes it flexible. However, high energy consumption is needed to achieve the performance of objective [6].

Currently SDR can be used to implement simple radio modem technologies such as Global System for Mobile Communications (GSM), Wide band Code Division Multiple Access (WCDMA), WiMAX , Wi-Fi and others.

This paper reviews on the comparison between various types of Software Defined Radio such as SDR USRP, SDR SORA, SDR AirBlue, SDR SODA and SDR WARP. The SDR Universal Software Radio Peripheral (USRP) will be explained in section II, while section III will discuss about SDR Software Radio (SORA). Next, SDR AirBlue will be discussed in section IV, and SDR Signal Processing On-Demand Architecture (SODA) will be described in section V. Lastly, SDR Wireless open-Access Research Platform (WARP) is discussed in section V1.

2. SDR USRP

The USRP is proposed by Ettus Research [7]. USRP is flexible platform and low cost. The hardware for USRP it consists of ADC/DAC, FPGA and USB controller [2].

USRP1 consist an Altera Cyclone FPGA. This version provides 128 MS/s dual DAC, 64 MS/s dual ADC and it provides data to host processers. USB 2.0 connectivity is used in this peripheral [8].

USRP2 consist of a Xilinx Spartan 3-2000 FPGA. This version provides 400 MS/s dual DAC, 100 MS/s dual ADC and to provide data to host processers using Gigabit Ethernet interface [9].

In USRP N Series, there are two types which are USRP N200 and USRP N210. USRP N200 consist a Xilinx Spartan 3A DSP. This version provides 400 MS/s dual DAC, 100MS/s dual ADC and use Gigabit Ethernet interface offering data to host processors [10].

USRP N210 consist a Xilinx Spartan 3A DSP. This version provides 400 MS/s dual DAC, 100MS/s dual ADC and provides data to host processers by using Gigabit Ethernet interface[11]. USRP2 was no longer exist because it was not intended to replace the original USRP, which continue to be sold in parallel to the USRP2. It has been replaced USRP N200 and USRP N210. The comparison board resources between USRP1, USRP2, USRP N200 and USRP N210 are shown in Table 1 below:

Table 1: Comparison Board Resources between USRP1, USRP2, USRP N200 and USRP N210.

	USRP1	USRP 2	USRP N200	USRP N210
Interface	USB 2.0	Gigabit Ethernet	Gigabit Ethernet	Gigabit Ethernet
Total Host BW (MSPS 16b/8b)	8/*	16	50/100	50/100
Daughter card Slots	2	2	1	1
ADC Resolution	12	14	14	14
ADC Rate	64	100	100	100
DAC Resolution	14	16	16	16
DAC Rate	128	400	400	400
Internal GPS Disciplined Oscillator	No	No	Yes	Yes
1PPS/Ref Inputs	No	Yes	Yes	Yes

2.1 GNU Radio Toolkit

GNU Radio is suggested by Eric Blossom with a group of developing research and design team from A.D.2000. GNU radio is an open source project for SDR platforms [1]. It can be used for Radio Frequency (RF) real time applications. The signal processing is written in C++. The major application program offers the flow and connects the blocks via Phyton. This application is always chosen because of its ease of programming and flexibility [2].

3. SDR SORA

The SORA project started as a 'blue-sky' research project in the Wireless and Networking Group at Microsoft Research Asia (Beijing, China). The architectures of SDR SORA contain both software and hardware [13].

In the SORA architecture at the hardware components are a new radio control board (RCB) with an interchangeable radio front-end (RF front-end). The contents of hardware element are Virtex-5 FPGA, PCIe-x8 interface and 256MB of DDR2 Synchronous Dynamic Random-Access Memory (SDRAM). The radio front-end is a hardware element which receives

and/or transmits radio signals through an antenna. RF front-end is proposed by Rice University which is capable of transmitting and receiving a 20MHzchannel at 2.4GHz or 5GHz [14].

The SORA software works in C, with some assembly for performance-critical processing. It offers necessary system services and programming support for implementing various wireless PHY and MAC protocols in a general-purpose operating systems[13].

4. SDR AIRBLUE

Air blue is developed by Nokia Inc. Airblue consists of a low-end Altera Cyclone III FPGA. The FPGA possess a direct connection to a 2.4GHz. The baseband modulation is 40MHz and the RF front-end is 20MHz. The host processor communicates using high-speed USB[15].

5. SDR SODA

SODA is proposed by ARM Ltd. It consists of four cores, each containing asymmetric dual pipelines which support scalar and 32 wide SIMD execution. The arithmetic units are customized for 16 bits while only a few ports are needed for the register files and software-controlled scratchpad memories [16].

SODA processing element (PE) has five main components which are: 1) a scalar pipeline for sequential operations. 2) a programmable DMA unit to transfer data between memories and interface with the outside system. 3) an address generation unit (AGU) pipeline for providing the addresses for local memory access. 4) two local scratch- pad for the SIMD pipeline and the scalar pipeline 5) a SIMD pipeline for supporting vector operations [17].

6. SDR WARP

This section will be discussed on SDR Wireless open-access Research Platform. It describes the architecture of SDR WARP and the key feature of SDR WARP includes FPGA board V1, FPGA board V2 and WARP V3. The key features of SDR WARP will be described briefly as in Table 2.

WARP is developed by RICE University research team [18] and distributed by Mango Communication. WARP is an extensible, scalable and programmable wireless tool [19]. It is able to transmit in the 2.4 GHz to 2.5 GHz and to 5.875 GHz range with up to a 40 MHz bandwidth. The central in a WARP node is the FPGA board. Xilinx FPGA which is located in the heart of the board provides all the node's processing resources. It consists of a Xilinx FPGA and it provides daughter card slots that are compatible with all current WARP daughter card [20].

WARP FPGA board hardware version 1.2 consists of a Xilinx Virtex-II Pro FPGA. This version provides 10/100 Ethernet interface that is suitable for real-time communication between the wired network and wireless environment. There are four daughter card slots in a regular WARP [21] .

WARP FPGA board hardware version 2.2 consists of a Xilinx Virtex-4 FPGA. It offers 10/100/1000 Ethernet interface that is suitable for real-time communication between the wired network and wireless environment. It provides daughter card slots that are compatible with all current WARP daughter cards [22].

The latest generation of WARP hardware is WARP V3 which consists of a Xilinx Virtex-6 [23]. It integrates a high performance FPGA, two flexible RF interfaces and multiple peripherals to facilitate rapid prototyping of custom wireless design. The comparison board resources between FPGA board V1, FPGA board V2 and WARP V3 are shown in Table 2 below:

Table 2: Comparison Board Resources between FPGA board V1, FPGA board V2 and WARP V3.

	FPGA Board V1	**FPGA Board V2**	**WARP V3**
Daughter Card Slots	✓ 4	✓ 4	✓ -
Memory	✓ Two 2MB ZBT SRAM	✓ Up to 2GB(DDR2 SO DIMM Slot)	✓ DDR3 SO-DIMM Slot
Ethernet	✓ One 10/100 interfaces	✓ One Gigabit(10/100/1000) interfaces ✓ Two Gigabit (1000 Base-T only) interfaces (via optional SFR modules)	✓ Two Gigabit interfaces

Multi Gigabit Transceivers	✓ 8HSSDC 2 ports (2 populated)	✓ 4HSSDC 2 Ports (Infiniband keyed) ✓ 2 SATA Ports (1 Host,1 Target) ✓ 2 SFP ports	✓ 2.4/5GHz transceiver(40MHz RF bandwidth) ✓ 12-bit 170 MSps DAcs,12-bit 100MSps ADCs
MGT Clocking	✓ One on board oscillator	✓ Flexible Design ✓ 3 on-board oscillators ✓ Daisy Chain support	✓ Dual-band PA(20 dBm, Tx power) ✓ Shared Clocking MIMO applications
UART	✓ One RS232 (DB-9M Port)	✓ One RS232 (DB-9M Port) ✓ One USB/UART interfaces (FT 232R Transceiver)	✓ FMC HPC expansion slot
User I/O	✓ 2 Seven Segment Displays ✓ 4 LEDs ✓ 16 Bit TTL I/O ✓ 5 Push Buttons	✓ 3 Seven Segment Displays ✓ 16 LEDs (6 Red/6 Green/4Yellow) ✓ 16 Bit TTL I/O ✓ 5 Push Buttons	✓ 2 Seven Segment Displays ✓ 12 LEDs ✓ 4 Push buttons ✓ 4 bit DIP switch ✓ USB-UART ✓ 16-bit 2.5v I/O header

The comparison board resources between Air Blue, SODA and WARP are shown in Table 3 below:

Table 3: Comparison Air Blue, SODA and WARP

Air Blue	SODA	WARP
✓ Is an FPGA based SDR platform. ✓ It observed importance of modularity in programming wireless protocols. ✓ It provides two features latency-insensitivity and data-driven control. ✓ Do not provide an efficient modularity design framework or specific support for programmability.	✓ The SIMD processor also been employed for SDR design to leverage the advantage of high-throughput processing. ✓ It provides programmability the massive data parallel computing model is not suitable for wireless PHY modules. ✓ The GPU based platforms are too power-hungry for SDR system.	✓ It can communicate with a host computer through Ethernet connections. ✓ The latest version of WARP equips a relatively powerful FPGA for signal processing. ✓ It also provide a higher processing capacity than software based SDR platforms.

The comparison board resources between USRP1, USRP N200, USRP N210 and SORA are shown in Table 4.

7. CONCLUSION

This article focused on the comparison of various types Software Defined Radios. Each of the architecture of SDR is discussed. It compares the performances of SDR in a wireless network. Based on the discussion of this article, SDR WARP V3 is the best choice because it integrates a high performance FPGA, two flexible RF interfaces and multiple peripherals facilitate rapid prototyping of custom wireless design. The advantage of SDR WARP, it is able to achieve the high symbol rates while execute all the signal processing inside the FPGA. The GNU Radio software can configure the USRP easily and ease to do programming. The drawback of GNU Radio is that it does not support 802.11 because of slow data transfer among the USB port to a personal computer.

Table 4: Comparison USRP1, USRP N200, USRP N210 and SORA.

USRP1	USRP N200	USRP N210	SORA
✓ Provides entry- level RF processing capability. ✓ Provides software defined radio development capability for cost-sensitive users and applications. ✓ Support two complete RF daughterboard ✓ Requires high isolation between transmit and receive chains or dual-band dual transmit/receive operation. ✓ Stream up to 8MS/s to and from host applications, users can implement custom functions in the FPGA fabric. ✓ Use USB 2.0 to provide data to host processers.	✓ Provides high bandwidth, high dynamic range processing capability. ✓ Stream up to 50MS/s to and from host applications and users can implement custom functions in the FPGA fabric, or in the on-board 32-bit RISC soft-core. ✓ Offers the potential to process up to 100MHz of RF bandwidth in both transmit and receive directions. ✓ Provides data to host processers using Gigabit Ethernet.	✓ Provides high bandwidth, high dynamic range processing capability. ✓ Provides a larger FPGA than USRP N200. ✓ FPGA offers the potential to process up to 100MS/s in both transmit and receive directions. ✓ Use Gigabit Ethernet to provide data to host processers.	✓ Is a software-dominant SDR platform high-end multi-core machines running the windows OS, with a special hardware aid in timing-intensive components ✓ The data rate requirement for 802.11a/g is 54Mbps. ✓ Does not fully guarantee the tight timing/real time requirement of the MAC layer in WiFi standards. ✓ Requires partitioning, mapping and balancing of sub-tasks. ✓ It needs special skill in programming

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BIOGRAPHIES

Engr. Vigneswara Rao Gannapathy currently serving as a lecturer in Universiti Teknikal Malaysia Melaka (UTeM) and he actively involves in research activities which is related to electronics and wireless networking. His research direction has focused on Wireless Mesh Networks which emerged as a key technology for next-generation wireless networking

Ahamed Fayeez B Tuani Ibrahim, a Masters holder in Electronics & Telecommunication, is a vivid computer networking enthusiast. His specific research interest includes low power network design and programming. He is a certified Cisco Network Analyst.

Dr. Zahriladha Zakaria, PhD, MIEEE, BEM, Grad IEM is currently working as a lecturer at the Faculty of Electronic and Computer Engineering, University Teknikal Malaysia Melaka. (UTeM). His research interests include a variety of microwave device development such as planar and non-planar microwave filters, amplifiers and antennas.

Associate Professor Dr. Abdul Rani Othman, PhD, is currently working as lecturer at the Faculty of Electronic and Computer Engineering, University Teknikal Malaysia Melaka. (UTeM). His research interests include a variety of microwave device development, radio wave propagation, amplifiers and antennas.