ECG BASED HEART RATE MONITORING SYSTEM IMPLEMENTATION USING FPGA FOR LOW POWER DEVICES AND APPLICATIONS

Neha Joshi[1], Preet Jain[2]

[1]Department of Electronics and Communication Engineering, S.V.I.T.S, Indore, Madhya Pradesh, India
[2]Department of Electronics and Communication Engineering, S.V.I.T.S, Indore, Madhya Pradesh, India

Abstract

This paper proposes a new design to monitor the Heart Rate from Electrocardiogram (ECG) signal. The proposed design is based on the concept of identifying the voltage level of the R-wave complex component of the ECG signal above a threshold level. A 100 Hertz sample rate is selected to sample the complex ECG signal. A dual-counter based calculation method is used to obtain the mathematical value of Heart Rate. The proposed FPGA based ECG Heart Rate monitoring system can operate with high performance with respect to the low-power and high speed. The system is designed using Verilog hardware design language and Xilinx XC3s500E FPGA.

***Keywords**- ECG, Sampling, Threshold, Heart Rate, FPGA*

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1. INTRODUCTION

The basis method of monitoring the cardiovascular (CV) health of a person can be performed by observing the Heartbeat of that person. The fundamental device used to monitor heartbeat is Electrocardiogram (ECG). An ECG monitoring system involves a sensor to sense the small signals produced by the flow of blood in the human body and implementing a transducer to convert the signal equivalent in terms of electrical signal to make it easy to process with the help of electronic system.

Several time domain and frequency domain heartbeat detection techniques have already been proposed in previous works like pattern recognition [1], using auto-correlation [2], [3], [4], observing impedance plethysmogram (IPG) [5], [6], ballistocardiogram [7], Heartrate turbulence using Mean Shape Information [8]. ECG monitoring also provide information regarding various human body behavior by identifying ECG wave complex features like Automatic QT Detector [9], QRS detection using wavelet transform [10], Pan & Tompkins QRS Detector [11].

The ECG signal is a continuous varying signal. When observed using a sensor to convert it into an electrical equivalent signal it gives a very small variation in terms of voltage. So it is first amplified using precise amplifiers. In these stages of signal acquisition and amplification, various noise signals are added in the amplified signal. To extract various required information from this signal a very accurate system design is required. In this work a heartbeat detector design is proposed for an amplified electrical ECG signal. The basic observation of a person's health can be observed by calculating the occurrence of heart beats in one minute. This is also called heart rate (HR).

2. ELECTROCARDIOGRAM

The ECG signal that is observed from a human body is a complex continuous wave. The complete wave can be classified in various wave components. A simplified representation of ECG signal is shown in fig. 1. An overview of a general classification of an ECG signal is also shown in fig. 1. The analysis of various complex components of the ECG wave is used to identify the symptoms related to various cardiovascular diseases.

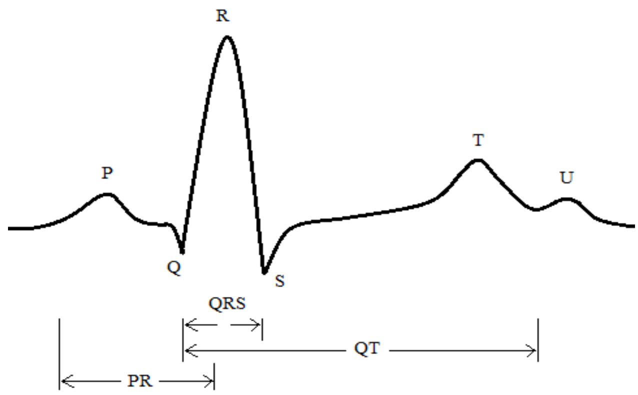

Fig. 1: ECG Signal: Wave Component Classification

When continuously observed, an ECG wave does not have a standard or a fixed voltage variation profile. The Heart Rate of an ECG wave can be calculated by considering any observable component of the wave as all the component are repetitive in nature. In a continuous wave with multiple occurrence of a particular point in time domain, if the occurrence of a particular point is marked and joined using a curvilinear path then the trajectory of that particular point can be obtained.

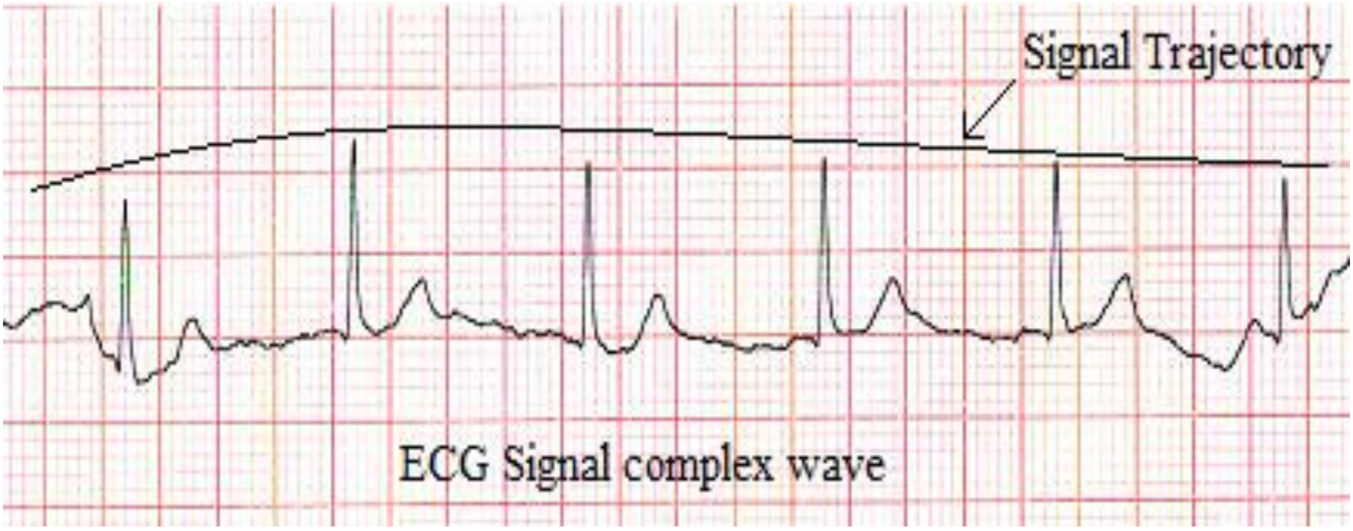

Fig. 2: Trajectory Complex ECG wave

The trajectory shown in the fig. 2 is with respect to the peak value of QRS complex component.

3. PROPOSED METHOD

3.1 ECG Signal Sampling

In the proposed method, an amplified ECG analog signal is sampled to receive its 8-bit binary equivalent. The sampling frequency is kept constant at 100 hertz. The complete range of the variation of the ECG signal variation is divided in 32 discrete levels for the ease of calculation using hardware design implementation.

A threshold value of voltage is selected which is more than the trajectory of the peak of the T-wave component and less than the trajectory of the peak of the R-wave component. Table-1 shows the various observed values of the R-peak and T-peak.

Table.1. Peak-T and Peak-R level observation

Peak-T and Peak-R level observation Table				
Observation Number	**Level of Peak-T**	**Level of Peak-R**	**Maximum Level of Peak-T**	**Minimum Level of Peak-R**
1	10	21	14	21
2	12	24		
3	14	26		
4	14	26		
5	12	24		
6	10	22		
7	11	23		
8	13	25		
9	12	24		
10	10	22		

3.2 Threshold Comparison

All observed values of Peak-T and Peak-R are represented in equivalent decimal value of one of the 32 discrete value of the complete variation range of the ECG signal. The level between the maximum level of Peak-T and minimum level of Peak-R, as per observation, is level-17 or level-18. In the proposed work level-18 is considered as the threshold level. This level is approximate to 56% of the total variation of the ECG signal. This is shown in fig. 3. Here, the selected value of threshold has approximately 10% of the total signal range variation as tolerance to compensate the variations in the trajectory of the minimum value of observed Peak-R and maximum value of observed Peak-T values.

The ECG input value when compared with the threshold value, will give a logic output ‘high’ value for ECG value greater than threshold value, else logic output ‘low’.

Fig. 3: Input signal range and Threshold level for heart rate calculation

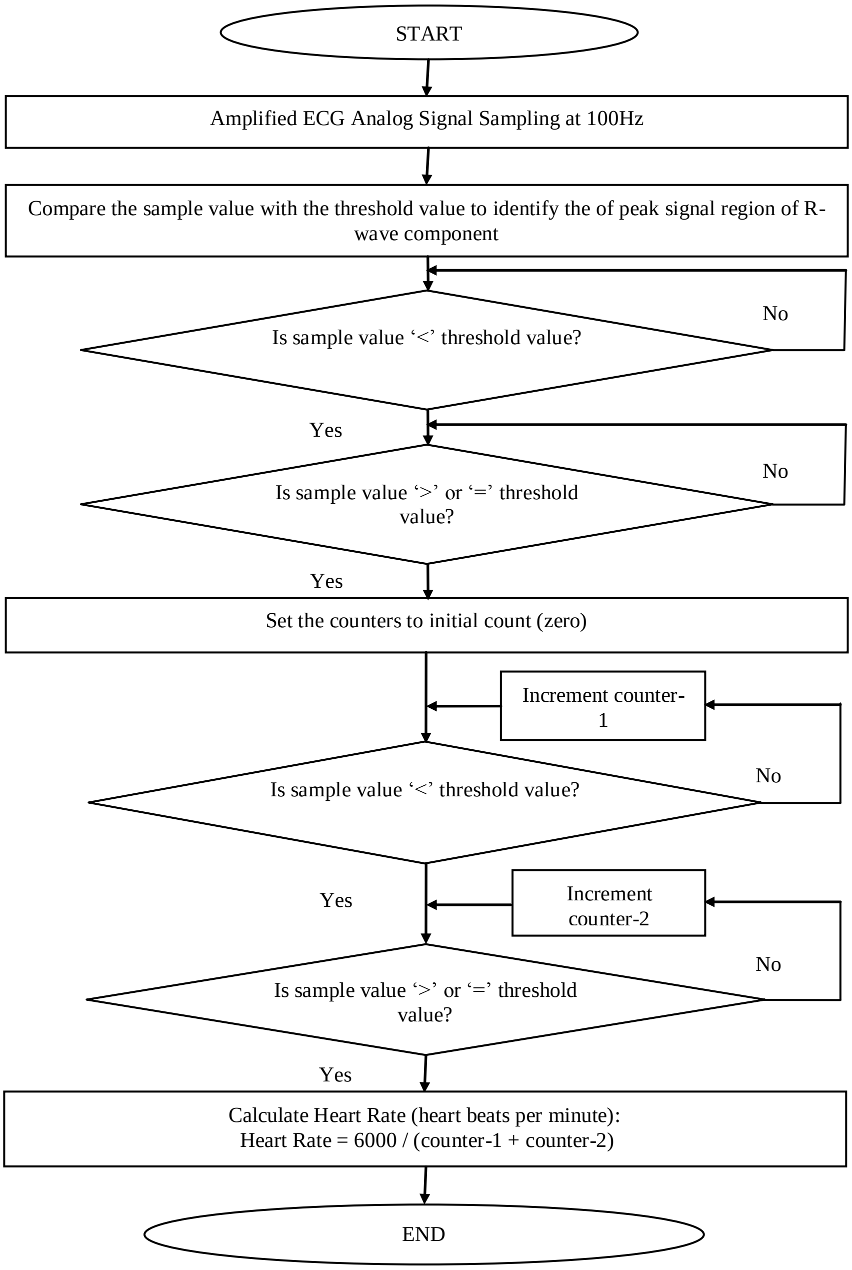

Fig. 4: Decision Flow Chart of ECG Monitoring System to calculate the Heart Rate

3.3 Heart Beat Duration Calculation

The design flow of the proposed work is shown in fig. 4. Here, after comparing the value of the ECG input signal with the threshold value, a conditional logic is used to identify the beginning of the wave component where the output of the threshold comparator is logic 'high'. This point on the ECG wave is identified as the starting point of the calculation of the heart rate.

The duration of one complete heart beat is the addition of the consecutive durations when the output of the threshold comparator is 'high' and 'low'. To calculate these time durations, a 100 hertz frequency is used for sampling the ECG analog signal. A counter is incremented on every sample for the duration when the output of the threshold comparator is logic 'high', referred in fig. 5 as 'counter1'. Another counter is incremented on every sample for the duration when the output of the threshold comparator is logic 'low', referred in fig. 5 as 'counter2'.

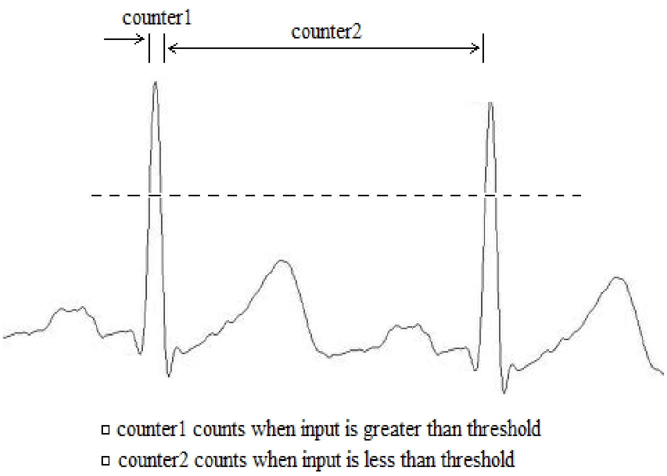

Fig. 5: counter1 and counter2 active regions in the complex ECG wave

3.4 Heart Rate Calculation

The time duration (in second) represented by counter1 is,

$$T1 = C1 / 100 \quad (1)$$

The time duration (in second) represented by counter2 is,

$$T2 = C2 / 100 \quad (2)$$

The time duration (in second) of the heart beat is,

$$T_{total} = (C1 + C2) / 100 \quad (3)$$

Where, C1 is the count value of counter1,
C2 is the count value of counter2.

Number of heart beats per minute (heart rate) is,

$$HR = (1 / T_{total}) \times 60 \quad (4)$$

4. CONCLUSION

The input ECG signals are used from MITBIH Arrhythmia database and generating using MATLAB to provide input to the design for simulation. The input is provided to analog-to-digital converter. The analog-to-digital converter is interfaced with the FPGA.

The device that is used for implementing the design is Xilinx Spartan3 XC3S500-4PQ208 FPGA. The hardware resource utilization summary is presented in Table. 2.

Table.2. Hardware Resource Utilization Summary

Hardware Resource Utilization Summary			
Hardware Resource	**Available**	**Utilized**	**Utilization %**
Slices	4656	568	12
Slice Flipflops	9312	293	3
4-input LUTs	9312	1068	11

This design proposes a low-power implementation design. The proposed design provides a low frequency solution of Heart Rate measurement techniques. The on-board available 50 MHz clock signal is reduced to a 100 Hz frequency signal for Simulation of the design. The hardware requires 11.336 ns time to process the data.

The design can be interfaced with the existing hardware designs. Future work can improve the proposed design by adding the features to detect and analyze ECG wave components by extending the algorithm.

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