IMPLEMENTATION OF LATCH TYPE SENSE AMPLIFIER

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Abstract

Sense amplifiers plays an important role in memories like Dynamic Random Access (DRAM) and Static Random Access (SRAM) for read and write operations. A sense amplifier compares the bit line voltage and its complement amplifies it to rail to rail output voltages. In this project, we mainly concentrated on the write operation. Sense amplifier is one of the peripheral circuits in memories that are placed in each column of the memory array. In this project, we discuss some of the sense amplifiers circuits and they are simulated in SPICE. An analytical model has been derived and simulated using 90nm CMOS technology with a supply voltage of 1.2v. When the input voltage difference of a sense amplifier is greater than the offset voltage (V_{OS}), the sense amplifier correctly detect the signal and amplifier it to correct logic levels. In an ideal case, the offset voltage of a sense amplifier is zero. Therefore, the sense amplifier can correctly sense the voltage present in the input bitlines, unless the differential bitline voltage is zero. Practically, the offset voltage is not zero because of the mismatch between the transistors. Hence, the differential bitline voltage must be greater than the offset voltage of the sense amplifier for correct sensing operation. Sensing delay, latching delay is one of the important factors in sense amplifier design. So the sense delay and latching delay of sense amplifier has been calculated for various supply voltages. Finally, the current mode sense amplifier has low sensing delay and latching delay compared to other latch type sense amplifiers.

Keywords: *Sense amplifier, DRAM, SRAM, SPICE, CMOS*

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1. INTRODUCTION

Sense amplifier plays an important role in the read operation of data stored on memory cells. It has two input bitlines (bl and blb). One of the bitline is used to read the data from particular memory cell while the other input bitline is used as a reference line. It senses the voltage from a bit line which represents a data bit (1 or 0) stored in a memory cell and amplify the small voltage swing to recognizable logic levels There is one sense amplifier for each column of memory cells. It is the only analog circuits on a digital memory chip. If the sense amplifier is not designed properly it may leads to undesired data output while reading the data in the memory. This work presents a several sense amplifiers using 90nm CMOS technology.

2. CONVENTIONAL SENSE AMPLIFIERS

2.1. NMOS Sense Amplifier

Sense amplifier is connected to a pair of bitlines. One is the output data from a particular cell, while the other is used as a reference line. When the voltage on a wordline (Wl) goes high, the transistor is attached to the wordline, connecting respective capacitor to the associated bitline. Then the capacitor discharges or shares its stored charge with the bitline. This charge sharing causes the voltage of the bitline either to increase or decrease. The sense amplifier senses this change and pulls the bitline voltage either to '1' or '0'. The sense amplifier which is made by using n-channel MOSFET is called as n-MOS sense amplifier. The technology used here is 90nm. The width of the n-channel MOSFET is 1um and the width of the p-channel MOSFET is 2um. The ratio of W/L is 10/1. The schematic diagram of n-MOS sense amplifier is shown in Fig.1

The charge or absence of charge on the capacitor (Cmbit) changes the voltage on the bitlines. Consider we are accessing (reading) the data in one of the cell in array 0. So, the sense amplifier sense the bitline from array 0 (bitline 0) and the bitline from array 1 (bitline 1) is used as a reference. The bitlines are precharged to half of the supply voltage (Vdd/2) before start sensing.

The bitlines have large number of capacitive loads. Because of large loads, the bitlines swing slowly. To reduce this delay, the bitlines are precharged to Vdd/2. Here equilibrate signal (Eq) is used to setting both the bitlines to Vdd/2. The data in the cell can be accessed by setting word line (Wl) line high, which turns on the Mn7. The storage capacitor (Cmbit) contains zero, so we reading out zero. So, the bitline 0 discharges from the precharged value. Evaluation of the bitline begins when sense_N is driven high, causing NLAT to go low. If the bitline0 fell from precharged value, the n-sense amplifier would pull the bitline 0 to low. The simulation result for reading out '0' using NMOS sense amplifier is shown in Fig.2

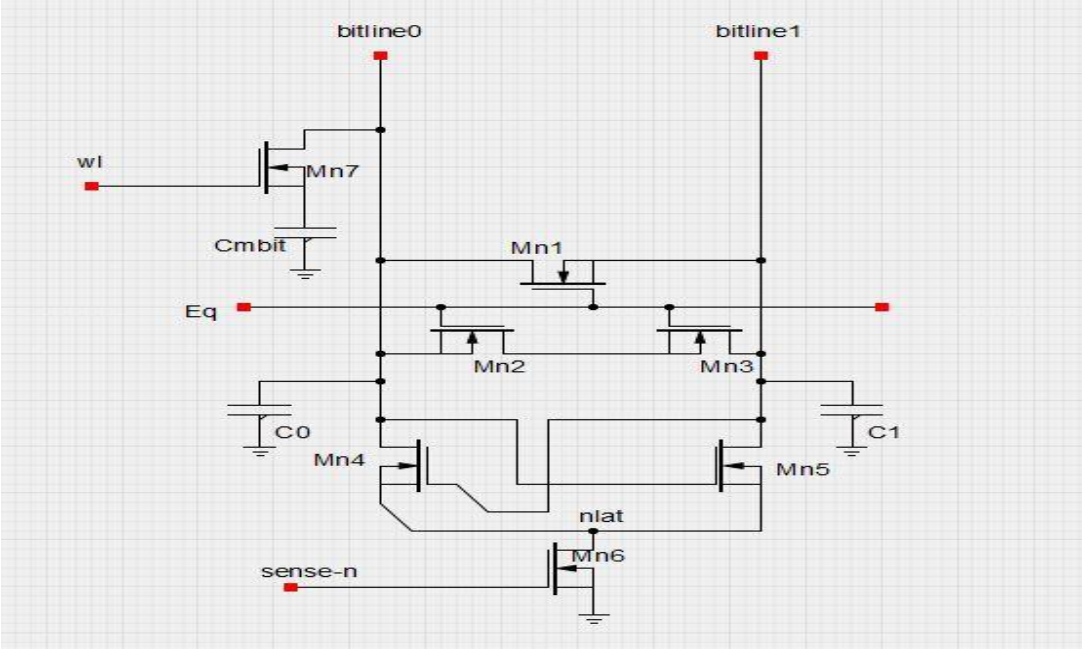

Fig 1: NMOS Sense Amplifier

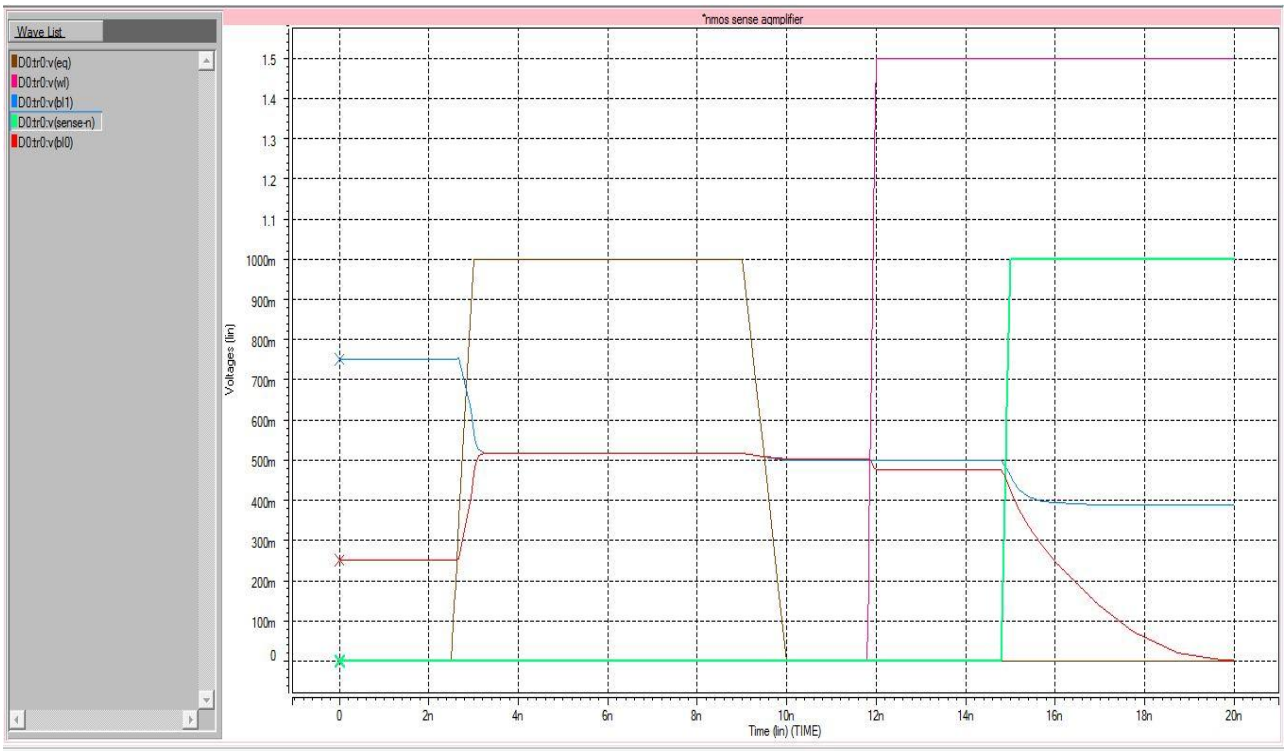

Fig 2: simulation result

If the memory cell contains high, the bitline 0 voltage increased from the precharged value. The nmos- sense amplifier would not pull the bitline 0 to high. So we need PMOS- sense amplifier to pull the bitline to Vdd while reading '1'.

2.2 PMOS Sense Amplifier

The sense amplifier which is made by using p-channel MOSFET is called as PMOS sense amplifier.The schematic diagram for PMOS sense amplifier is shown in Fig.3. P-mos sense amplifier can be fired by setting the sense-pbar signal to low. Similarly, Eq is used to precharge the bitlines. By setting the word line high, the Mn4 gets turns ON. Consider the cell contains '1', the capacitor (Cmbit) shares it charges with the bitline 0. This causes the bitline 0 voltage to increase from the precharged value.

The change in bitline 0 can be sensed by the PMOS sense amplifier and pull up the bitline 0 voltage to Vdd. The simulation result for reading out '1' using PMOS sense amplifier is shown in Fig.4.

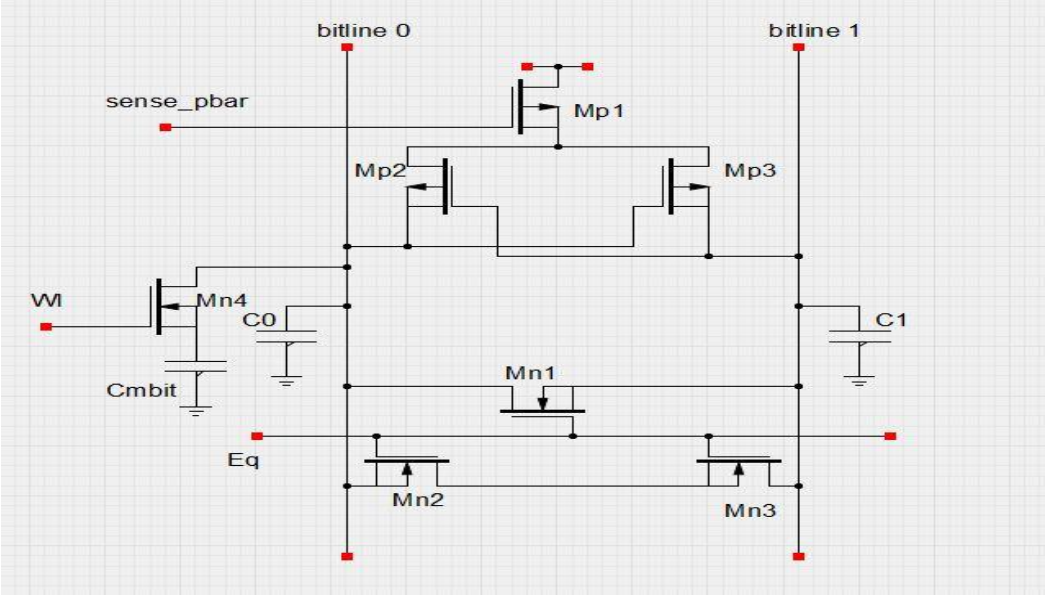

Fig 3: PMOS Sense Amplifier

The NMOS sense amplifier only pulls down the biltine voltage to zero but not pull up the bitline voltage to one. Similarly, the PMOS sense amplifier only pull up the bitline voltage to one but not pull down the bitline voltage to zero.

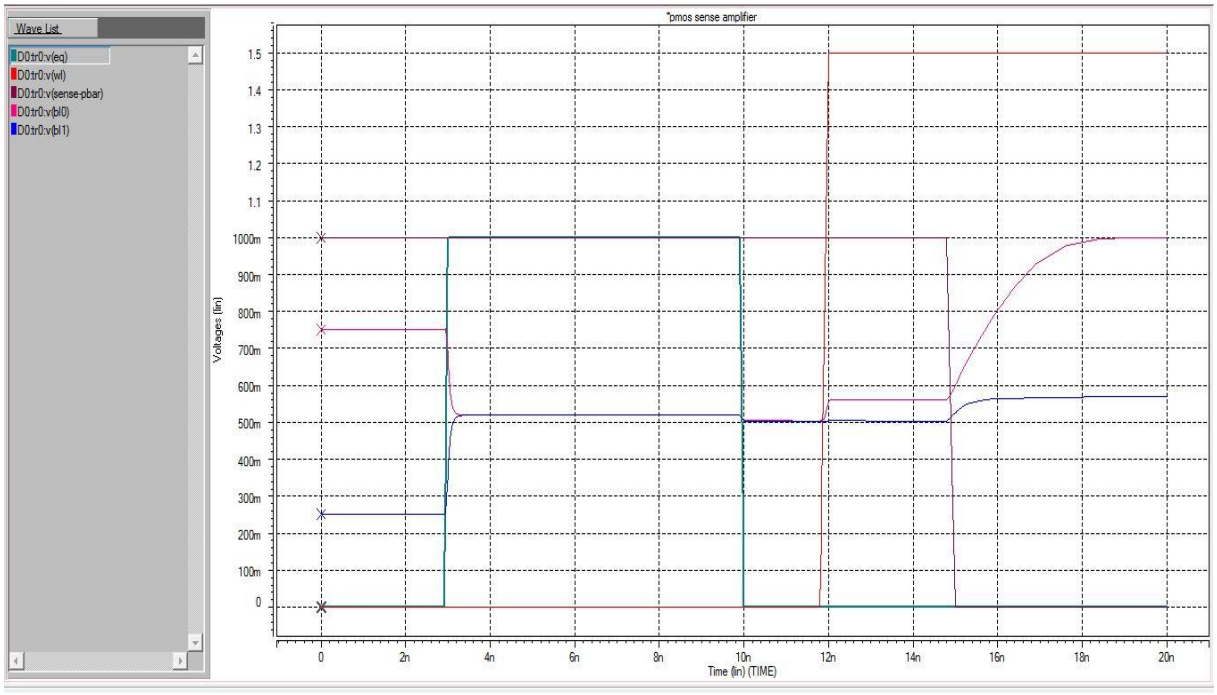

Fig 4: Simulation result

The sense amplifier which is made by using NMOS and PMOS sense amplifier is shown below. The bitlines are precharged to half of the supply voltage before start sensing.

The memory cell can be accessed by making word line (wl) voltage high. The schematic diagram for sense amplifier is shown in Fig. 5.

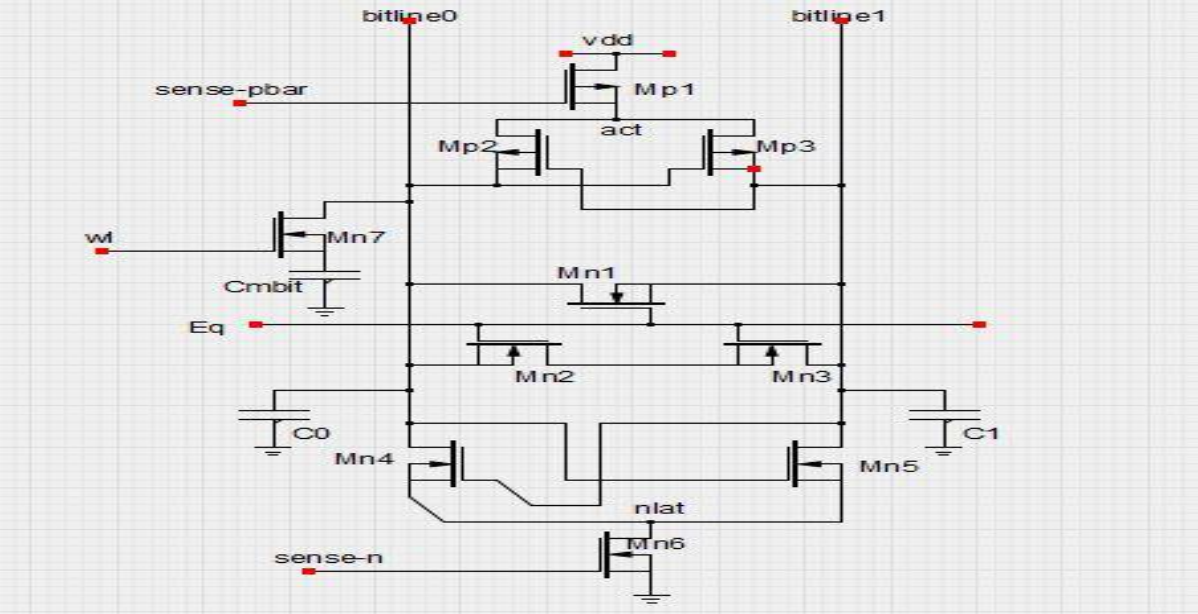

Fig 5: Sense Amplifier

When we accessing '0' in a memory cell, the voltage on the bitline 0 decreases. The sense-n fires the NMOS sense amplifier by making voltage high.

The sense-pbar fires the PMOS sense amplifier by making voltage low. The NMOS sense amplifier pull down the bitline 0 voltage to zero. The PMOS sense amplifier pulls up the bitline 1 voltage to one. The simulation result for reading out '0' using sense amplifier is shown in Fig.6

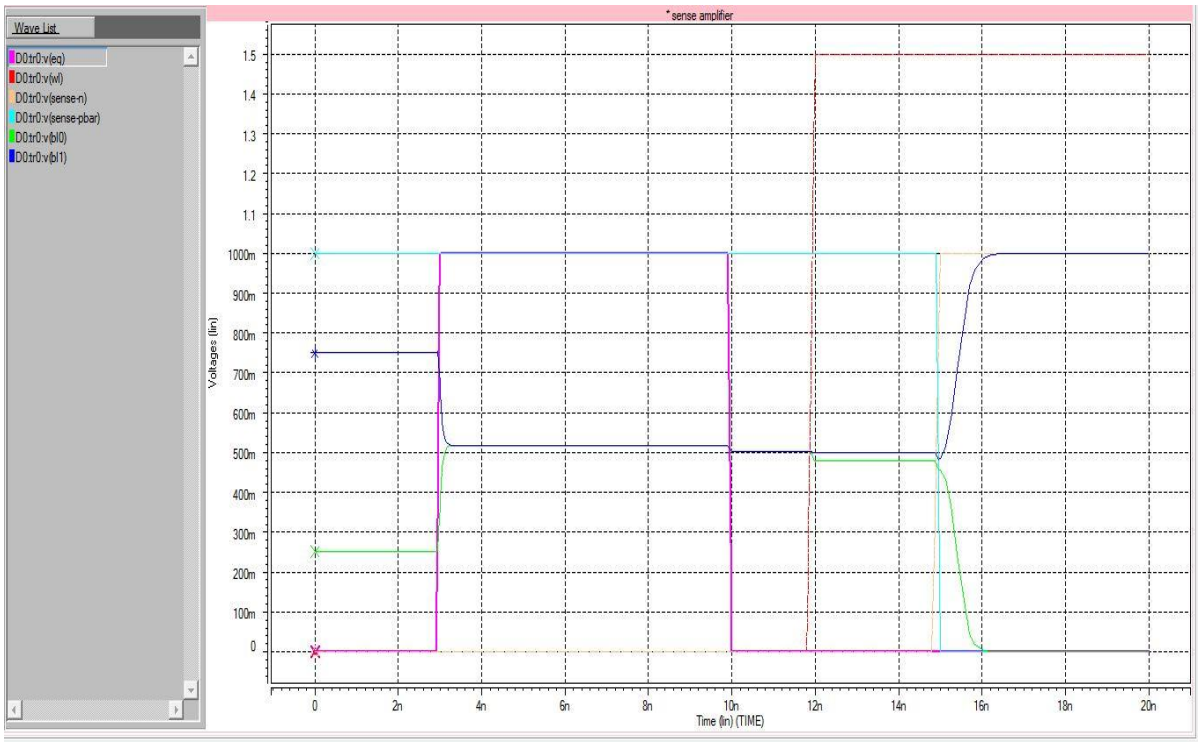

Fig 6: Simulation result

The simulation result for reading out '1' using sense amplifier is shown in Fig.7. This implies that the data stored in the memory cell will be one.

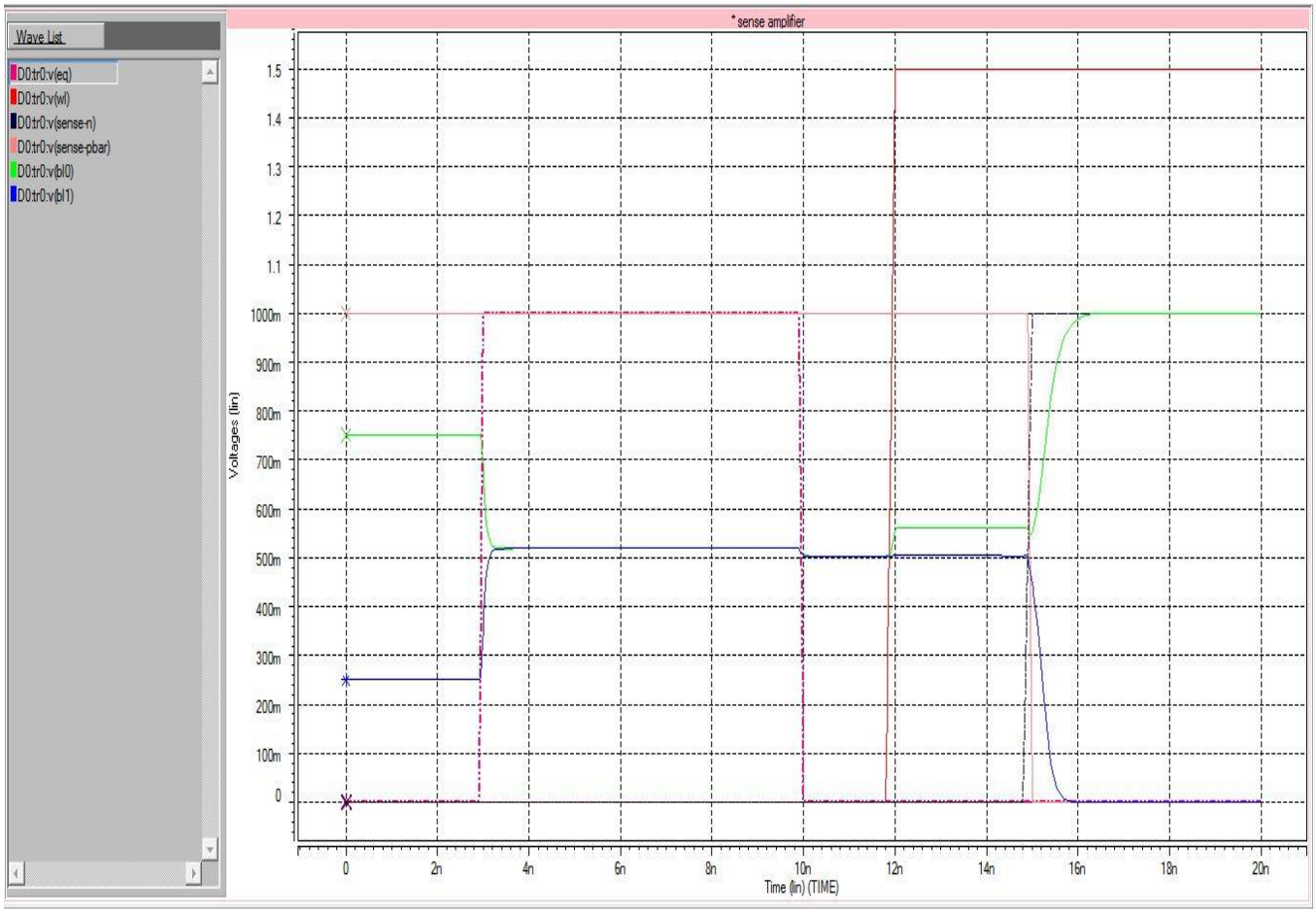

Fig 7: Simulation result

3. LATCH TYPE SENSE AMPLIFIER

3.1. Alpha Latch Sense Amplifier

The alpha latch sense amplifier has two sensing stages. One is local sensing and the other is global sensing stage. The circuit which is placed above the datalines (dl and dlb) are said to be local sensing stage while the global sensing stage is present below the datalines (dl and dlb).

The schematic diagram for alpha latch sense amplifier is shown below. The sense amplifier has two modes. One is standby mode and the other is operation mode. During standby mode, the sense amplifier does not perform any function. During operation mode only it performs sensing operation. To save power the sense amplifier is turned off by mn5 transistor during standby mode.

The sense amplifier is activated by making the enable (EN) signal high. The input voltage from the bitline (bl) and bitlinebar (blb) induces current variation in the mn9 and mn10 transistor. This result in current difference will appear at the drains of mn9 and mn10. Since column select (CS) signal turns off mn13, the full swing voltage will be appearing at the nodes of A and B. This will turning one of the transistors mn7 and mn12 to be on while the other is off. During operation mode the ENB signal kept low. Then the mp3 and mp4 transistors are turned on, thus only one current either i1 or i2 to the datalines. Then the global sense amplifier senses this voltage difference and amplifies it to CMOS logic levels. The schematic diagram for alpha latch sense amplifier is shown in Fig.8

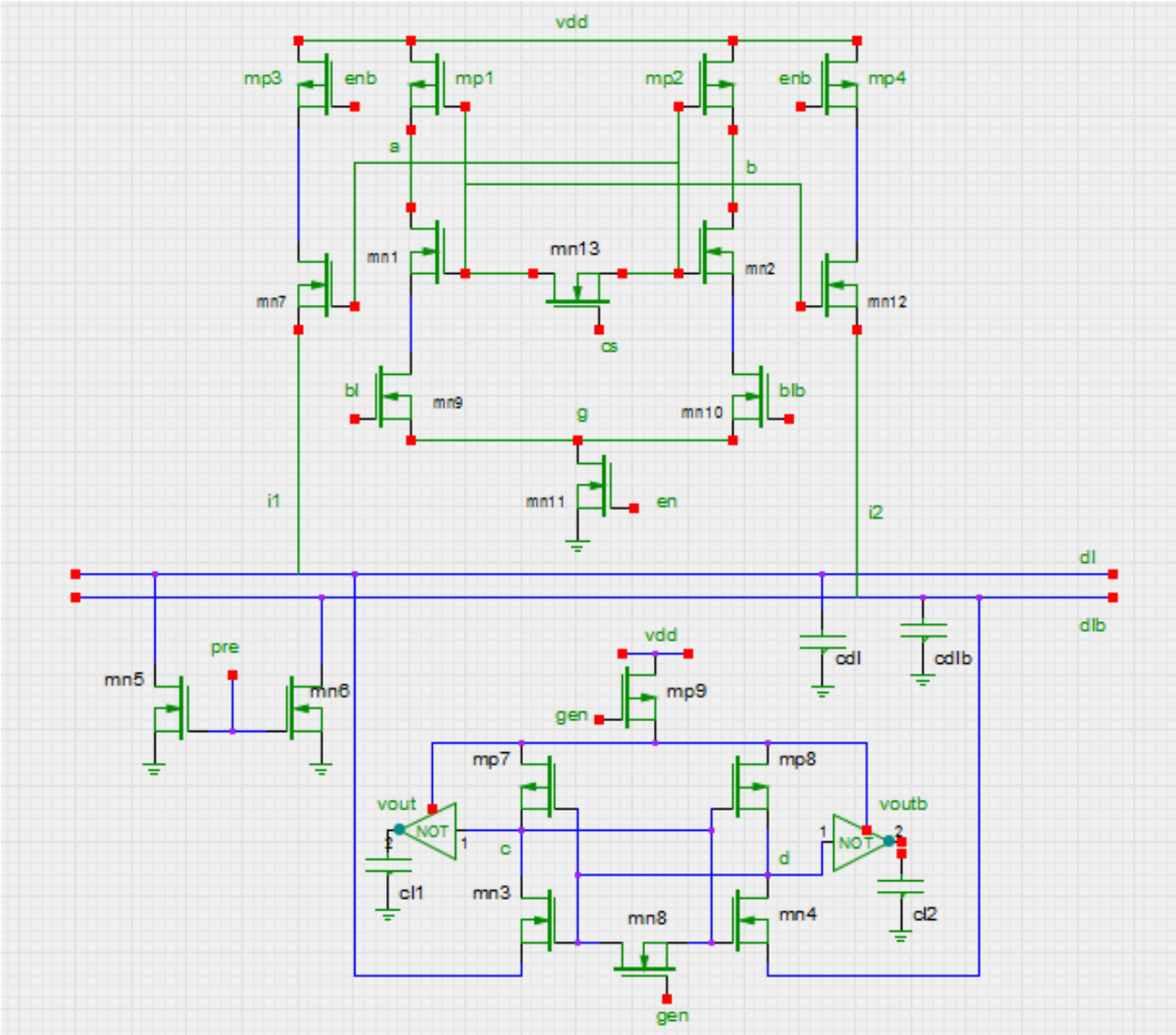

Fig 8: Alpha Latch Sense Amplifier

3.2. Current Conveyor Sense Amplifier

The global sensing stage of current conveyor sense amplifier is same as the alpha latch sense amplifier. The only difference is the local sensing stage, which is present above the datalines (dl and dlb). The four PMOS transistors mp1-mp4 are connected in a feedback structure. During read cycle the bitlines (bl and blb) are precharged to vdd. This will turn on the four PMOS transistors mp1-mp4 and operate in saturation region. The sense amplifier has the ability to convey the differential current from the bitlines to the datalines. The global sense amplifier senses this difference and amplifies the small voltage swing to full CMOS logic levels. The current conveyor has the current mirror circuit at the end of the local sensing stage. This will improve the current drive ability of the circuit. The below diagram shows the schematic diagram of current conveyor senseamplifier

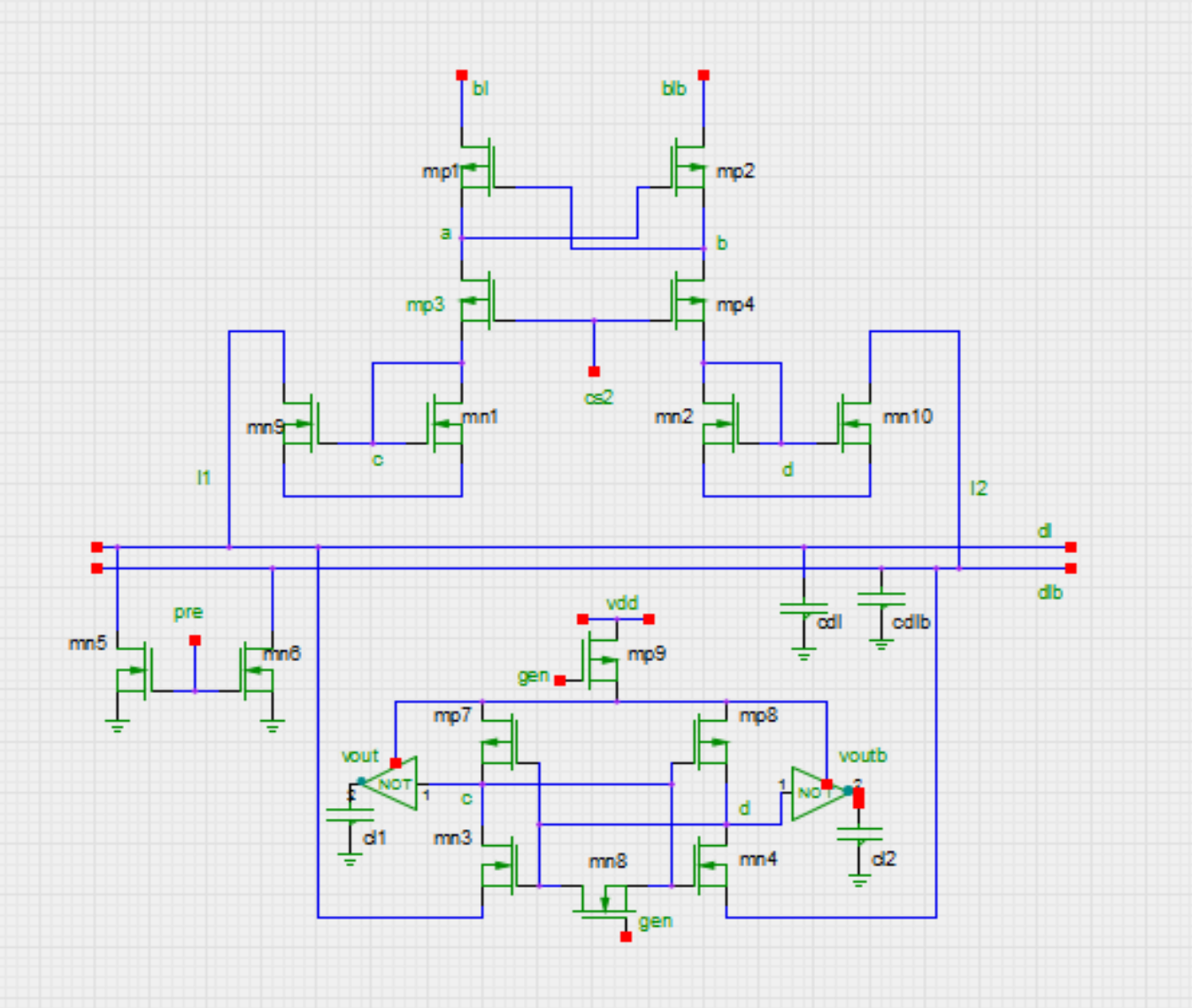

Fig 9: Current conveyor sense amplifier

3.3. Current Mode Sense Amplifier

The current mode sense amplifier also has two sensing stages. They are

(i) Local sensing stage, and
(ii) Global sensing stage.

The circuit which is place above the data lines (dl and dlb) are said to be local sensing stage. The transistor mp3 and mp4 act as a column switch. The local sensing stage consists of cross coupled inverter. It generates the bit lines differential current and transfers them to data lines. The circuit which is place below the datalines are said to be global sensing stage. The transistors mn5 and mn6 act as precharge transistor. During standby mode, the signal Column Select (CS) becomes high and makes the transistors mp3 and mp4 to be turned off, which in turn it block the bitlines current to flow. The Global Enable (GEN) signal also high during the standby mode.

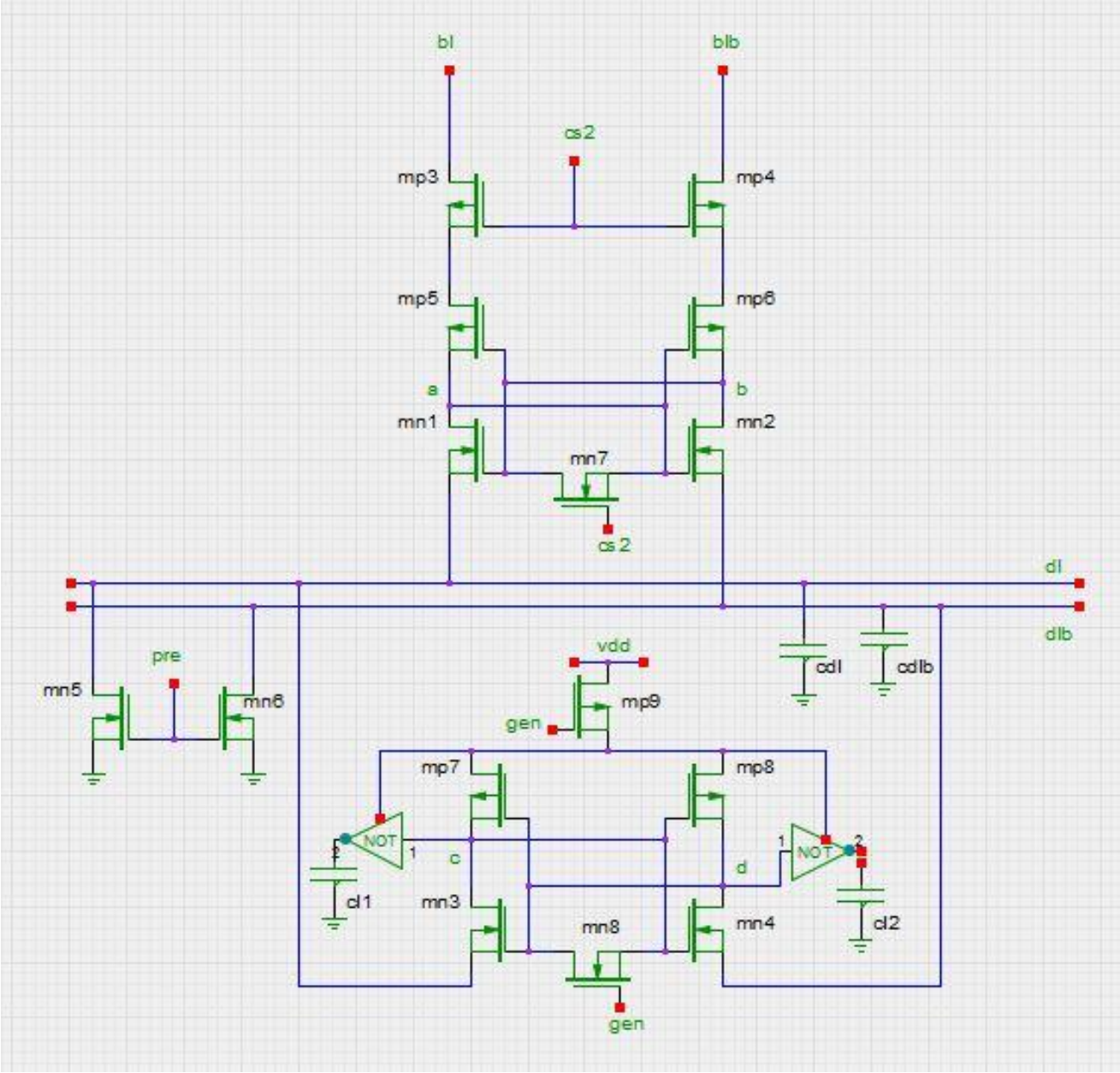

Fig 10: Current Mode Sense Amplifier

The above diagram shows the circuit diagram of current mode sense amplifier. The CS and GEN signal turn on the transistors mn7 and mn8 to equalize the nodes A, B, C, and D to same potential. Meanwhile, the mn5 and mn6 transistors turn on by precharge (PRE) signal. The PRE signal turns on the transistors mn5 and mn6, and pulls the datalines (dl and dlb) to ground. During operation mode, the signal PRE turn off the mn5 and mn6, allow the datalines to change freely. Consider the bitline (bl) voltage is higher than that of bitlinebar (blb).

The simulation result for current mode sense amplifier is shown in Fig.10.

As CS is triggered low, mp3 and mp4 are turned on to transfer the bitline potential and current to the input of the cross-coupled inverter. At the same time, mn7 turned off and activate the local cross-coupled inverter. This block senses the voltage and current differences at the source terminal of mp5 and mp6 and finishes its latching process. Hence, node A is pulled to vdd while node B is discharged nearly to ground.

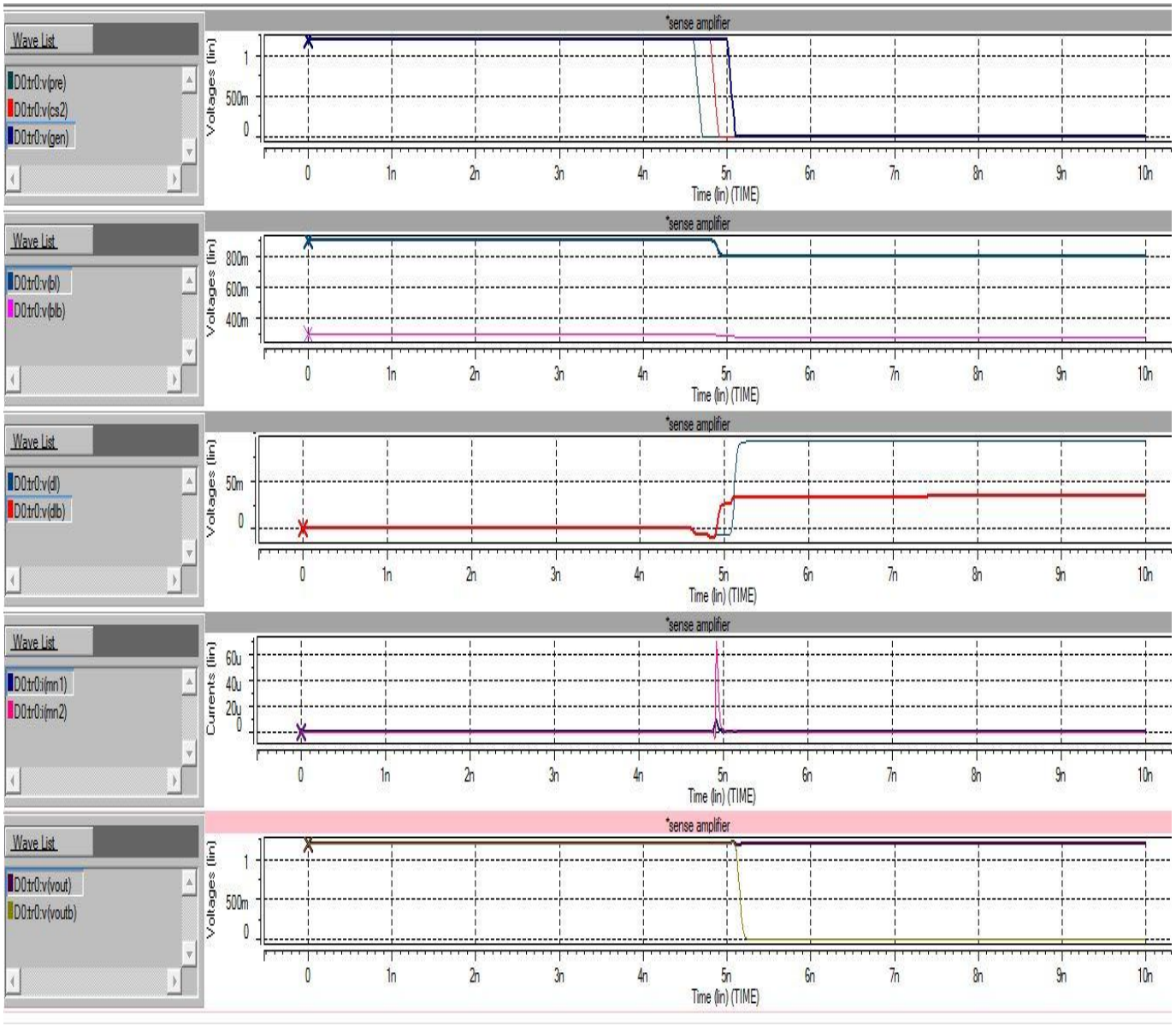

Fig 11: Simulation result

During this latching process, the current (i2) flow from mn2 to dlb is high compared to current (i1) from mn1 to dl. These differential current flow to the datalines and induce a voltage difference on the global data lines. This voltage difference is amplified by the global sensing stage to the node c and d. Then these voltages are fed to the output inverter and we get a full logic level.

The global sensing stage activated after the local amplification is performed. The current mode sense amplifier has the ability to quickly amplify a differential voltage swing on the bitlines and the dataline to the full CMOS logic level. It does not require a large input voltage swing. So it is widely used as one of the ways to reduce the sensing delay of the sense amplifier.

Fig.12. Shows the comparison of sensing delay between the latch type sense amplifiers for different power supply voltages. The supply voltage of the latch type sense amplifiers are scaled down to reduce the supply voltage of the sense amplifiers. Sensing delay of the sense amplifier is measured at from half of the supply voltage of the column select (CS) signal to the differential output of the sense amplifier reaches half of the supply voltage.

Latching delay of the sense amplifier is measured from half of the supply voltage of the enable (EN) signal of the sense amplifier to the when the differential output of the sense ampflifier reaches half of the supply voltage.

The graph of sensing delay versus supply voltage is shown in Fig.12. The graph shows that sensing delay for latch type sense amplifiers for various supply voltages. The snsing delay for current mode sense amplifier is low compared to the alpha latch sense amplifier and current conveyor sense amplifier.

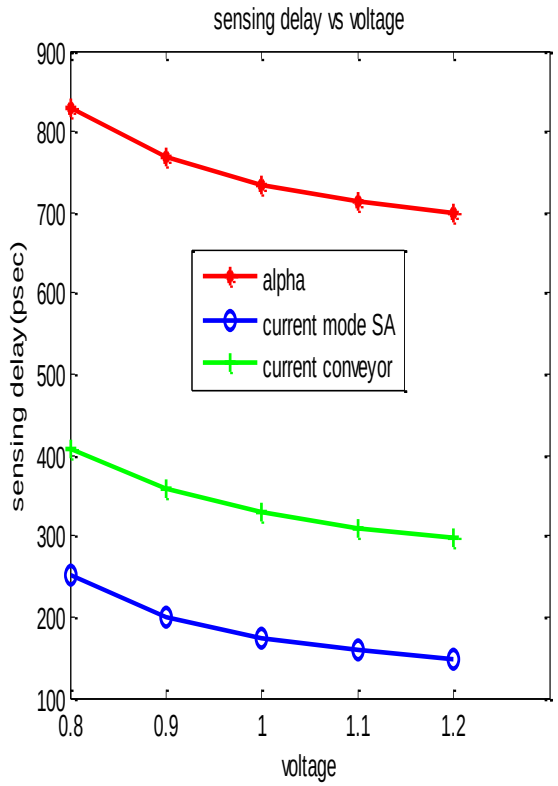

Fig 12: Graph of sensing delay Vs supply voltage

Table -1: Comparison of Latching delay Vs Supply Voltage for Alpha Latch Sense Amplifier

Supply voltage	Latching delay(nsecs)
1.2	198.8
1.1	213.18
1	234.79
0.9	269.76
0.8	329.78

Table -2: Comparison of Latching delay Vs Supply Voltage for Current Mode Sense Amplifier

Supply voltage	Latching delay(nsecs)
1.2	98.92
1.1	108.58
1	124.46
0.9	155.31
0.8	201.49

The above table shows latching delay for current mode sense amplifier and alpha latch sense amplifier for various supply voltages.

Due to the current-mode nature of the current conveyor we do not study its input-offset voltage. As a result, latching delay analysis is not applicable for current-conveyor sense amplifier.

4. CONCLUSION

The sensing delay and latching delay for various latch type sense amplifier has been analyzed using 90nm CMOS technology for various supply voltages. From that current mode sense amplifier has low sensing delay and latching delay. From the above, it can be concluded that current mode sense amplifier is suited for low voltage applications.

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BIOGRAPHIES

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