A SURVEY OF LOW POWER WALLACE AND DADDA MULTIPLIERS USING DIFFERENT LOGIC FULL ADDERS

R Naveen[1], K Thanushkodi[2], Preethi[3], C Saranya[4]

[1]*Assistant Professor, ECE Department, Info Institute of Engineering, Tamil Nadu, India*
[2]*Director, ACET, Tamil Nadu, India*
[3]*PG Student, ECE Department, Info Institute of Engineering, Tamil Nadu, India*
[4]*Assistant Professor, ECE Department, Info Institute of Engineering, Tamil Nadu, India*

Abstract

In recent years, power dissipation is one of the biggest challenge in VLSI design. Multipliers are the main source of power dissipation in DSP block. Power of any multiplier can be reduced by designing a full adder which will consume very less power. So a lot of researches have been made to decrease the power consumption of the full adder. Here a structured approach for analysing the Wallace and Dadda multiplier is introduced. These multiplier are designed using existing full adders like 28T,16T,14T, and TGFA. These designs are studied and the analysis is made based on the simulation parameter like no of transistors count and power consumption using micro wind tool.

Keywords: *Full Adder, Wallace Tree Multiplier, Dadda Multiplier, Power Consumption.*

----------***----------

1. INTRODUCTION

The explosive growth in portable system and cellular network has intensified the research efforts in low power microelectronics. Multiplier being the most important component of digital signal processors and microprocessors [1] requires more attention towards its design. In recent years many research have been made to reduce the power consumption in multipliers. The researchers mainly target on three goals such as minimizing the transistor count, minimizing the power consumption and increasing the speed while designing a multiplier [2]. Among the existing multiplier, here Wallace tree multiplier and Dadda multiplier were chosen due to high performance and high speed. C.S. Wallace suggested a fast multiplier [3] during 1964 with combination of half adders and full adders. Later many researchers were worked on this multiplier. Among them, the Wallace multiplier with full adder design had showed rapid development in reducing leakage power [4]. Luigi Dadda suggested a parallel multiplier during 1965 with combination of full adders and half adders. Then Dadda multiplier with full adder [5] shows rapid development in leakage power. For both the multiplier full adder being the basic unit and power consumption in this full adder extensively reduce the power consumption of both the multipliers. Hence a survey is made on these multipliers with different logic style full adders.

2. WALLACE AND DADDA MULTIPLIER BASED ON 28T FULL ADDER

2.1 28T Full Adder

The conventional full adder consists of 28 transistors [6] and it is shown in Fig -1.

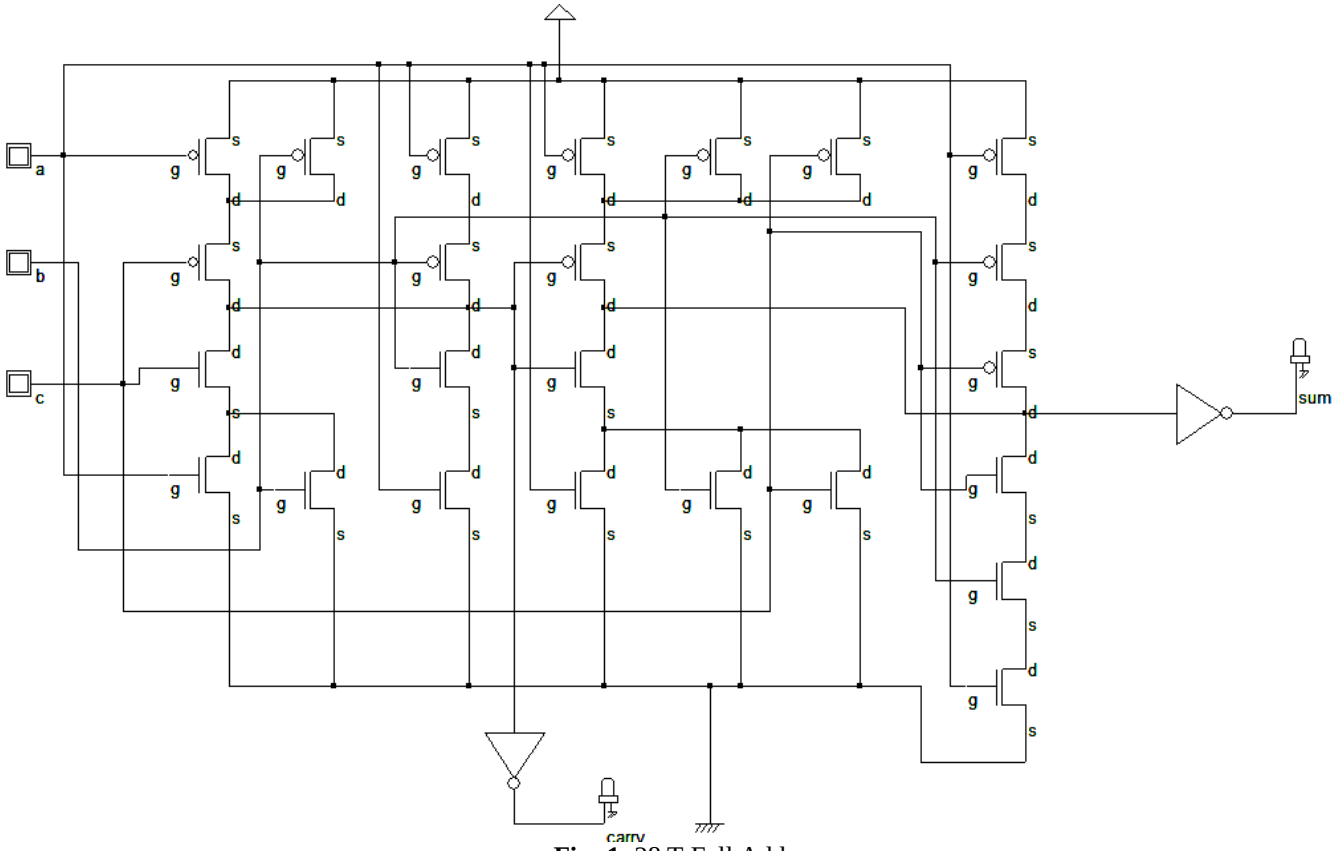

Fig -1: 28 T Full Adder

Adders form to be the most important component in the applications such as Digital Signal Processing architectures and microprocessor. The essence of the digital computing lies in the full adder design. Conventional full adder consists of 28 transistors [6] and is shown in Fig -2. Conventional CMOS implementation consists of two functional blocks pull-up and pull-down.

Pull-up functional block is implemented with P-channel MOS transistors and pull-down functional block is implemented with N-channel MOS transistors. One of the most significant advantages of this full adder was its high noise margins and thus reliable operation at low voltages. The layout of CMOS gates was also simplified due to the complementary transistor pairs. The voltage scaling and high noise margin design makes them highly advantageous than others thus it makes them to work at low voltages at ratio less transistor sizes.

Due to complementary relationship between pull-up and pull-down networks, an input combination which turns OFF the pull-up transistor will turn ON the pull down network and vice-versa. This eliminates the possibility of floating output. Pull down network is constructed using nMOS devices whereas for pull up network, pMOS devices are used. The main reason for this choice is that nMOSFET transistors produce “strong zeroes” and pMOSFET transistors give “strong ones”. A pMOS switch is able to charge the output all the way to vdd and nMOS transistor fails to raise the output above (vdd to vtn). In CMOS logic, all switches in pull-up network are implemented by using pMOS transistors whereas all switches in pull-down network are implemented by using nMOS transistors.The simulation had been done using microwind to analyse the performance of 28T full adders and the parameters are shown in Table -1.

2.2 28T Full Adders Based Wallace Tree Multiplier

The 4x4 Wallace tree multiplier is designed using 28T full adder [2] and it is shown in Fig -2.

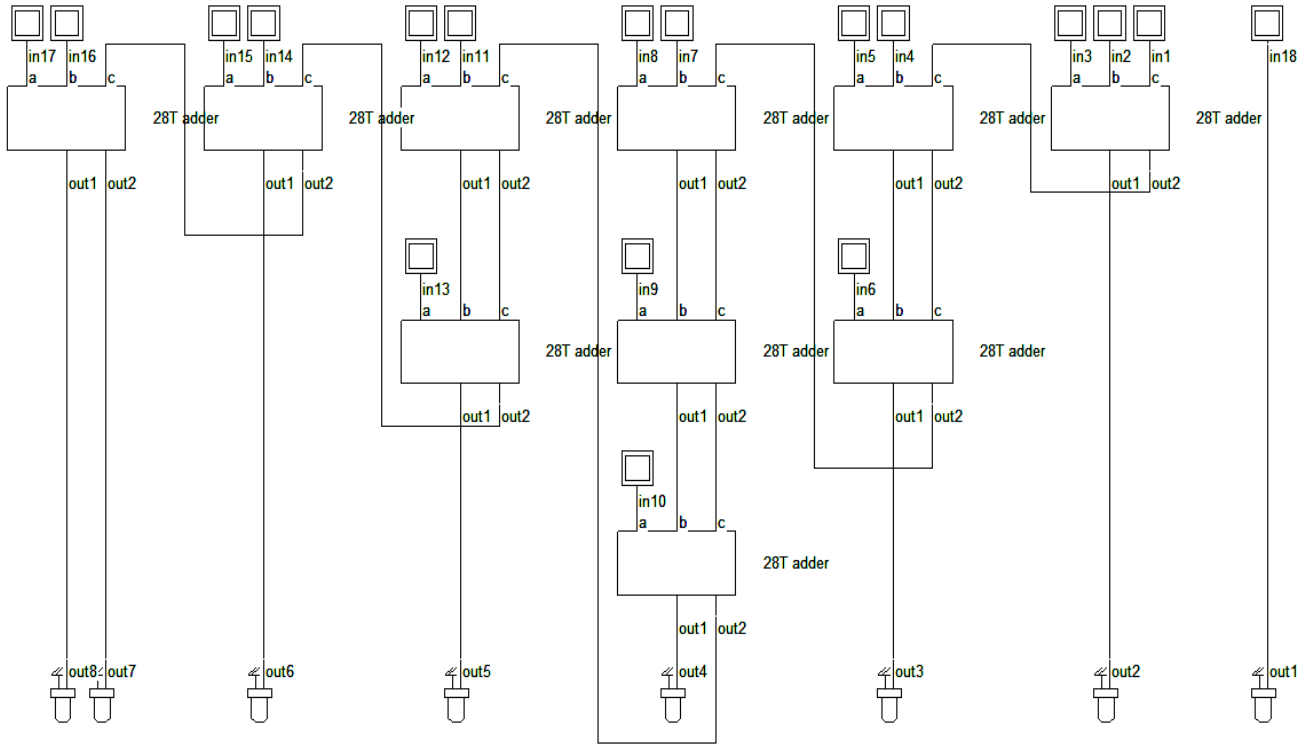

Fig -2: 28 T Full Adder Based 4*4 Wallace Multiplier

The design is simulated using micro wind tool. This design has 280 transistors and 8.58W power consumption.

2.3 28T Full Adders Based Dadda Multiplier

The 4x4 Dadda multiplier is designed based on 28T full adder as shown in Fig -3. The performance is analysed using micro wind simulation tool. This result shows that the design has 336 transistors and 0.1378uW power consumption

3. WALLACE TREE AND DADDA MULTIPLIER BASED ON 14T FULL ADDER

3.1 14T Full Adder

The 14T full adder requires 14 transistors to realize the adder function [7] as shown in Fig -4.

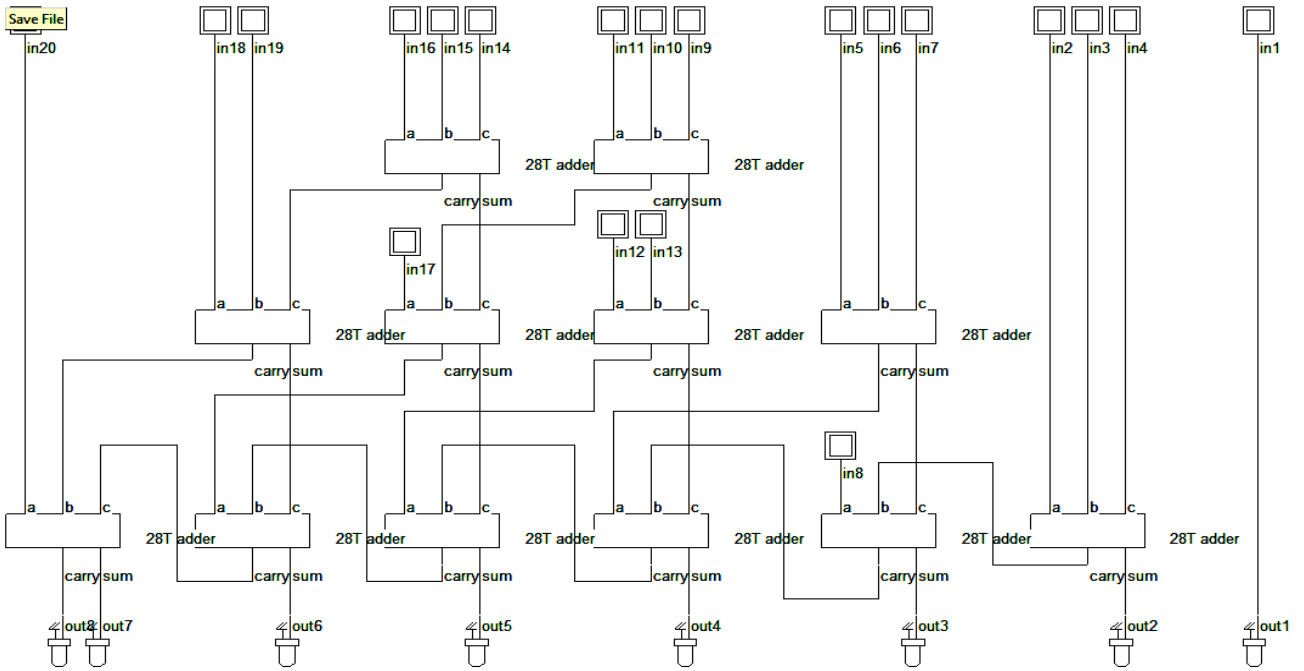

Fig -3: 28 T Full Adder Based 4*4 Dadda Multiplier

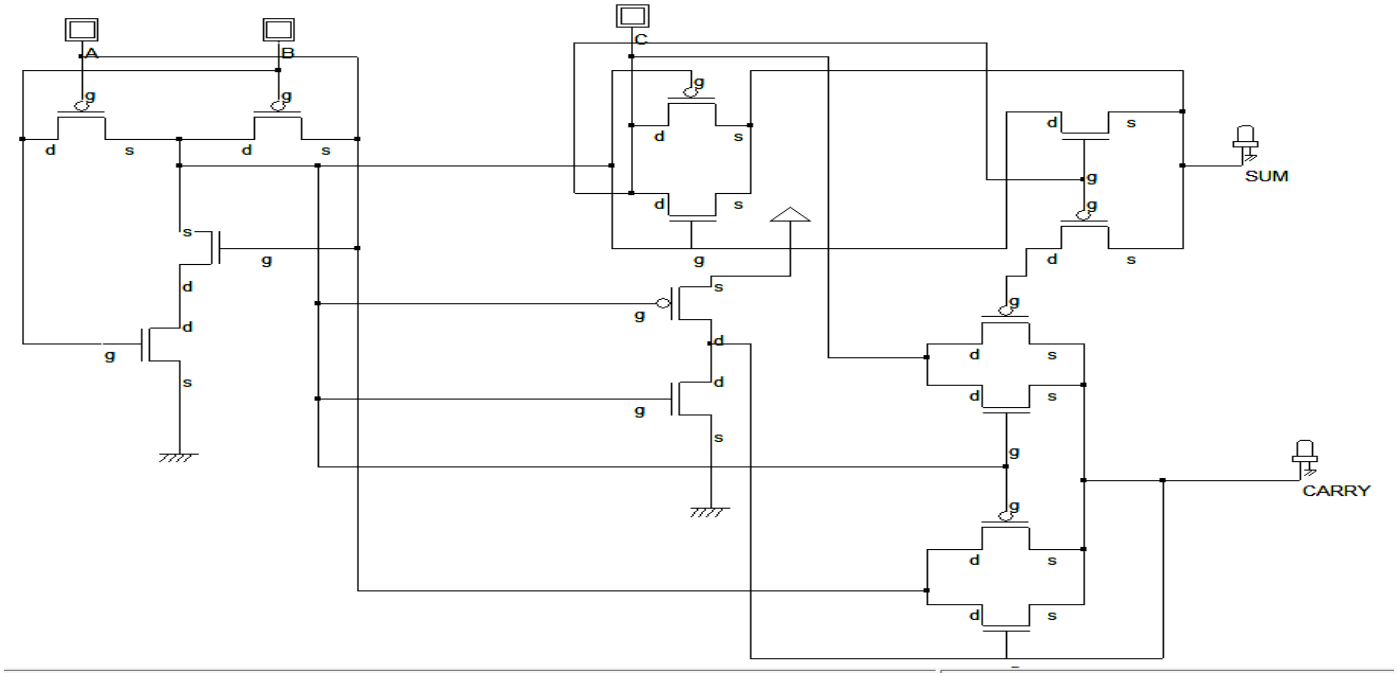

Fig -4: 14T Full Adder

The 14T full adder contains a 4T PTL XOR gate, an inverter and two transmission gates based multiplexer designs for sum and cout signals. This circuit has 4 transistors XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously to generate sum and carry. The signals cin and cin bar are multiplexed which can be controlled either by (a xor b) or (a xnor b). Similarly the carry can be calculated by multiplexing 'a' and 'cin' controlled by (a xor b).

The one advantage of this 14T adder is that it is the fastest and simpler than conventional adder. The main disadvantage of this adder is the large power dissipation which is more compared to conventional adder. However with same power consumption it performs faster. The transistor count and power consumption is shown in Table -1.

3.2 14T Full Adder Based 4*4 Wallace Tree Multiplier

The 4x4 Wallace tree multiplier has 10 full adders blocks with 14T logic style as shown in Fig -5. The design is simulated using Microwind tool .This design has 140 transistors and 8.60W power consumption.

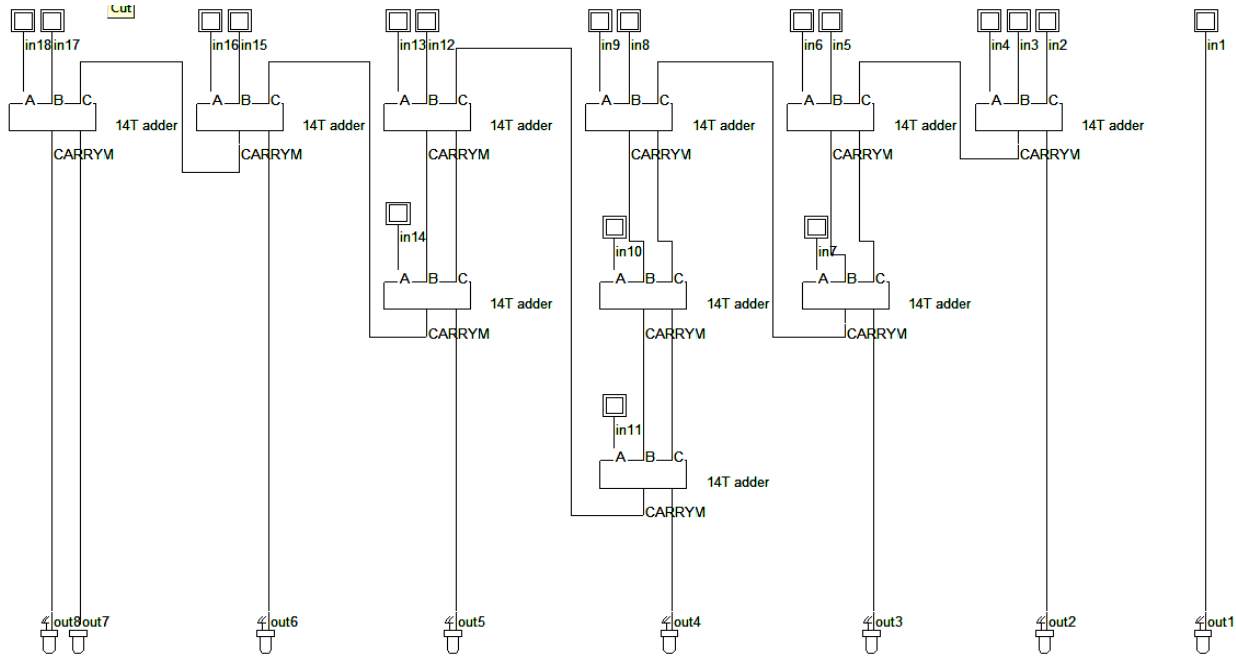

Fig -5: 14T Full Adder Based 4*4 Wallace Multiplier

3.3 14T Full Adders Based 4*4 Dadda Multiplier

The 4x4 dadda multiplier has 12 full adder blocks with 14T logic style full adders as shown in Fig -6. The design is simulated using Microwind tool and it has 168 transistors and 1.091uW power consumption

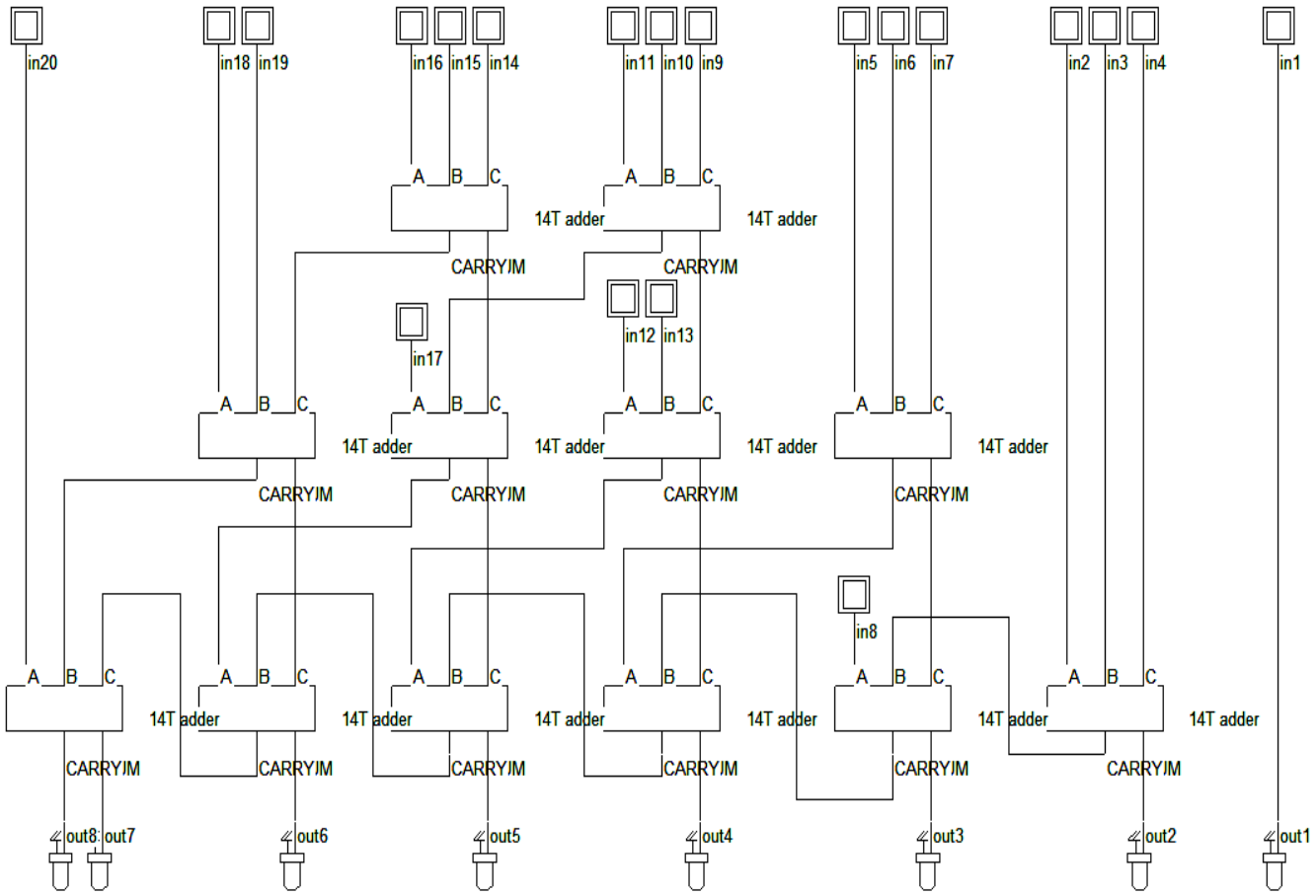

Fig -6: 14T Full Adder Based 4*4 Dadda Multiplier

4. 16T FULL ADDER BASED WALLACE TREE MULTIPLIER AND DADDA MULTIPLIER

4.1 16T Full Adder

16T full adder is the improved version of 14T full adder cell. It is same as 14T in terms of the output modules [8].This cell offers higher speed and lower power consumption than standard implementations of the 1-bit full-adder cell. It consumes less power compared to existing adders as it uses the XOR-XNOR circuits, pass transistor and transmission gates for its design. Eliminating an inverter from the critical path accounts for its high speed, while reducing the number and magnitude of the cell capacitances, in addition to eliminating the short circuit power component [10], account for its low power consumption. This adder has 16 transistors. It is based on the 4-transistor implementations of the XOR and XNOR functions presented in pass transistor and transmission gates. This new style has several advantages; first, it removes the inverter from the critical path of the cell, which decreases the cell delay. Second, it balances the delays of generating H and H0 , which leads to fewer glitches at the outputs. Third, it decreases the capacitance at node H, since it is no longer loading an inverter, while at the same time decreasing the capacitance at node H0. This eliminates the short-circuit power component within the cell. Finally, the incomplete voltage swing at H and H0 for some input combinations (A = B = 0, A = B = 1) reduces the power consumed by the circuit as shown if Fig -7. The transistor count and power consumption is shown in Table -1.

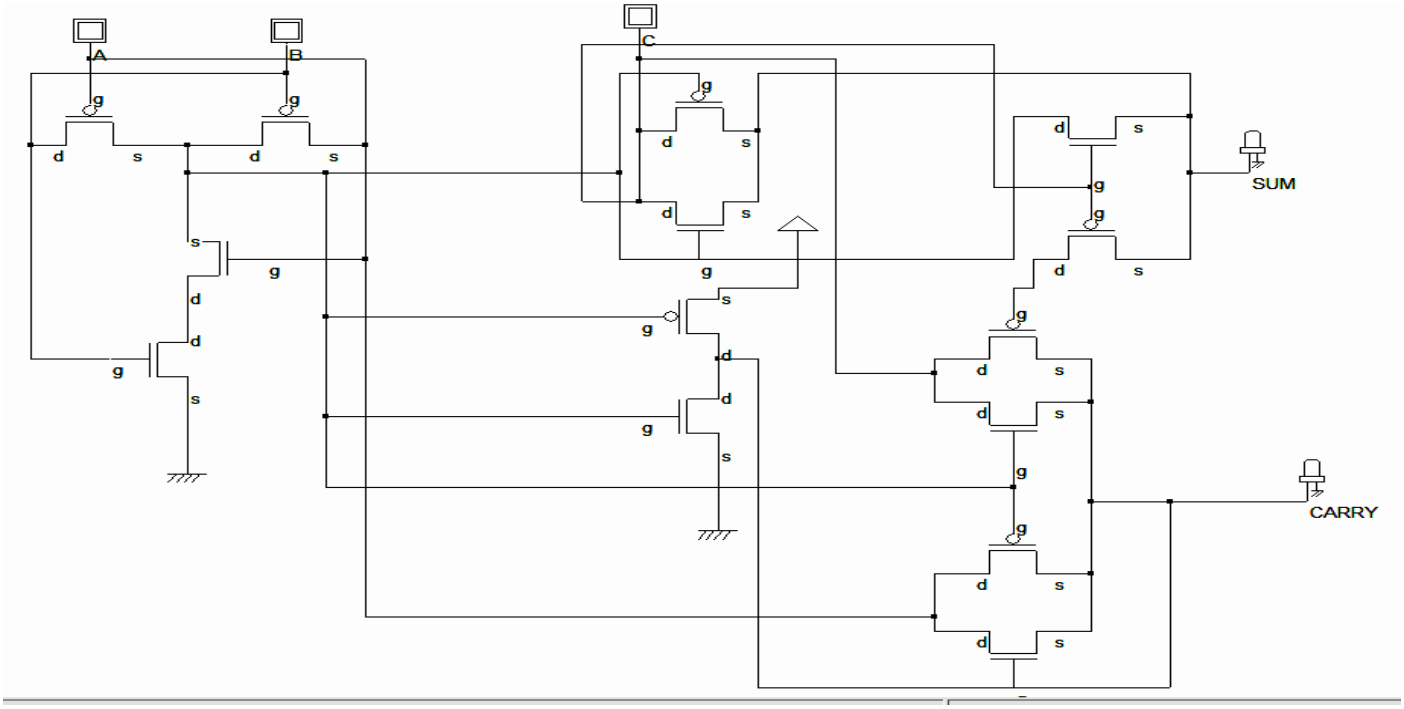

Fig -7: 16T Full Adder

4.2 16T Full Adder Based 4*4 Wallace Tree Multiplier

A 4x4 Wallace tree multiplier is designed using 16T based full adder as shown in Fig -8. The design is simulated using Microwind tool and it has 160 transistors and 08.50W power consumption.

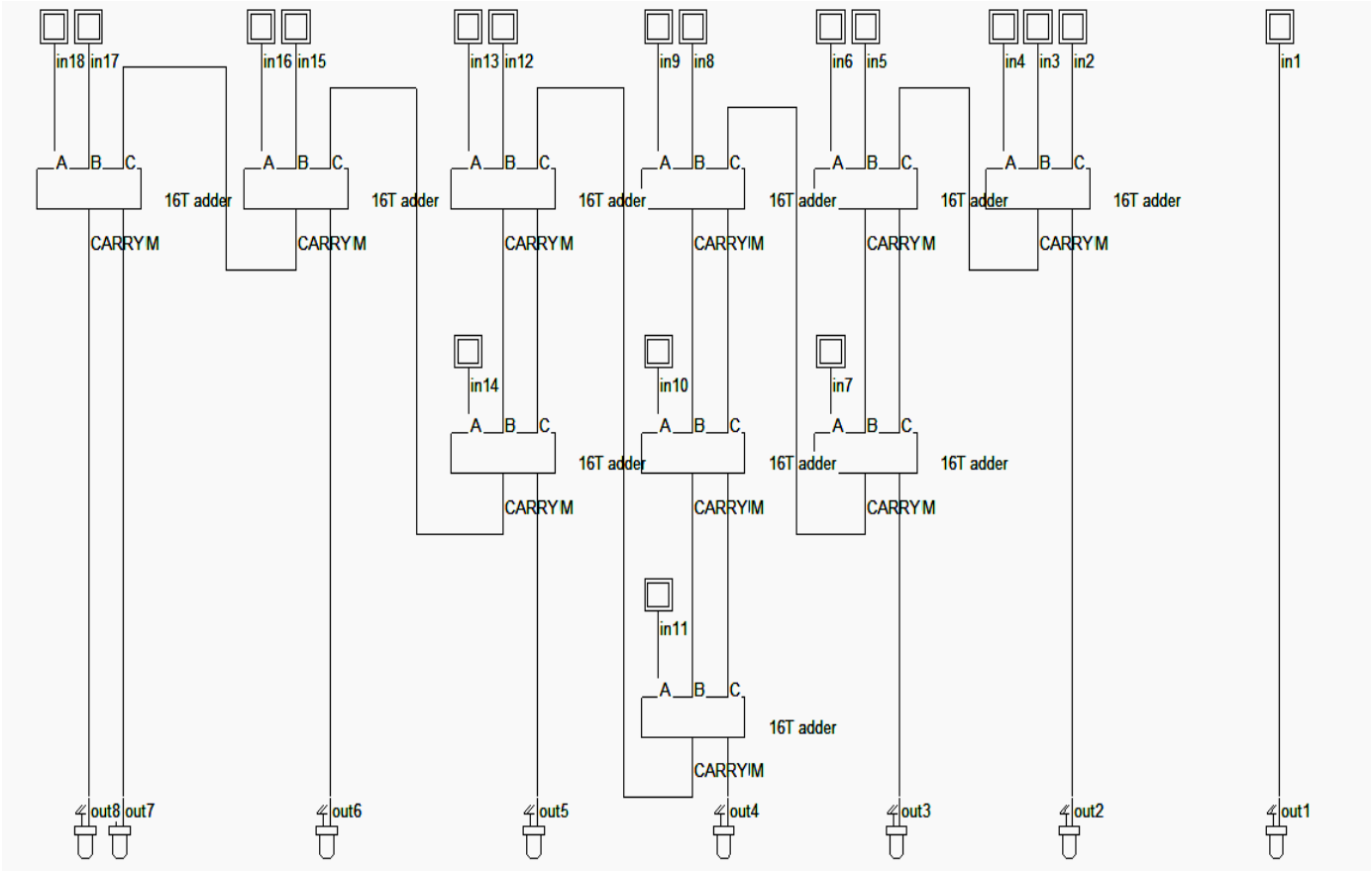

Fig -8: 16T Full Adder Based 4*4 Wallace Multiplier

4.3 16T Full Adders Based 4*4 Dadda Multiplier

A 4x4 dadda multiplier is designed using 16T based full adder as shown in Fig - 9. The design is simulated using Microwind tool and it has 192 transistors and 0.891uW power consumption.

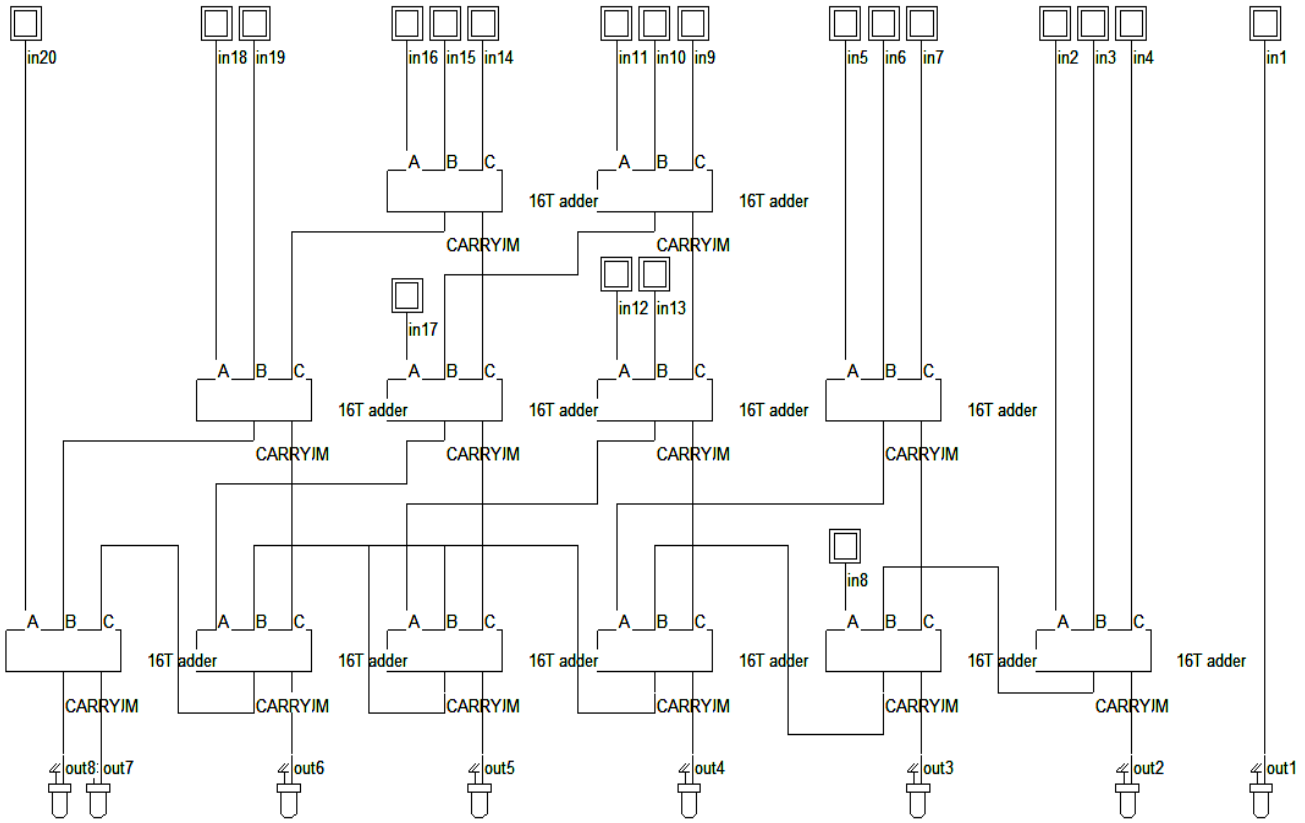

Fig -9: 16T Full Adder Based 4*4 Dadda Multiplier

5. TGFA BASED WALLACE TREE MULTIPLIER AND DADDA MULTIPLIER

5.1 Transmission Gate Based Full Adder

A transmission gate full adder is formed by connecting an nFET and pFET in parallel as shown Fig -10. The nFET Mn is controlled by the signal s, while the pFET Mp is controlled by the complement s bar. When wired in this manner, the pair acts as a good electrical switch between the input and the output variables x and y respectively. The operation of the switch can be understood by analysing the two cases for s. If s=0, the nFET is OFF; since s bar=1, the pFET is also OFF, so that the TG acts as an open switch.The transmission gate based full adder produces ouputs of proper polarity for both sum and carry with the disadvantage of high power consumption. The circuit have two inverters followed by two transmission gates which act as 8T-XOR[11]. Subsequently 8T-XOR module follows. It is the fastest adder. It is also simpler compared to conventional adder. But the power dissipation of this circuit is more than the conventional adder. The transistor count and power consumption is shown in Table -1

5.2 Wallace Tree Multiplier Based on Transmission Gate based Adder

Then the Wallace Tree Multiplier designed based on Transmission Gate based adder is shown in Fig -11. The design is simulated using Microwind tool and it has 200 transistors and 09W power consumption.

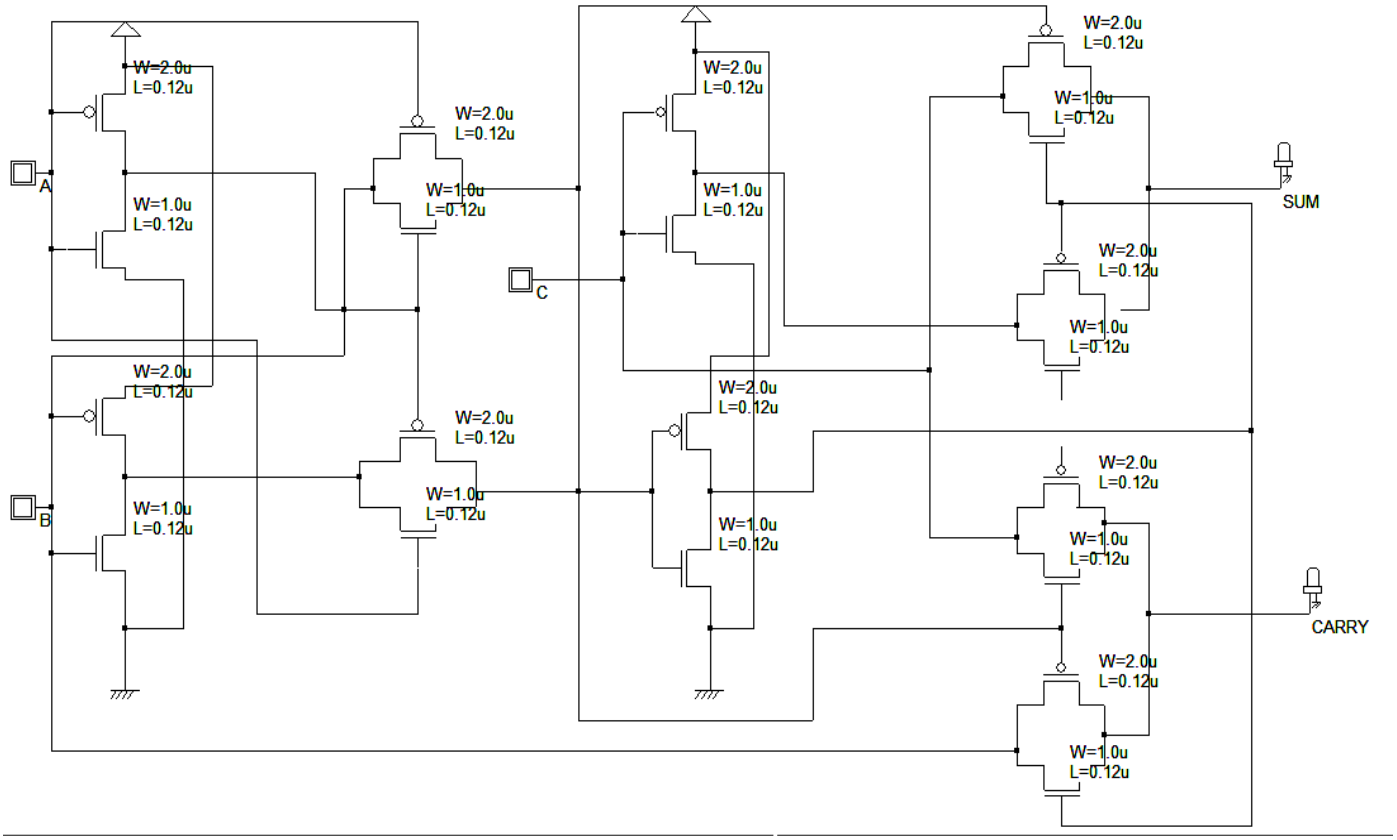

Fig -10: Transmission Gate based Full Adder

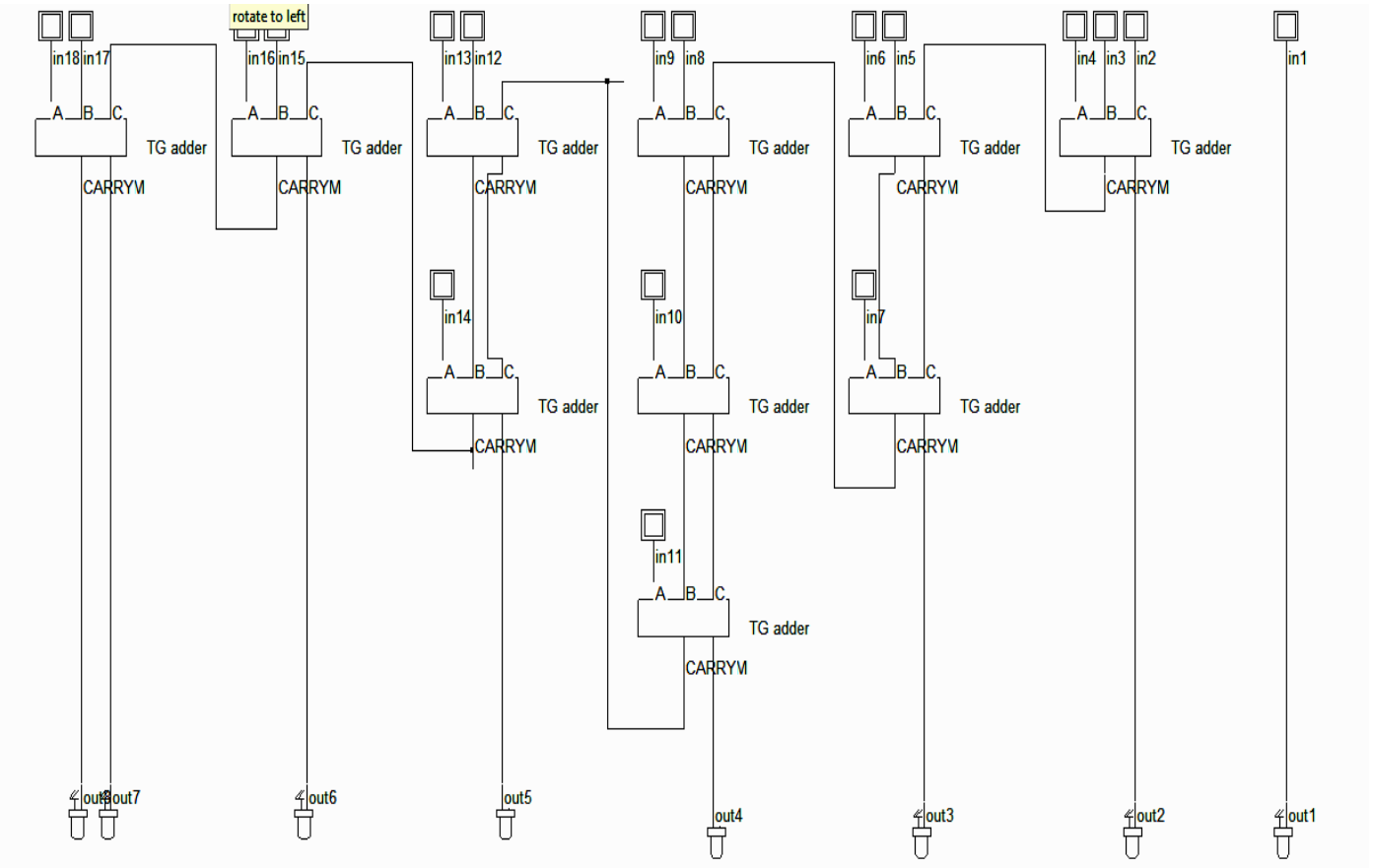

Fig -11: TGFA based 4*4 Wallace Multiplier

5.3 Dadda Multiplier Based on Transmission Gate based Adder

The Dadda Multiplier designed based on Transmission Gate based adder is shown in Fig -12. The design is simulated using Microwind tool and it has 240 transistors and 1.130uW power consumption.

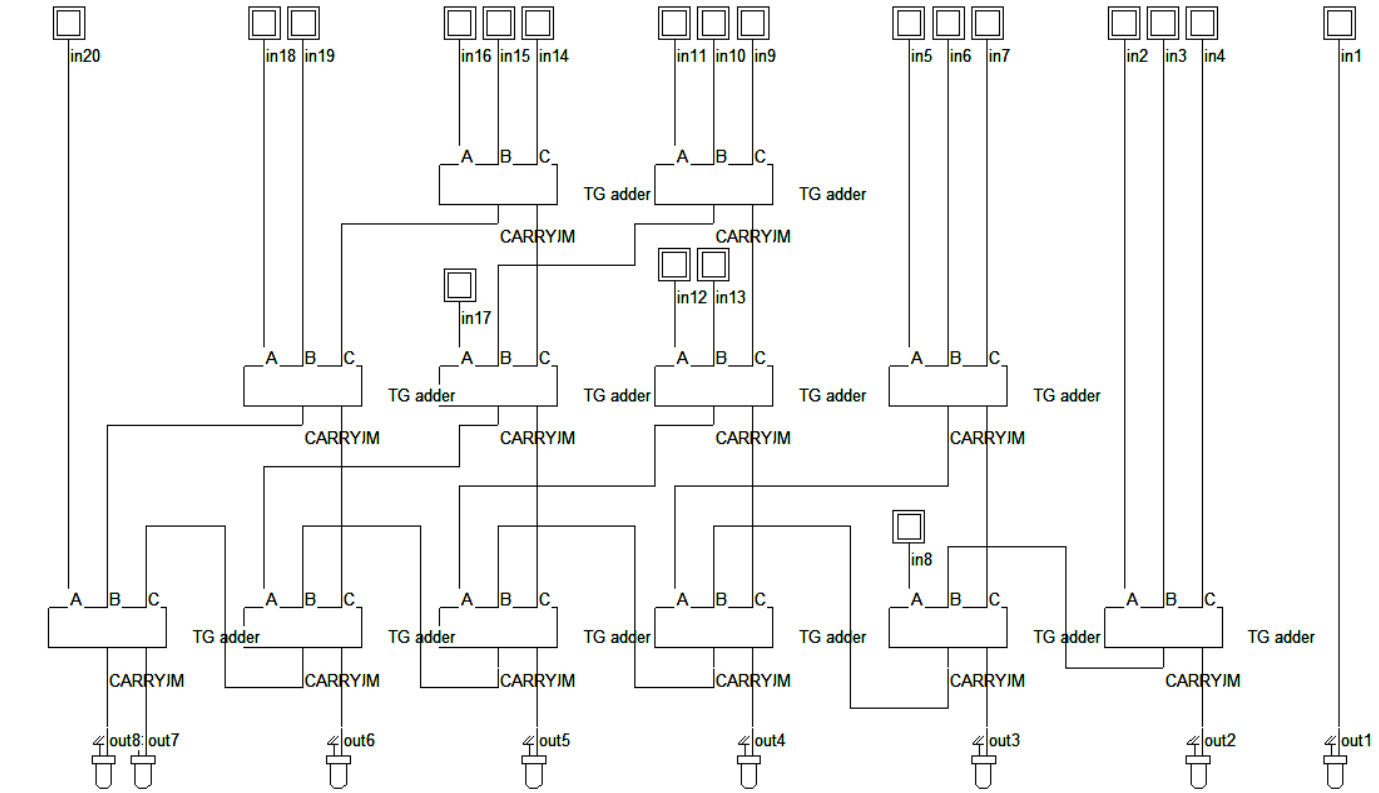

Fig -12: TGFA based 4*4 Dadda Multiplier

6. PERFORMANCE ANALYSIS AND COMPARISON

6.1 Performance Analysis of Adders

The performance of a full adder circuit depends greatly on the type of design used for implementation and also on the logic function realized using the particular design style. The analysis parameters are shown in the Table -1

Table -1: Performance Analysis of Adders

Types of adders	Transistor Count	Power Consumption
28T	28	91.66nW
14T	14	207.4nW
16T	16	85.04nW
TGFA	20	51.82nW

6.2 Performance Analysis of 4*4 Wallace Tree Multiplier

4*4 Wallace Tree Multiplier is designed using different logic full adders. The Wallace multiplier topology employs an array of full adders blocks in cascaded structure. Table -2 presents the performance of Wallace multiplier using different full adders.

Table -2: Performance Analysis of 4*4 Wallace Tree Multiplier

Wallace Tree Multiplier	Transistor Count	Power Consumption
28T based full adder	280	08.58W
14T	140	08.60W
16T	160	08.50W
TGFA	200	09W

6.3 Performance Analysis of 4*4 Dadda Multiplier

Here 4*4 Dadda multiplier is designed using different logic full adders. The Table -3 shows the performance of Dadda multiplier

Table -3: Performance Analysis of 4*4 Dadda Multiplier

Dadda Multiplier	Transistor Count	Power Consumption
28T based full adder	336	01.378uW
14T	168	01.091uW
16T	192	0.891uW
TGFA	240	1.130uW

7. CONCLUSION

In this paper, 4*4 Wallace and Dadda multipliesr has been designed based on various full adders had been reviewed from the most recent published research work. Wallace and Dadda multiplier are compared with themselves based on different logic full adders by considering parameters like transistors count and power consumption. Based on the survey it is concluded that 14T based Wallace and Dadda multiplier have less transistors count and 16T based Wallace and Dadda multiplier have less power consumption..

REFERENCES

[1]. N.M.Chore ,R.N.Mandavgane," A Survey of low power high speed one bit full adder"in Recent Advances in Networking,VLSI & Signal processing 2012,pp 302-307

[2]. Janagam.Srinivas Rao,Gulivindala.Suresh,"Performance Analysis of full adder& its impact on multiplier design",in IJSCE,Vol-3,no-3,pp 216-220,2013.

[3]. C.S.Wallace,"A suggestion for a fast multiplier",IEEE Trans.Electron.Vol EC-13,pp 14-17,Feb 1964

[4]. R.Naveen, K.Thanushkodi, C.Saranya," Leakage power reduction in Wallace tree multiplier using current comparison based domino logic adders",JATIT.Vol-55,no-1,2013

[5]. Kenneth Steiglitz and Peter R.Cappello, "A VLSI layout for a pipelined Dadda multiplier", ACM transaction on computer systems Vol-1,no-2,pp 157-174.pg.983

[6]. M.S.Damle, Dr.S.S.Limaye and M.G.Sonwari, "Comparative Analysis of different types full adder circuits",IOSR Journal of computer Engineering,Vol-11,no.3,pp1-9,2013

[7]. T.Vigneshwaran, B.Mukundhan, P.Subbarami Reddy,"A Novel low power and high speed performance 14T transistor CMOS full adder cells", Journal of applied sciences,6(9),pp .1978-1981,2006

[8]. H.Eriksson, P.L.Edefors, T.Henriksson, C.Svensson, "Full Custom versus standard cell design flow: an adder case study "in proceedings of 2003.Asia and south pacific design automation conference,pp.507-510,2003

[9]. Keivan Navi,Majid Hashparast and vahid Forouteen,"A new low power dynamic full adder cell based majority function",World aoolied sciences journal vol.4,no-1.pp 133-147,2008

[10]. Hajar Zare Bahramabadi, Hamidreza Dalili Oskouei, Asghar Ebrahimi, "Design Low Power Full adders for Arithmetic Applications," International Journal of Emerging Science and Engineering, Vol.1, 2013.

[11]. Santhosh Chede, Kishore Kulat, Rajesh Thakare, "A Significance of VLSI Techniques for Low Power Real Time Systems," International Journal of Computer Applications, Vol. 1, 2010.