LV SIDE DISTRIBUTED POWER FACTOR CORRECTION SYSTEM

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Abstract

Power factor is a very important parameter of power system. In an electric power system, a load with a low power factor draws more current than a load with a high power factor for the same amount of useful power transferred. The higher currents increase the energy lost in the distribution system, and require larger wires and other equipment leading to increase in the cost of the system [1]. So it is very necessary to have a good power factor. Here we have proposed a Low Voltage (LV) side distributed model to correct the power factor of the power system. It can reduce the losses in the transmission, system size, cost of the system and complexity in the instalment. We have also designed a low cost, reliable, efficient system using ATmega16 (8-bit CPU) from Atmel Corporation which can be used in the proposed system for automatic correction of the power factor.

Keywords: *Power Factor, Automatic Power factor Correction System, AVR, ATmega16, Capacitor Bank, Power System etc…*

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1. INTRODUCTION

In electrical engineering, the power factor of an AC electrical power system is defined as the ratio of the real power flowing to the load, to the apparent power in the circuit [2], and is a dimensionless number between -1 and 1[3]. If we denote real power with P and apparent power with S then:

$$\text{Power Factor} = P/S \qquad (1)$$

If we denote power factor by Cos (ω), where ω is the angle between the real power and apparent power or phase difference between current and voltage; then real power flowing in the system will be:

$$P=VI\ Cos\ (\omega) \qquad (2)$$

At **ω=0°, Cos (ω) =1**, putting these values in equation (2):

$$P=VI*1$$

$$P_{MAX}=VI \qquad (3)$$

So for the maximum value of real power to be transferred power factor should be equal to one in other words the current and voltage should be in the same phase. In the power system power factor is generally kept between 0.9 and 0.95[4].

2. PROPOSED MODEL

We are using power correction devices generally at substations marked with "**A**" in the figure below. A part of power is wasted in the transmission lines before it reaches to the user. There are several more problems occur in case of system we use now days i.e. instalment cost, maintenance, re instalment on system failure. So here we have proposed a distributed system of power factor correction system at LV side which will inject the reactive power at the user level instead of substations to do so we can install a small device for every user which will fulfil the need of reactive power for that particular user. This proposed model has several advantages over what we are using now days as explained below. A block diagram of proposed model is shown below:

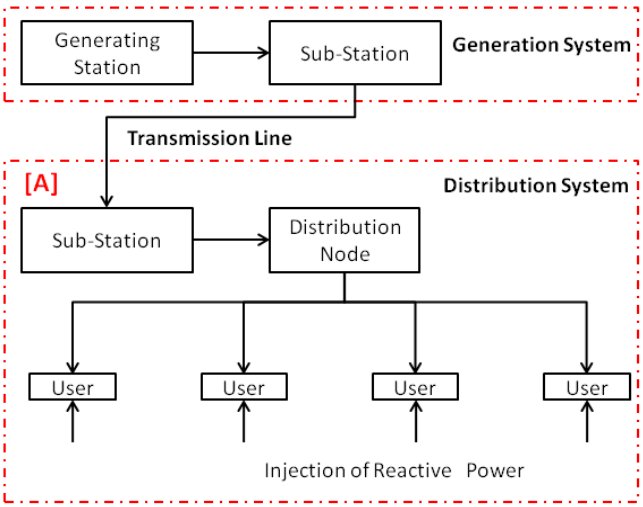

Fig-1: Block Diagram

Advantages of Proposed Model:

1. In case of our proposed model the system is distributed over user level so in case, if any unit fails we will still have the other unit to compensate the effect.
2. In case of system failure re instalment of device will not be expensive.
3. It will reduce the complexity in instalment.

4. Voltage at distribution side is quite low (220/440 V) and designing and manufacturing of capacitor used in capacitor bank for power factor correction is easy and economical as compared to high voltage capacitors. This will reduce the cost of the system.
5. If we inject the reactive power at user level then we can save a part of electrical energy which being wasted in the transmission. This will improve the efficiency of the system.
6. We can improve the system response by using our proposed model as we know that a small unit can response faster than a big one.
7. We can design system with higher precision and repeatability.

These are few advantage of using our proposed model but still there are many more to discover

3. SYSTEM DESIGN OF AUTOMATED POWER FACTOR CORRECTION SYSTEM

For the system design of automated power factor correction system we have used ATmega16 (8 bit CPU) from Atmel Corporation as processing and calculating device. It comes in 40 pin DIP package having 32 I/O pins, one 16 bit timer/counter named as timer1, one 10 bit ADC using successive approximation technique for Analog to digital conversion, capable of taking 16 K samples per second and Interrupt pins capable of triggering software interrupts on external events i.e. rising edge, falling edge or on logic change [5]. For the measurement of load current we have used ACS712ELCTR-20A-T Current sensor module capable of measuring A.C. current up to 20 A. Its output is calibrated to give 100mV per Ampere of input current [6]. Block diagram of the whole system is shown below:

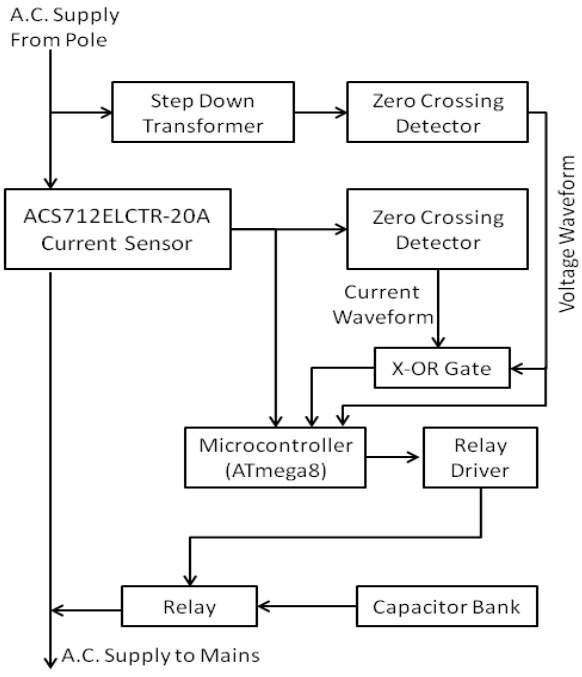

Fig-2: System Design

As for the power factor control we need both phase angle and the load current. So we can explain the whole system design in following steps:

3.1. Measurement of Phase Angle:

Here our task is to measure the Phase angle between the voltage and current. There are many techniques to measure the phase difference but voltage and current but as using microcontroller we can measure the time period very easily and accurately so here we are using the time measurement technique to measure the phase angle. We are measuring the time delay between the voltage and current and then we are converting it back in the angle. To measure the time delay between the voltage and current first of all we have passed the voltage waveform to the zero crossing detector circuit (ZCD) through a step down transformer to convert it in digital format. Again we have passed the output of the current sensor module to the zero crossing detector circuit (ZCD) to get the current waveform in the digital format (reference voltage in case of current waveform to ZCD is 2.5 V instead of 0 V because output of current sensor is adjusted about 2.5 V not 0 V. Here current sensor module output varies with the input current passing through it so it works as I-V converter. We are also using it for the measurement of load current) both current and voltage waveform from both zero crossing detector circuit (ZCD) circuit is passed to an X-OR gate. We are getting high level voltage at its output only during the time which is equal to the lag or lead time. It can be understand easily from the figure below:

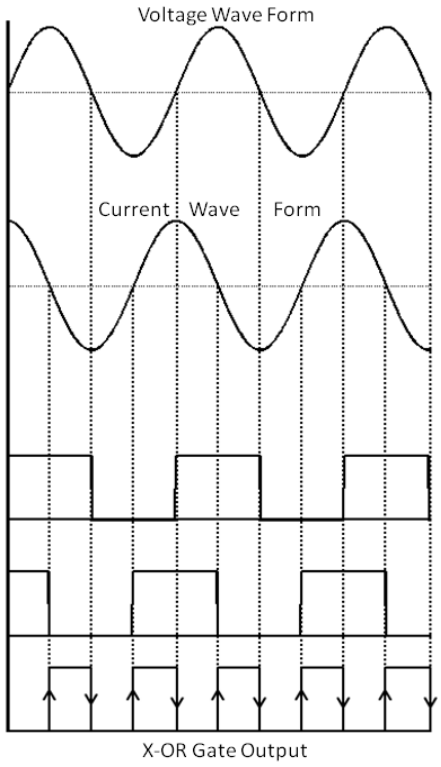

Fig-3: Output Wave forms

As we can see in the figure above that if we can somehow able to measure the time period between the rising and falling edge of X-OR gate then we can easily find the Phase angle. The output of X-OR gate is connected to the INT0 pin of ATmega16 which is capable of generate software interrupt on rising and falling edge of input signal. We have used timer1 running at 2 MHz to measure the time duration between two events on INT0 pin.

Once a rising edge occurs at INT0 pin of ATmega16 it requests an interrupt and while executing interrupt handler we have programmed it to reset the timer/counter value to zero. Now as soon as the falling edge occurs at INT0 pin it requests an interrupt again and while executing the interrupt handler we programmed it to capture the timer value for the manipulation of phase angle. This can be understood from the figure below:

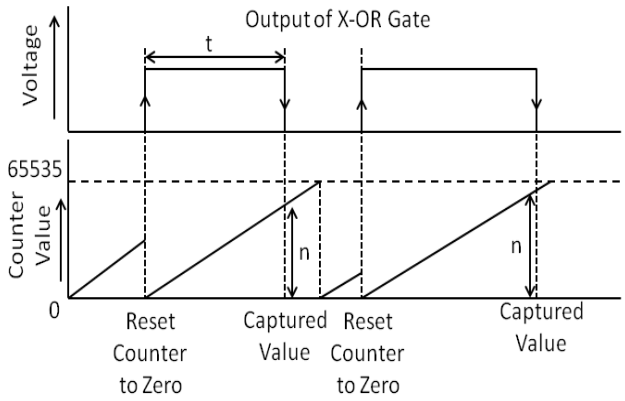

Fig-4: Capturing Time Period of output of X-OR Gate

As we know that timer is running at 2 MHz so time taken by it to increment its value by one will be its time period if we denote it by T then:

$$\mathbf{T=1/(2*106)} \qquad (4)$$

Where T is in seconds,

If the captured value is **n** and if we denote captured time by **t** then captured value t will be

$$\mathbf{t = 1000nT} \qquad (5)$$

Where t is in ms (1 s = 1000 ms).

Now we need to convert this time into the phase angle.

We know that for 50 Hz A.C. supply 20 ms is equal to 360°:
20 ms = 360°

So, 1 ms = 360°/20=18°

And $\mathbf{t\ ms = 18t°}$ (6)

From equation (6) we can calculate the phase angle between the voltage and current in degrees.

Here to find that this phase angle is leading or lagging we have given a feedback to the microcontroller from the voltage waveform. From the output waveform we can easily understand that if voltage will be leading with current then falling edge of X-OR gate and voltage will occur at same time. If voltage will be lagging with current then rising edge of X-OR will occur at the falling edge of voltage waveform. In this way we can find that the phase angle is for leading or lagging.

3.2. Measurement of Load Current:

To measure the load current using current sensor module we have used ADC of ATmega16. We know that PEAK value and RMS value of current are interchangeable using the equation below:

$$\mathbf{I_{RMS} = I_{PEAK} /\sqrt{2}} \qquad (7)$$

We are measuring the PEAK value of the input current as it is easy to measure form the ATmega16. To measure the PEAK value of current from ATmega16 we have used 5V as V_{REF}

So step size will be,

$$\mathbf{Step\ Size = V_{REF} / 1024 = 5/1024} \qquad (8)$$

If the digital output from ADC is **X.**

Then,

$$V_{OUT} = X*\text{Step Size}$$

$$\mathbf{V_{OUT} = (X*5)/1024} \qquad (9)$$

Where V_{OUT} is measured in volts. The output of current sensor module is adjusted around 2.5 V instead of 0 V so we need to subtract 2.5 from the V_{OUT} to get the PEAK voltage so,

$$\mathbf{V_{PEAK} = V_{OUT} - 2.5} \qquad (10)$$

Where $\mathbf{V_{PEAK}}$ is in Volts

The current sensor output is calibrated to give output of 100mV/Amp so,

$$I_{PEAK} = (V_{PEAK} * 1000)/100$$

$$\mathbf{I_{PEAK} = (V_{PEAK} * 10)} \qquad (11)$$

Where I_{PEAK} is measured in Amp. So by using equation (11) we can find the PEAK value of current flowing into the system or load current.
Now,

$$\mathbf{I_{RMS} = I_{PEAK} / \sqrt{2}} \qquad (12)$$

By using equation (12) we can find the RMS value of the current in Amperes.

4. WORKING OF DEVICE

Once we have calculated the power factor and load current our task is to inject the reactive power into the system depending upon the need so that power factor can be improve. We have used capacitor bank to inject the reactive power into the system as they are easy to design and low cost. Before we connect capacitor bank to the power system we must need to know that how much capacitance we should connect. For that we have done a little bit of calculation. For calculation we need to know the phasor diagram of the various currents in the power system. A typical phasor diagram of various currents in the power system is shown below:

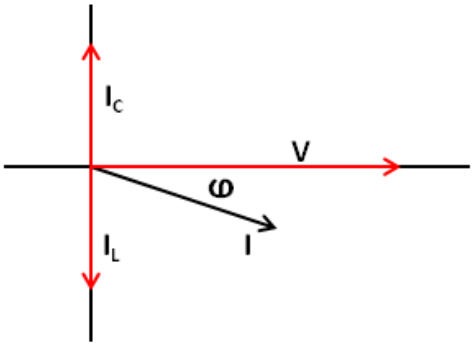

Fig-5: phasor Diagram of Current and Voltage

In last section we have shown that how we have measured the $\mathbf{I_{RMS}}$ value of load current. If we denote $\mathbf{I_{RMS}}$ by **I** as:

$$I = I_{RMS}$$

Then from the phasor diagram:

$$\mathbf{I_L = I * \sin(\omega)} \qquad (13)$$

From the equation (13) we can calculate the reactive current I_L. Here we can see that I_R is responsible for the reactive power and I_C is the counter part of it and for perfect balance.

$$\mathbf{I_C = I_R} \qquad (14)$$

Now we know that,

$$Q = CV$$

$$dQ/dt = C\,(dV/dt)$$

$$\mathbf{I_C = C\,(dV/dt)} \qquad (15)$$

Now as we know that A.C. voltage changes 0-311 V in 5 ms (considering 220 V_{RMS} supply) then,

$$\mathbf{dV/dt = (311 * 1000)/5 = 62200\ V/Sec} \qquad (16)$$

Putting this value in equation (15):

$$I_C = C * 62200$$

Or $$\mathbf{C = I_C / 62200} \qquad (17)$$

Where C is in Farad.

From equation (14) for perfect balance:

$$I_C = I_L$$

So putting this value in equation (17)

$$\mathbf{C = I_L / 62200} \qquad (18)$$

From above equation we can calculate the value of capacitance needed for the perfect counter back. Once microcontroller is calculated the phase difference, load current and finally the value of capacitance required to encounter the reactive power we need to connect that amount of capacitance to power system. We have designed a capacitor bank using 10 capacitors (**10µF** each). We have connected those using relays in such a way that any one of them can be connected in series or in parallel. In this way they can offer a maximum of **100µF** capacitance while connected all in parallel and minimum of **1µF** while all connected in series. By choosing the various combinations of relays we can get value from **1µF** to **100µF** which needs to be connected with the power system. Using this system we can encounter a minimum IL of 0.0622 A (when **C=1µF**) and maximum of 6.22 A (when **C=100µF**). We can calculate these values very easily by just putting the values of capacitance in the equation (18). For more power applications more capacitor can be connected in sequence. Below is the circuit diagram of the capacitor bank we have designed.

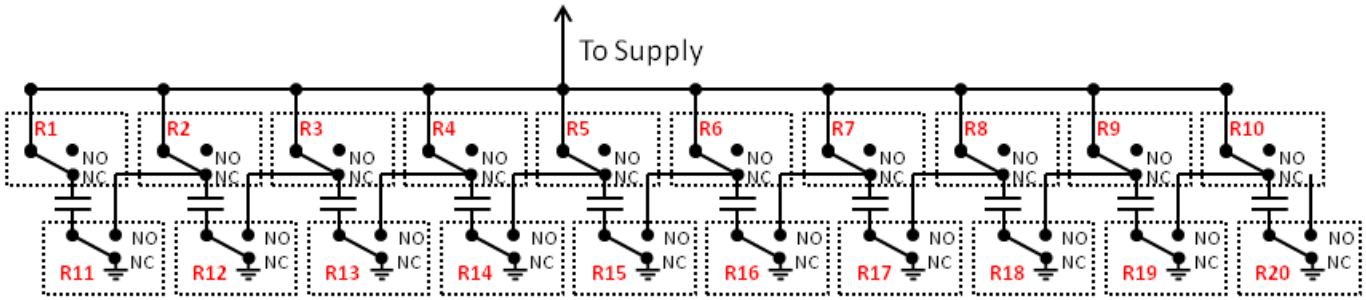

Fig-6: Design of Capacitor Bank

We have not shown here the energy coil of the relays for the simplicity. They should be considered connected properly. As we can see here that initially all capacitors are connected in parallel offering a total capacitance of **100µF**.

Algorithm to find the number of capacitors required to connect in series or parallel for a particular value of capacitance: once we have capacitance value then we need to know that in above design of capacitor bank out of 10 how many capacitors we required to connect in series and how many are required to connect in parallel.

In the value of capacitance value the number at tenth place is directly equal to capacitor required to connect in parallel i.e. for C = 25, Two will be the required no. of capacitors to connect in parallel.

So,

Parallel capacitors = no. at tenth place (19)

And by taking the inverse of No. at unit place multiplied by 0.1will give us the capacitors required to connect in series i.e. for C=25, it will be 1/(5*0.1) = 2.

So,

Series capacitor= 1/ (0.1 * no. at unit place) (20)

Here in case of float value chose nearest integer greater than float value. By using equation (19) and equation (20) we can find the no. of capacitance required to connect in series and parallel from the value of capacitance.

5. CONCLUSIONS

In this paper, we have proposed a distributed model of power factor correction system and their advantages over what is being used now days. We have also suggested a process of manufacturing of a very low cost, reliable and easy to install automated power factor correction system using ATmega16, 8 bit microcontroller from Atmel Corporation.

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