# DESIGN & DEVELOPMENT OF EMBEDDED APPLICATION SOFTWARE FOR INTERFACE PROCESSING UNIT (IPU)

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## Abstract

*The objective of this project is to design, develop and implement the Digital Glue Logic (DGL) in VHDL for Interface processing unit (IPU) Sub-system. The IPU sub-system consists of two major components, Blanking Interface Module (BIM) and Gyro Interface Module (GIM). The Digital Glue Logic for both the above modules is to be designed, developed and implemented individually in standalone mode and sequential integration of both the modules, porting on a Virtex-4 FPGA based XILINX evaluation platform.*

***Keywords***— *Power processor, BIM, GIM, Digital Glue Logic.*

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## 1. INTRODUCTION

Electronic Support Measure (ESM): ESM is a passive EW System that uses enemy transmissions to support surveillance operations by monitoring the electromagnetic (EM) spectrum.

IPU subsystem is part of ESM system. There are various systems on board any platform whose information is required by the ESM system which will process them for different ESM system requirements. The various systems which are found on board platform are Radars, Horizontal Gyro system, Vertical Gyro system, GPS, DATALINK II.etc.,. The information from these systems is very essentially required by any on board ESM system as part of its requirements.

Hence, it has become very essential that these on board systems need to be interfaced with the ESM system for different system requirements. Hence this has called for the need to design and develop an IPU subsystem which would take care of all the on board systems requirements interfaces with the ESM system.

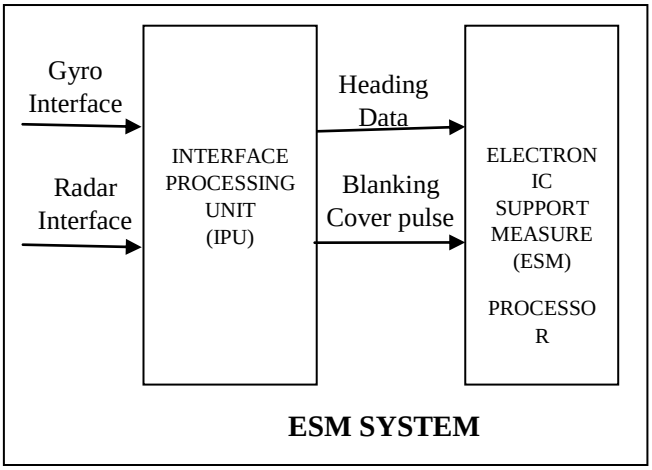


**Fig 1:** Block Diagram of ESM System

## 2. DESIGN

The design requirement specifications of IPU subsystem are, basically categorized into 2 types
(1) Hardware requirements
(2) Software requirements

### 2.1 Hardware Requirements

The hardware should be able to provide provision for,

### Gyro Interface

**Inputs:** It should be able to accept data either in analog form (synchro/resolver format either 1:1 or 1: 360) or in digital form.

**Outputs:**The output data is a 12 bit binary and hence it should provide an RS422 parallel interface to output this data to other subsystems for further processing.

### 2.2 Software Requirements

The software to be developed should be able to comply with the following functionality for the following interfaces appropriately. Here digital glue logic using VHDL implementation is developed for the two following modules namely,

### Radar Interface:

**Inputs:** It should be able to accommodate at least 10 nos. of analog Pretriggers from 10 on board radars. With amplitude range from +2V to +75V or -2V to -75V. The H/W should also be able to accommodate either positive or negative polarity pretriggers.

**Outputs:** The outputs generated are band wise Blanking cover pulses (BCP's) along with the respective composite blanking cover pulses based on three different bands. To output these BCP's an RS422 parallel interface to be provided in the IPU.
(a) Gyro Interface Module (GIM)
(b) Blanking Interface Module (BIM)

Finally the above two modules are integrated into a single software project

### Gyro Interface Module

**Inputs:** GIM can receive signals either the gyro in analog (1:1) form or in a digital form. The function of the GIM module is as follows.

If the GIM receives analog signals which are in either synchro/resolver form will first be converted into digital form of 12 bit binary data. Generally it is seen that the gyro information from the onboard gyro system will always have an offset in it due to various reasons. Hence next activity is to correct this offset (which is platform dependent), here the 12 bit binary data is corrected using the offset data depending on the mode of the polarity bit i.e., by either adding or subtracting the offset to/from the 12 bit binary data. Finally this 12 bit parallel binary corrected gyro data is sent to ES processor for further processing.

**Outputs:** The output data is a corrected 12 bit parallel binary data along with one data valid bit. It should provide an RS422 parallel interface to output this data to other subsystems for further processing.

### Blanking Interface Module

**Inputs:** The BIM module should be able to accommodate at least 10 nos. of analog Pretriggers from 10 on board radars. With amplitude can range from +2V to +75V or -2V to -75V. The H/W should also be able to accommodate either positive or negative polarity pretriggers.

**Outputs:** The outputs generated are band wise Blanking cover pulses (BCP's) along with the respective composite blanking cover pulses based on three different bands. To output these BCP's an RS422 parallel interface to be provided in the IPU.

## 3. GYRO INTERFACE MODULE

The 12 bit corrected Gyro data along with 1 bit valid data is used for Direction of Arrival (DOA) computation with reference to true north. Gyro data is required to compute the true Direction of Arrival (DOA) of the threat signal. Receiver with respect to the geographical/ true north and locate threat signals with respect to platform heading which is known as Relative DOA. The gyro data is added to this relative DOA to compute the True DOA with respect to geographical true north. This DOA based on true is displayed on the ESM display. Gyro data is generated by the gyro compass unit, which is available on board platform. If there is an error in the generation of the gyro data, it has to be corrected before it is added to the Relative DOA. This error can be +Ve or –Ve (The correctness of the gyro data is measured by monitoring the out of the gyro compass against each set value of the input).

The GYRO module is designed to find the true DOA of the threat signal. The inputs of the module are 12 bit gyro data and 12 bit gyro offset and polarity selection pin, clock and reset. And the outputs are corrected gyro data and valid bit

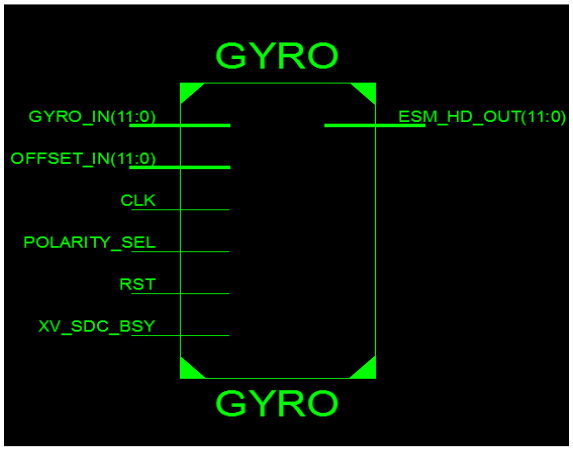


**Fig 2:** GIM Module

## 4. BLANKING INTERFACE MODULE

### 4.1 Purpose of Blanking

The objective of this module is to generate the band wise Composite Blanking Cover Pulses (BCPs) for the main transmission pulse of on board Radar, by taking the pre-trigger pulse as input from on board radars. The Blanking cover pulse is a TTL Pulse, which is used to shut off the ESM Receiver or electrically disconnect the antenna during on board radar transmission.

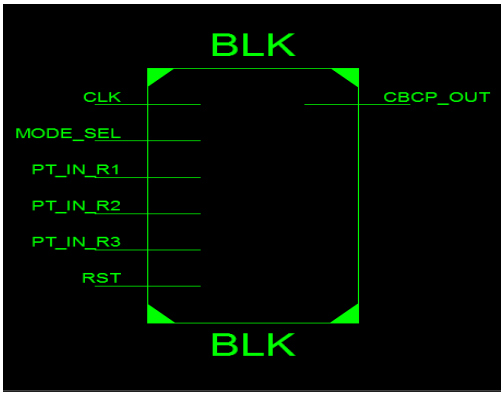


**Fig 3:** BIM Module

**Blanking is done for two reasons:**

1. To protect our own on board Electronic equipment (ESM Receiver Chain) from high power signals emitted by the on board radars. When the on board Radars are switched ON for their intended purpose, the ESM Receiver chain and other electronic equipments co-located on board platform will pick up these high power signals immediately and get burn electronically. This happens because, the RF and Microwave components used in the ESM Receiver chain will have the maximum power handling capability in the order of Watts, where as the output power emitted by the on board Radars will be in the order of Kilo Watts. So, they get burned electronically. To overcome this drawback we have to shut off the ESM Receiver or turn off the antenna during on board radar transmission.

2. To avoid processing of our own signals.When the on board Radars are switched ON for their intended purpose, the ESM Receiver co-located on board platform will pick up these signals and start processing it which, is of no use to the user as the main purpose of the ESM Receiver is to locate the source of threat signals.

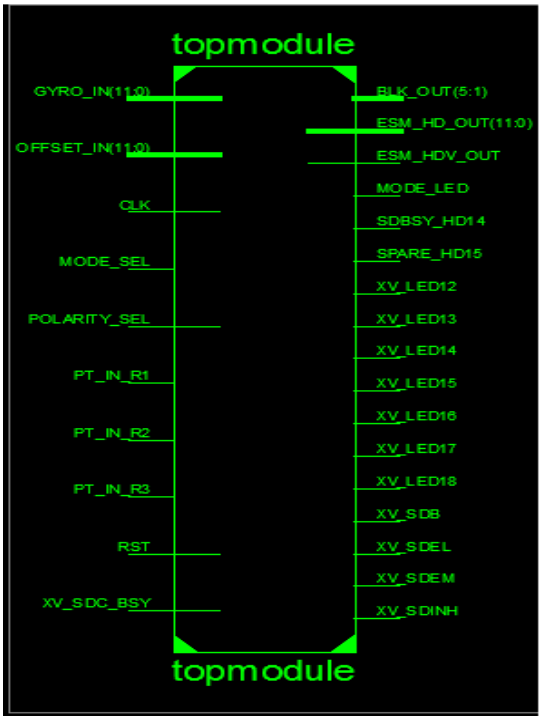


**Fig 4:** Intergation OF GIM And BIM Modules

## 5. RESULTS

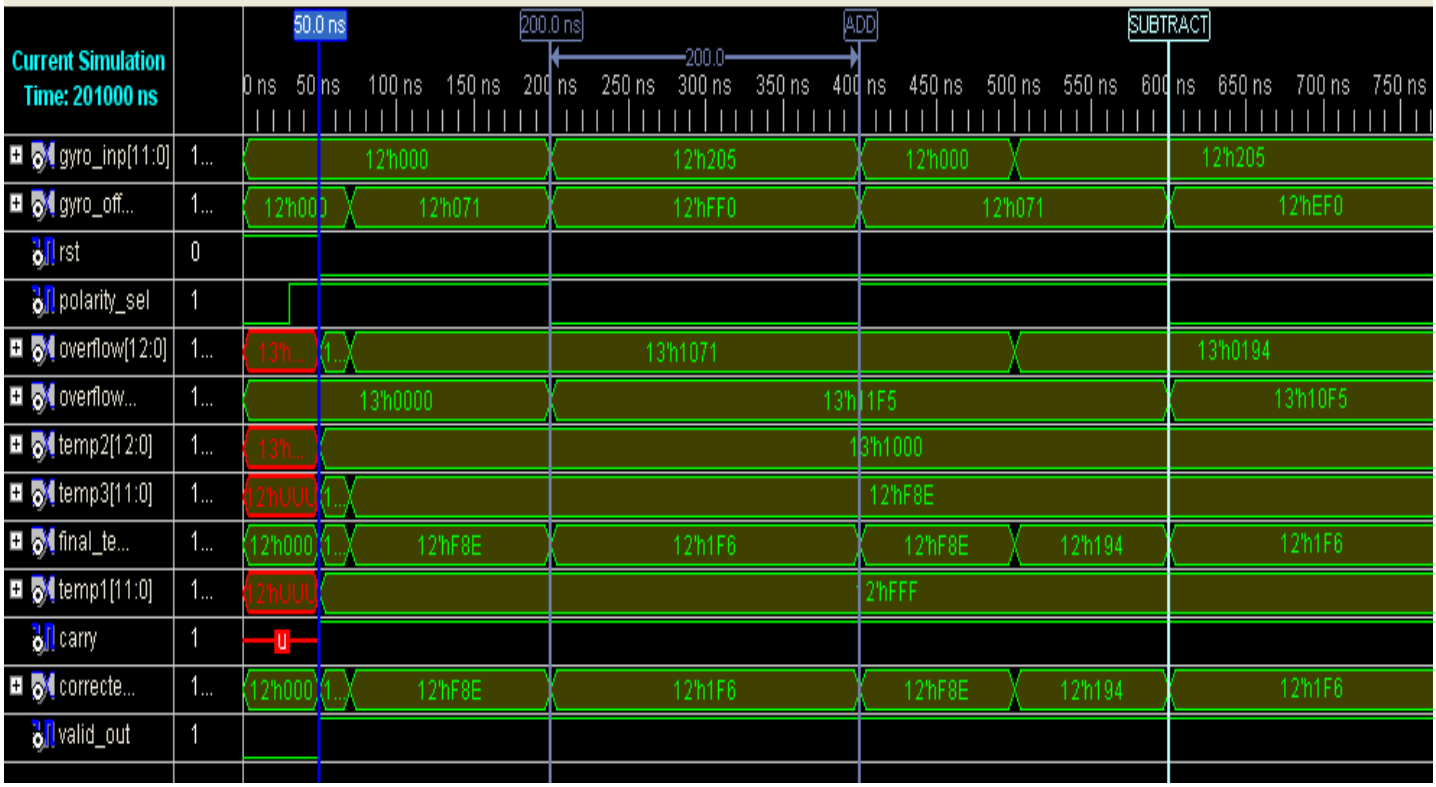


**Fig 5:** GIM Simulator Results

In GIM module the Gyro input data is corrected gyro offset data. The type of correction using can be either +ve or –ve correction. The polarity pin decides the type of correction to be implemented. The inputs are gyro_input and gyro_offset each of 12 bits, polarity_sel and reset pin.

When a polarity pin is high a –ve correction is applied. and is indicated by the marker and corrected value is indicated on 12 bit corrected gyro data.

When polarity pin is low a +ve correction is applied and is indicated by the marker the corrected gyro data is validated by comparing it with the specified values.If it is in the specified range then a valid bit is generated indicating a high on the output pin

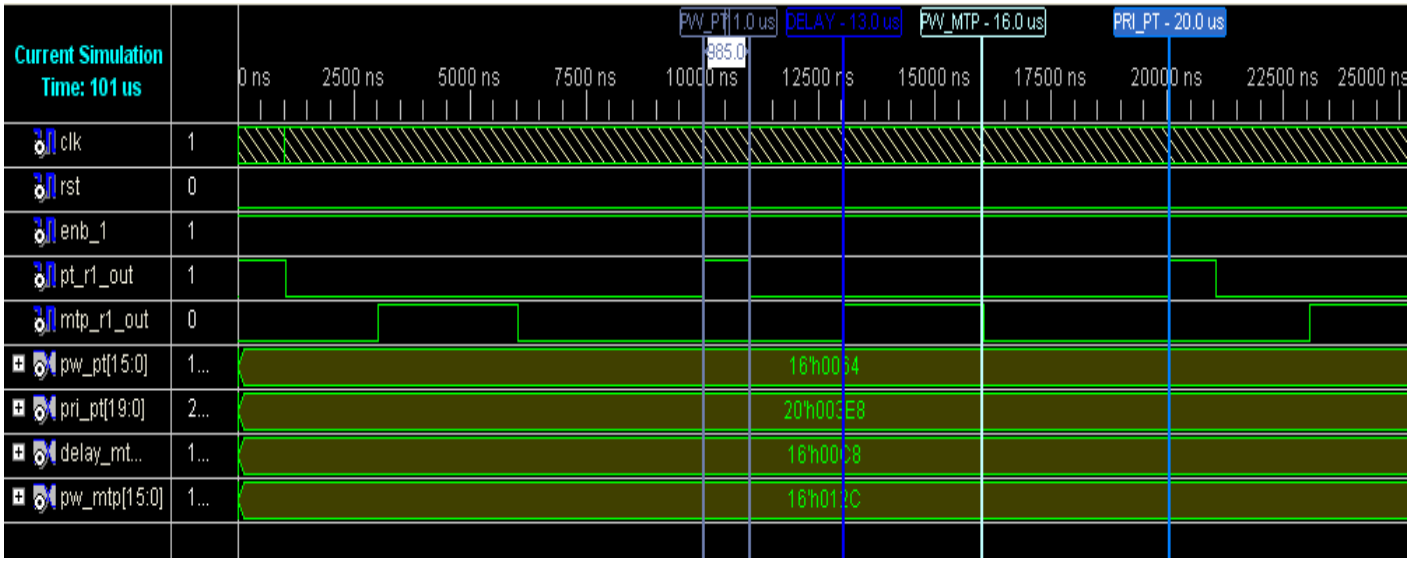


**Fig 6:** BIM Simulator Results

In this figure it describes the inputs such as clock and reset for free running clock generator. The enable is like switch and is kept high for circuit to be activated. The outputs are PT and MTP. PT pulse is generated for every PW and PRI period. The PW period is HIGH and PRI period is LOW. Thus it generates a continuous pulse. The MTP pulse is generated taking the reference trailing edge of PT pulse. The DELAY period is LOW and PW period is HIGH. Thus it also generates a continuous pulse. The parameters of PT and MTP are internal to the system so there are kept in constant in the code.

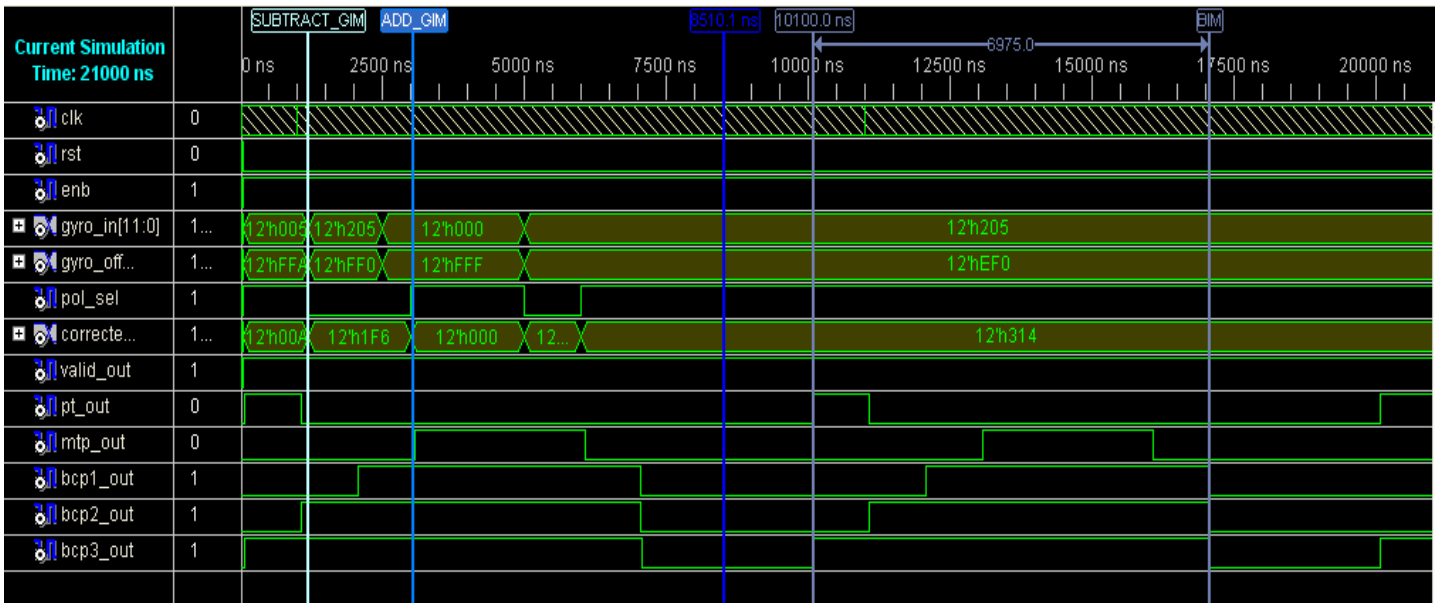


**Fig 7:** Simulation Results Of The Intergated Module

BIM and GIM modules can be intergated using structural design model. The inputs are same for each module as used previously. The outputs of the integrated module are independent.

## 6. FUTURE SCOPE

The IPU subsystem is compatible to interface data from various on board interfaces. In GIM module the offset gyro data is fixed for a speified onboard system thus using Flash PROM the offset gyro data is stored. The DGL is extended to the embedded processor using Ethernet.

## 7. CONCULSIONS

Design and implementation of Digital Glue Logic on Xilinx Platform using VHDL is presented. A core is designed for the IPU sub system for DGL.. The core is designed for each module individually and combined in one top module. For each module a test bench has been written to simulate each module and validate for its complete functionality. The designed core is synthesized and implemented in VIRTEX 4 FPGA board.

Main conclusions derived from the work are

- Designed and implemented BIM module and monitored the Bcps and validated for their functionality.
- Designed and implemented GIM module and recorded the corrected gyro data along with valid bit.
- Integrated both modules and simulated and implemented on VIRTEX 4 FPGA board.

## ACKNOWLEDGMENTS

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