MLGNR INTERCONNECTS WITH FINFET DRIVER: OPTIMIZED DELAY AND POWER PERFORMANCE FOR TECHNOLOGY BEYOND 16NM

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Abstract

Multi- layer graphene nanoribbon is emerging as a potential candidate for deep-nanometer interconnects due to its superior conductivity and current carrying capabilities. MLGNR showed superior performance over SLGNR for global interconnects. Also multi-gate devices such as FinFETs are the most promising building blocks in sub-micron technology. This paper combines these recent technologies of interconnects and devices and provides the analysis of delay and power performance of the combination. The driver-interconnect- load (DIL) system engaging FinFET driver with MLGNR interconnect is used for analyzing the performance.

Key Words: *FinFET, Graphene nanoribbon interconnect, deep sub-micron, Single layer GNR (SLGNR), Multi-Layer GNR (MLGNR), delay, power dissipation.*

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1. INTRODUCTION

In VLSI field, research is going on tremendously from last 4 decades. Due to the required performance increment in electronic gadgets and integrated circuits, a research pipeline is set in the field of semiconductor technology. Basically, this increase in performance is coming from the decrease in dimensions of devices in deep sub-micron regime [1]. There are plenty of strong candidates at device level in the present scenario but all are facing limitations imposed by interconnect technology. Any new technology that is advantageous in terms of power dissipation, performance, delay or crosstalk will have to be harmonized with an interconnect technology that provides similar performance parameters to avoid the variability issues due to interconnects [2].

The new candidates at device level in post CMOS era are CNFETs, TFETs, sub-threshold CMOS, Triple-Gate FET and FinFETs etc. As the resistance and capacitance values of different device technologies differ from each other, the constraints put by them on interconnects are also different. So, it is important to investigate the interactions of interconnects with all these emerging devices [3].

In recent nanoscale device dimensions, Cu interconnects are mostly affected by grain boundaries and sidewall scatterings [4]. So, the researchers are forced to find an alternative solution for global VLSI interconnects. Graphene is most promising interconnect material due to its inimitable physical properties that are higher current density, thermal conductivity and long mean free path [5]. Ballistic transport in graphene makes it suitable for interconnects as well as for switching transistors.

In this paper we have paired FinFET driver with MLGNR interconnect in driver-interconnect-load (DIL) system and analyzed their performance in terms of delay and power dissipation. The organization of the paper is as follows. Section 2 gives the brief overview of FinFET and Graphene nanoribbon technologies that are used in simulations of this paper. Section 3 emphasizes on the model of graphene as sub-micron VLSI interconnect. Section 4 throws light on the simulation setup used for our analysis. Results and their analysis are briefly explained in section 5 and section 6 concludes the paper.

2. TECHNOLOGIES USED

2.1 Driver and Load Technology: FinFET

FinFET has its technology roots in 1990s. The term FinFET is given by researchers of University of California, Berkeley. It is a non-planar, multi-gate transistor, built on SOI substrate. The unique characteristic of this device is that its conducting channel is wrapped under a thin silicon “fin” which forms the body of device.

The Berkeley team suggested that a thin-body FET structure would control short-channel effects and reduce leakage by keeping the gate capacitance in closer proximity to the whole of the channel. In 2012, Intel started using FinFETs for its future commercial devices. Intel's FinFET shape has an unusual shape of a triangle rather than rectangle and it is speculated that this might be either because a triangle has a higher structural strength and can be more reliably manufactured or because a triangular prism has a higher area to volume ratio than a rectangular prism thus increasing switching performance [6].

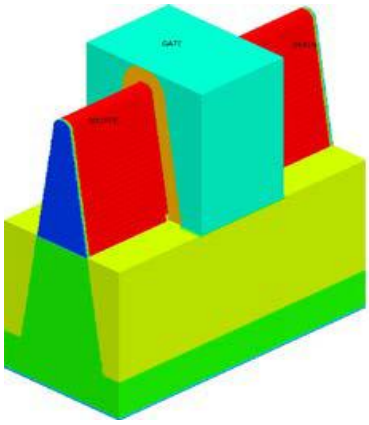

Fig -1: Structure of FinFET.

FinFETs are estimated to be up to 37% faster while using less than half the dynamic power or cut static leakage current by as much as 90%. FinFETs also promise to alleviate problematic performance versus power tradeoffs. Designers can run the transistors faster and use the same amount of power, compared to the planar equivalent, or run them at the same performance using less power. This enables design teams to balance throughput, performance and power to match the needs of each application [7].

2.2 Interconnect Technology: GNR

Graphene, a sheet of graphite, tightly packed into a 2D honeycomb lattice structure and mono-atomic thick building block of carbon allotropes, has emerged as a striking material of the sub-micron CMOS designing era [8]. GNRs can be constructed from unzipping of carbon nanotubes, so GNRs own properties similar to CNTs. It is a semiconductor with zero bandgap, phonon like 2D confined properties, linear energy dispersion, ambipolar charge transport, and a very high carrier mobility of 10^6 cm^2/V-sec at room temperature [9][10]. In a high quality graphene sheet, the mean free path (MFP) is ranging from 1-5 µm [11].

Due to its zero energy gap, graphene cannot be used directly to make transistor devices, so the logic applications [12]. So, a further confinement of the electrons of graphene in one of the in-plane directions is required and it results in graphene nanoribbons. These ribbons are strips of graphene with dimension less than 10 nanometers, so called Graphene nanoribbons [9]. GNR are classified as armchair and zigzag GNRs depending upon their termination style. Fig. 2 shows the structures of Armchair and Zigzag GNRs.

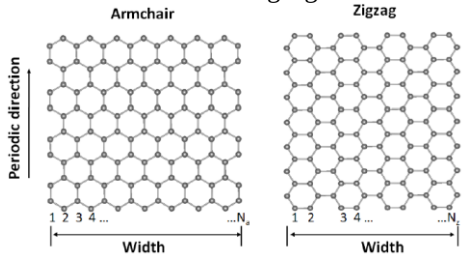

Fig -2: (a) armchair, (b) zig-zag

Width of armchair GNR is decided by the number of hexagonal carbon rings or generally referred as dimer lines (N_a) across the ribbon. Similarly width of zig-zag GNR is dependent on the number of zig-zag chains (N_z) across the ribbon [13]. The ac-GNRs can be again classified as metallic and semiconducting based on number of hexagonal rings (N_a) while zz-GNRs are always metallic [14].

The GNR interconnects can be classified as single layer GNR (SLGNR) and multilayer GNR (MLGNR) depending upon the number of layers [15]. Due to their higher resistance SLGNRs are not suitable for the interconnect applications but as MLGNRs have multiple parallel conduction paths so their resistance decreases by the concept of parallel resistances and thus they are well suited for the interconnect applications in sub-micron VLSI circuits [16].

3. RLC MODEL OF GNR INTERCONNECTS

The distributed *RLC* model for MLGNRs is defined in Fig. 3. The distributed capacitance of GNRs comprises of electrostatic and quantum capacitances and the distributed inductance comprises of the magnetic and kinetic inductances. This is the same situation as in CNTs [17].

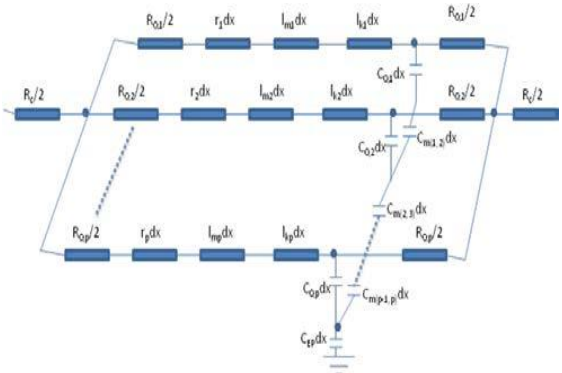

Fig-3: Distributed RLC model of MLGNR interconnect

The value of quantum contact resistance R_Q, Quantum and electrostatic capacitances C_Q and C_E respectively and kinetic and magnetic inductances l_K and l_M can be expressed by [11, 18, 19]

$$R_Q = (h/2q^2)/N_{ch}N_{layer} = 12.94\ K\Omega/N_{ch}N_{layer} \quad (1)$$

$$C_Q = N_{layer}N_{ch}4q^2/hv_f = N_{layer}N_{ch} * 193.18\ aF/\mu m \quad (2)$$

$$C_E = \varepsilon_0 * w/d\ aF/\mu m \quad (3)$$

$$l_K = (h/4q^2v_f)/N_{layer}\ N_{ch} = 8.0884/\ N_{layer}N_{ch}\ nH/\mu m \quad (4)$$

$$l_M = \mu_0 * (d/w)\ nH/\mu m \quad (5)$$

$$N_{ch} = N_{ch,electron} + N_{ch,hole}$$

$$N_{ch} = \Sigma\ [1 + \exp((E_{n,electron} - E_F)/k_BT)]^{-1} + \Sigma\ [1 + \exp((E_F - E_{n,hole})/k_BT)]^{-1} \quad (6)$$

, where
N_{ch}= number of conducting channels in one layer,
N_{layer}= number of GNR layers,
h = Plank's constant =6.626×10^{-34} J.s, and
q = electronic charge =1.6×10^{-19} C.
v_f= Fermi velocity = $8* 10^5$ m/s for GNR
E*n*,electron (E*n*,hole) = minimum (maximum) energy of the *n*th conduction (valence) sub-band.
In MLGNRs, mutual inductance and mutual capacitance exists between two layers due to the electron tunnel transport phenomenon. It is given by [20]

$$l_{mlayer(j-1,j)} = \mu_0 *(\partial /w)\ nH/\mu m \quad (7)$$

$$C_{mlayer(j-1,\ j)} = \varepsilon_0*(w/\partial)\ aF/\mu m \quad (8)$$

, where d is the distance of GNR interconnect from ground plane, ∂ is distance between two adjacent layers, μ_0 and ε_0 are the magnetic permeability and electrostatic permittivity of free space respectively.

The resistance of zz-GNRs is smaller than that of the corresponding ac-GNRs for the widths less than 45 nm. The way to improve multi-layer GNR conductance is to improve the specularity (smoothness) p of edges [21].

It has been also proved previously that the conductivity of graphite can be enhanced by intercalation doping by exposure to dopant vapor (e.g., AsF5). So, the intercalation doping has been proposed to boost the conductance of multilayer GNRs, and edge specularity effects for multilayer GNRs have been studied [21] [11]. So, this doping enhances the place of GNRs as interconnects in today's sub-micron VLSI area.

4. SIMULATION SETUP

This paper analyses the performance of MLGNR interconnects with FinFET driver in terms of the delay and power dissipation of the setup. The number of layers of the MLGNR are varied at the global interconnect lengths (100µm to 1000µm). Width is varied from 10 nm to 100 nm. The setup is employing FinFET driver at 16nm and 7nm node for the delay estimation and simulations are done using predictive models given by BSIM-CMG by BSIM group at University of California, Berkeley [22]. The above described RLC models are used for the parasitic values extraction of GNR interconnect. The simulation setup is using the supply voltage VDD = 0.7 V.

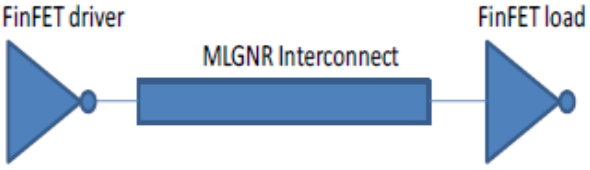

Fig-4: A MLGNR interconnect and FinFET driver system.

5. RESULTS AND DISCUSSIONS

TSPICE simulations are performed by using above mentioned simulation setup. FinFET is taken with number of fins M=3 and M=5. Simulations are performed for the MLGNR layers varying from 10 to 100. The width of interconnect is varied from 10 nm to 100 nm with lengths ranging from 100µm to 1000µm. Chart 1 through chart 6 shows the delay variation with varying widths at GNR interconnect lengths of 100, 200, 400, 600, 800 and 1000µms respectively. The number of layers are fixed at 10 in this analysis for number of fins M=3 and M=5 both. The results, clearly shows that delay are almost constant if the number of layers is constant and it is not dependent on the width. But delay is dependent on number of fins and increases with the increment in M. However, chart 7 and 8 shows the delay variation, at lengths 400µm and 1000µm respectively, with respect to number of layers variation and there are graphs plotted for all widths ranging from 10 to 100nm. These charts are plotted for number of fins M=5 and shows decrement in delay with increment in number of layers and it is due to the fact that increasing number of layers reduces the parasitic resistance. However, this decrease in delay is almost similar for all widths.

The increasing thickness of GNR by increment in number of layers also increases the conducting channels which results in lesser delay. So, MLGNR with large number of layers has a smaller delay as compared to less number of layers [5]. Chart 9 and 10 shows delay variation for M=3 and M=5. These plots show that the delay range is increased with the increment in number of fins. This is due to the fact that fins are treated as gates and at each gate some delay parasitic are present which add on in the delay time. Therefore, the charts 1 to 10 concludes that in this FinFET DIL system with GNR interconnect the delay is dependent on number of layers as well as number of fins of driver and load but is almost independent of width.

Chart 11 shows the delay vs length of interconnect plot. This plot shows increment in delay with increment in length, which is obvious as the length of the wire increases the parasitic resistances and capacitances increases which results into delay increment. But, this delay is less (in pico-seconds) in comparison with conventional devices of VLSI used with GNR interconnects.

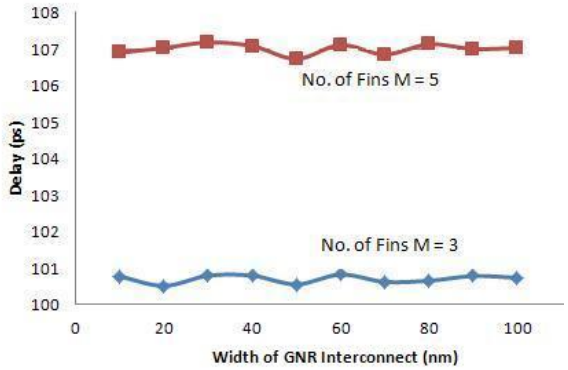

Chart -1: Propagation delay variation with varying width of MLGNR at N_{layer} =10 and L_{int} =100µm

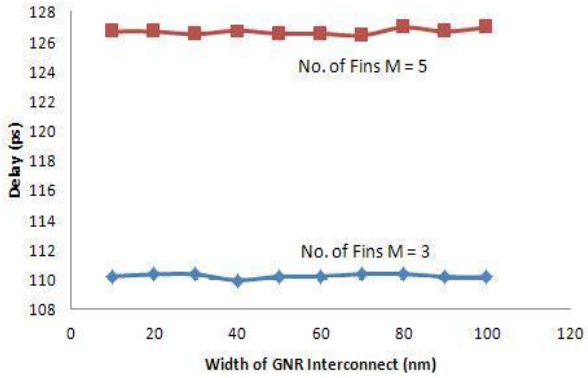

Chart -2: Propagation delay variation with varying width of MLGNR at N_{layer} =10 and L_{int} =200µm

The power dissipation for this setup is almost constant between 1.91nW to 1.89nW for M=3 and between 3.19nW to 3.16nW for M=5. This power dissipation is decreased in comparison to DIL system of CMOS and it is clear that this decrement is due to the usage of FinFET because as stated in [7] the dynamic power of FinFETs is 50% less than that of other conventional devices used in VLSI till date.

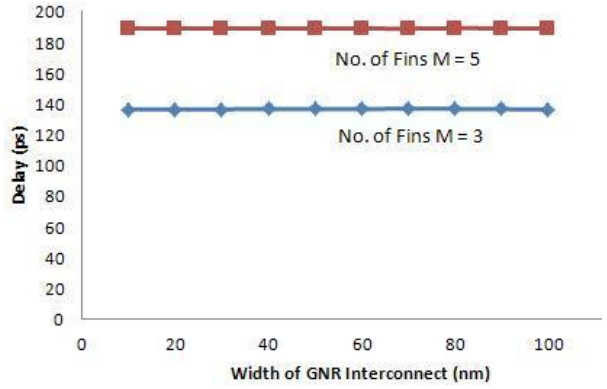

Chart -3: Propagation delay variation with varying width of MLGNR at N_{layer} =10 and L_{int} =400µm

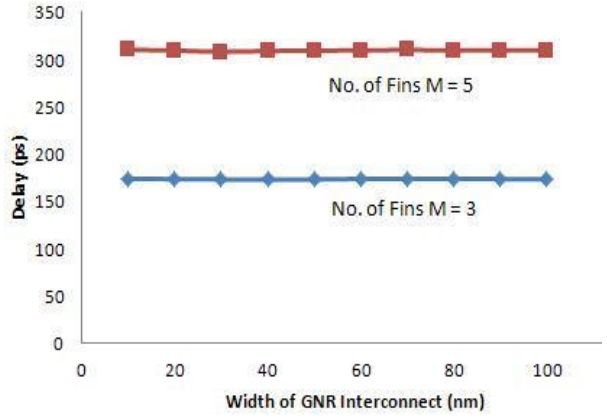

Chart -4: Propagation delay variation with varying width of MLGNR at N_{layer} =10 and L_{int} =600µm

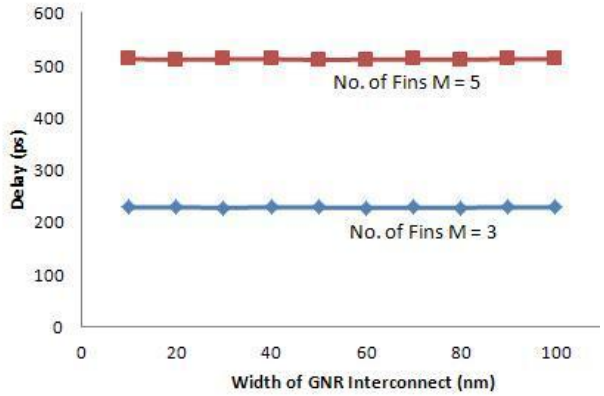

Chart -5: Propagation delay variation with varying width of MLGNR at N_{layer} =10 and L_{int} =800µm

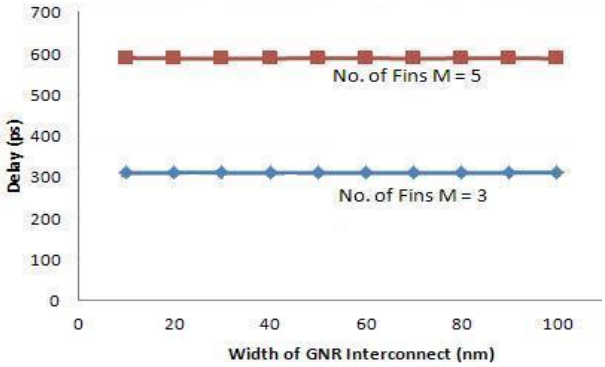

Chart -6: Propagation delay variation with varying width of MLGNR at N_{layer} =10 and L_{int} =1000µm

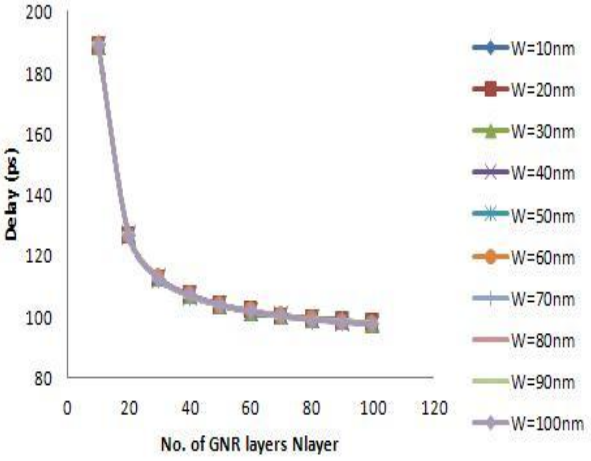

Chart -7: Propagation delay variation with varying MLGNR layers for widths from 10nm to 100nm, L_{int} =400µm and M=5

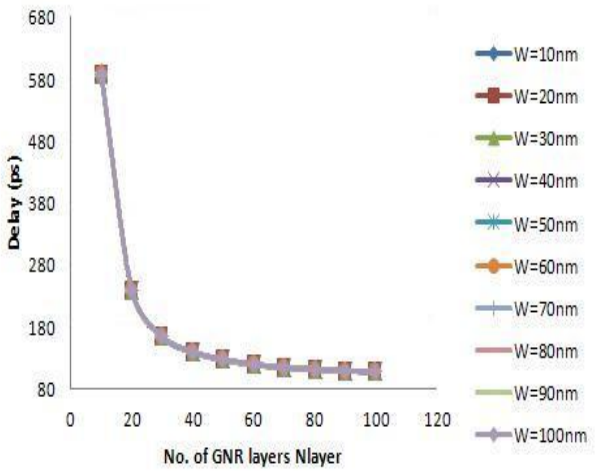

Chart -8: Propagation delay variation with varying MLGNR layers for widths from 10nm to 100nm, L_{int} =1000µm and M=5

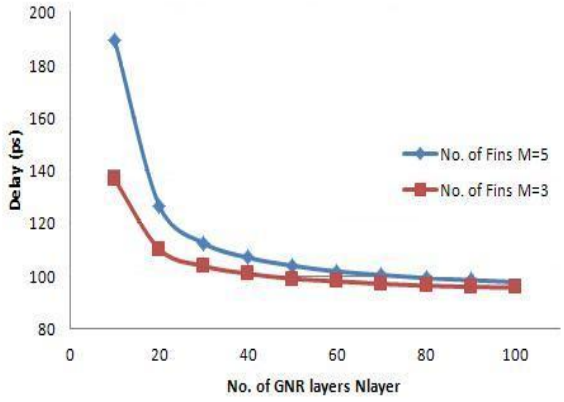

Chart -9: Propagation delay variation with varying MLGNR layers for W_{int} =10nm, L_{int} =400µm (both for M=3 and M=5)

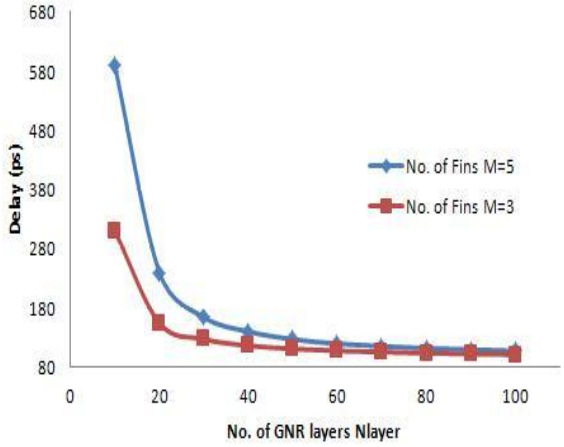

Chart -10: Propagation delay variation with varying MLGNR layers for W_{int} =10nm, L_{int} =1000µm (both for M=3 and M=5)

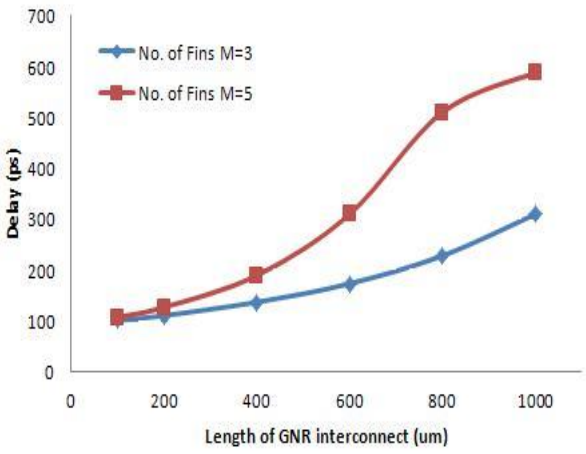

Chart -11: Propagation delay variation with varying lengths of MLGNR for W_{int} =50nm, N_{layer} =10µm (both for M=3 and M=5)

Table 1 shows the improvement in delay for MLGNR (N_{layer} =100) in comparison with lower number of MLGNR layers. This comparison is shown in terms of percentage improvement. Noteworthy improvement in delay is witnessed for longer interconnect length.

Table-1: Percentage Improvement in Propagation Delay for Higher Number of MLGNR Layers at Global Interconnects Level

Interconnects lengths (µm)	% improvement in delay for MLGNR N_{layer} = 100 as compared to MLGNR with N_{layer}								
	10	20	30	40	50	60	70	80	90
100	8.49	3.84	2.01	1.62	0.95	0.54	0.35	0.23	0.11
200	17.26	7.26	4.08	2.79	1.74	1.19	0.80	0.44	0.28
400	43.35	15.68	8.66	5.68	3.90	2.75	1.63	0.80	0.56
600	77.96	25.18	13.66	8.30	5.41	3.43	2.11	1.15	0.47
800	130.49	38.14	18.55	11.36	7.44	5.02	2.44	1.91	0.65
1000	207.45	52.36	25.73	14.76	9.63	6.15	4.11	2.70	1.12

6. CONCLUSIONS

The propagation delay of MLGNR interconnect with FinFET driver setup has been studied and it can be concluded from the results that MLGNRs are favorable candidates to be used with the new device technology. It has been observed that the MLGNR with higher number of layers can reduce delay by 112% as compared to the lower one. So, the MLGNR with higher number of layers can be considered as emerging material for interconnect in pace with the shrinking technology if they are used in finest manner. Also when this interconnect option is used with the upcoming new transistor technology FinFET, it has shown positive results in terms of delay as well as power dissipation. As, FinFET technology comes with the option of multiple number of gates, it is very helpful when the performance of circuit comes into picture. Researchers can optimize the number of fins with the accepted delay of the circuit and hence enhance the performance of sub- micron integrated circuits. The above results shows that the combination of FinFET with GNR interconnects can provide suitable option for the nanotechnology regime of VLSI.

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