DESIGN OF LOW POWER BARREL SHIFTER AND ROTATOR USING TWO PHASE CLOCKED ADIABATIC STATIC CMOS LOGIC

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Abstract

This paper presents low power operation of barrel shifter and rotator which are designed and simulated in 2 phase clocked adiabatic static CMOS logic. The power consumption of the circuits is compared with that of static CMOS logic. A barrel logic right shifter, a right rotator and shift/rotator are simulated in 45nm CMOS process technology. A mux based design is used for all the above circuits. The 2PASCL circuits are observed to have low power consumption while compared to circuits which are simulated using static CMOS logic. The power consumption of 2PASCL circuits are reduced by 69.67% compared to static CMOS logic. From the simulation results it is observed that the logic circuits which use 2PASCL logic can be used for low power applications.

Keywords: *barrel shifter, logical shift, rotation, adiabatic, two phase clock.*

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1. INTRODUCTION

With the invention of new technologies the usage of electronics devices has been increased. For every application it is necessary to find out an energy and area efficient integrated circuit design. The researcher's interest is to develop a technically acceptable VLSI design with low power consumption. Mostly for digital circuit's complementary metal oxide semiconductor (CMOS) logic is used. Since power consumption is proportional to the square of the power supply, voltage scaling is the easiest remedy for the above problem. While the supply voltage is scaled down, the threshold voltage is also reduced and it results in increased leakage current caused by sub threshold conduction. [1].

For past few years adiabatic logic, which are working on the basis of energy recovery, is being used for low power applications. Several diode based adiabatic logic families has been proposed and they are showing better performance. But it is observed that these diode based adiabatic families provides less output amplitude and some amount of power is dissipated across the diodes which are in the charging path [2] since the current is flowing through both the transistors and the diodes. In 2PASCL the circuit is designed such that charging occurs only through transistors.

The remainder of the paper is divided in to 4 parts. Section II explains about the 2 phase clocked adiabatic static CMOS logic. Section III presents the schematic and the operation of the circuits discussed in this paper. Section IV presents the results and discussion and the last session gives the conclusion.

2. TWO PHASE CLOCKED ADIBATIC CMOS STATIC LOGIC

Fig 1: shows a 2PASCL inverter. It is similar to static CMOS inverter but the working is based on adiabatic energy recovery [2]. Instead of dc supply voltage and ground, two sinusoidal waves namely phi and phi_bar are used as power supply. These split level sinusoidal waves are out of phase to each other [2]. Two MOSFET diodes are present, one is connected between output node and the power supply phi and other one is between NMOS tree and the power supply phi_bar. Here power dissipation is reduced by designing the charging path excluding diodes. The purpose of diodes is to recycle the charge from output node.

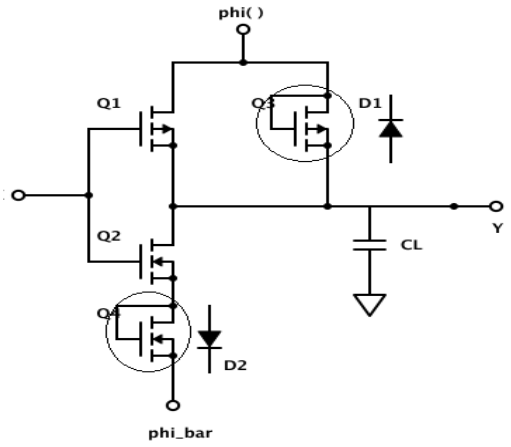

Fig-1:2PASCL inverter

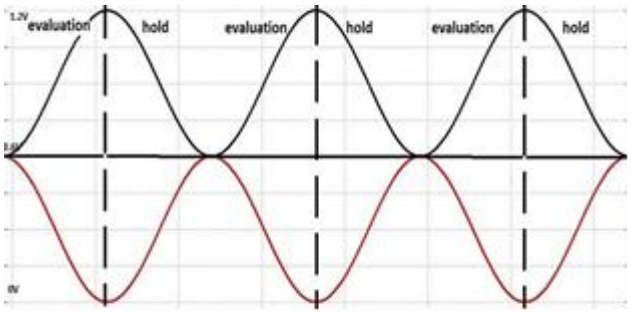

Fig-2: Power clocks phi and phi_bar

The two sinusoidal waves which are used as the power supply clocks are shown in fig2. Both are out of phase to each other. The voltage level difference between phi and phi_bar is Vdd/2 and the peak to peak value of these sinusoidal waveforms is 0.6V. The voltage difference between the two power supplies are very less, which leads to a reduced charging and discharging activities. Since these waves replace Vdd and Gnd, the substrate of pMOS and nMOS transistors can be connected to phi and phi_bar respectively [4]

2.1 Circuit Operation

The circuit operation can be illustrated in two phases, evaluation and hold. As shown in fig2: in evaluation phase, phi swings up and at the same time phi_bar swings down. In hold phase, phi and phi_bar swings down and up respectively. The circuit works as explained below. In evaluation phase, if the output node is in LOW state and at the same time, if the pMOS tree is happen to be turned ON , charging of the capacitor will occur which leads to a HIGH state at the output node. If the output node is at logic HIGH state and nMOS tree turns ON, discharging occurs through nMOS tree and the diode D2. For other two conditions, such as output node is in logic LOW state and nMOS tree is on, and output node is in logic HIGH state and pMOS tree is ON no transition occurs [4].

During hold phase there is no transition when the output node is in logic LOW state and nMOS tree turns ON. When pMOS is in ON state and output is in logic HIGH state, discharging will occur through D1 [4]. Due to the absence of diode in the charging path the 2 PASCL circuit dissipates less power compared to other diode based adiabatic logic families in which diodes are present in both charging and discharging path.

3. BARREL SHIFTER

Shifters are the vital component in general purpose processors and DSP processors. Shifters are needed for scaling of results and/or operands during computations in order to avoid the accuracy problems due to overflow and under flow [7]. When general shift registers are used for shifting purpose, speed of computation will be less since **in** one clock cycle only one bit will be shifted. So conventional shift registers cannot be used for complex computations since it slows down the processor. The barrel shifter/rotator is a combinational logic circuit which is capable of rotate/shift more than one bit in a single clock cycle. Because of this capability barrel shifter/rotator are used in applications where the speed of operation is the main goal. In this paper a mux based design approach is used and the power consumption is compared with that of static CMOS logic

3.1 2:1 Multiplexer

A 2:1 multiplexer is used as the basic component in the design of the shifter and rotator. A basic 2:1 multiplexer is shown in fig:3. A multiplexer select any one input from a set of inputs and pass it to the output node. A select input decides the input to be selected and given to the output. For a 2:1 multiplexer, if I0 and I1 are the inputs and S is the select input, output Y is given by:

$$Y= \acute{S}I0 + SI1 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 1)$$

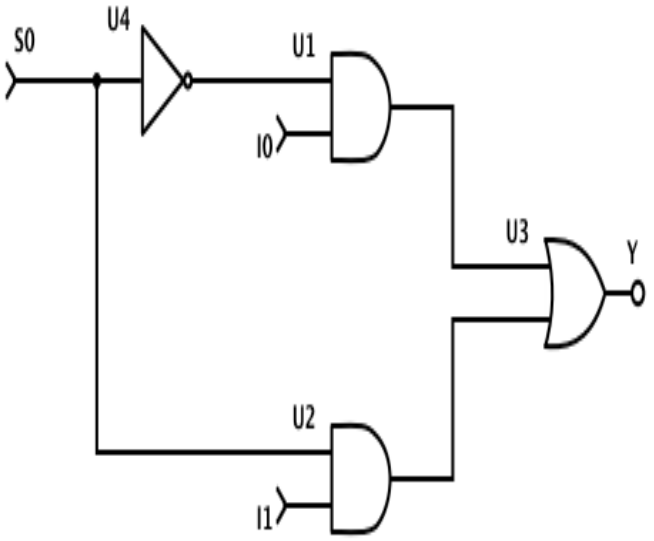

Fig-3: Schematic diagram of 2:1 mux

The schematic circuit of 2:1 mux is shown in fig3 which is made using AND gates and OR gate. The barrel shifter and rotator circuits are designed using 2:1 mux.

3.2 Shifter

Fig 4 illustrates an 8 bit logical right shifter. It has n bits of data inputs represented by A= a7 to a0 and n bits of data output Y= y7 to y0, the amount of data bits to be shifted is based on control signals b2 b1 b0. It has three mux based stages and in each stage 8 multiplexers are present. For each stage the amount of data to be shifted or rotated is curbing by b_k. if b_k =1 the data input to that stage is shifted by 2^k bits, otherwise data is unchanged. An m bit logical right shift

operation shifts the data to the right by m bits and the upper m bits of the result is set to zero [6]. For instance if the input to the shifter is a7a6a5a4a3a2a1a0 and b2b1b0= 100, then input is logically shifted by 4 bits and output Y = 0000a7a6a5a4.

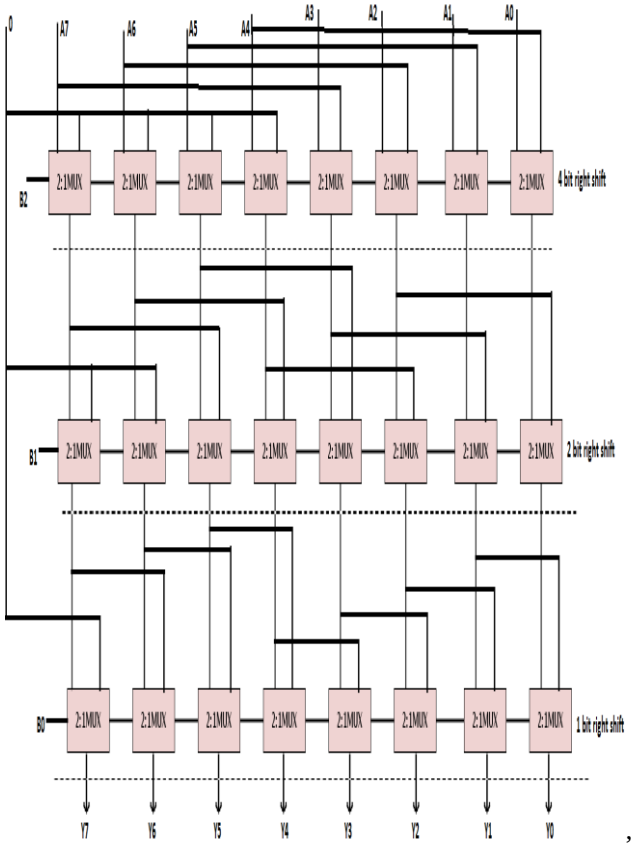

Fig-4: Schematic of 8 bit logic right shifter

3.3 Rotator

Fig 5: shows an 8 bit right rotator. During an m bit data right rotation the data is shifted to right by m bits and the lower m bits of A is placed at upper m bits of result [6]. For instance if A = a7a6a5a4a3a2a1a0 and b2b1b0= 100, then input is rotated by 4 bits and output Y = a0a1a2a3a7a6a5a4.

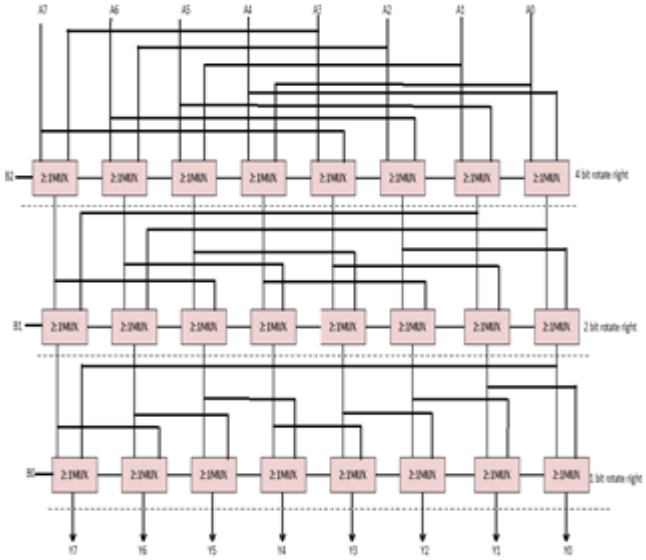

Fig-5: Schematic of 8 bit right rotator

3.4 Shifter/Rotator

A shifter/rotator performs both arithmetic shift and rotation operations. Fig 6: shows an 8 bit arithmetic right shifter and rotator. There are three stages of multiplexers for 4bit, 2bit and 1 bit shift/rotation. A multiplexer output decide the operation to be performed i.e., shift or rotation. Inputs to this mux are 0 and a7. Logical right Shift operation is performed if the mux selects 0.

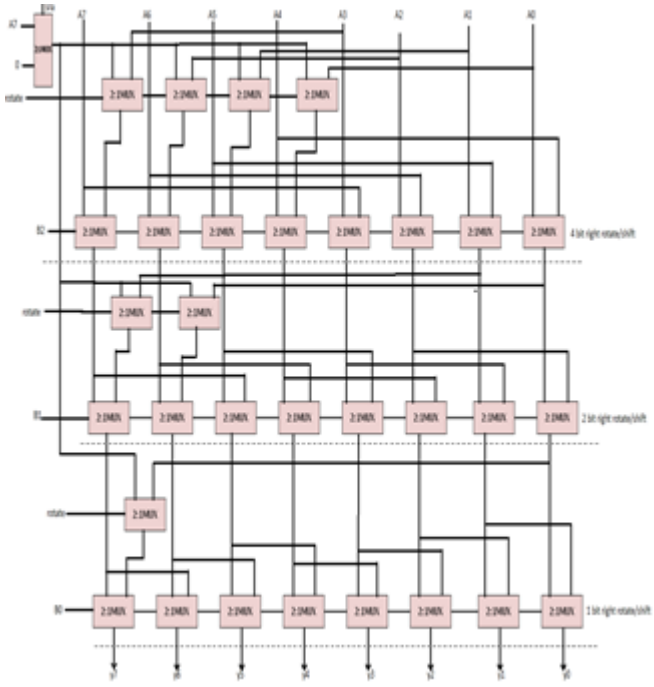

Fig-6: 8 Bit right Shifter/Rotator

4 SIMULATION RESULTS AND DISCUSSION

The circuits are simulated in 45nm CMOS process technology in Cadence Virtuoso. The sinusoidal waves of frequency 400 MHz are applied as power clocks. For each circuit binary inputs are applied to check the correctness of the circuits. Power consumption of all circuits is measured at 400 MHz clock frequency.

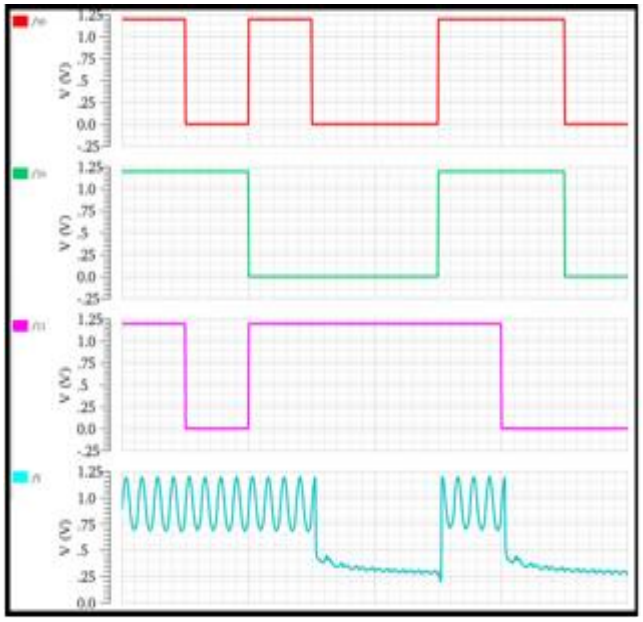

Fig-7: simulation result of 2:1 multiplexer

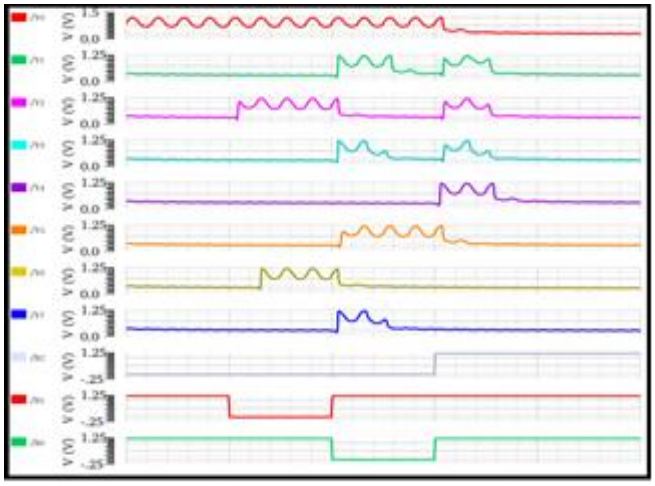

Fig-8: Simulation results of 8 bit right shifter

Fig 8: shows the simulation results of 8bit right shifter. The first set of inputs: A= 0001110 and the control vector B = 011. The input is right shifted by 3 positions and the output Y= 00000001.

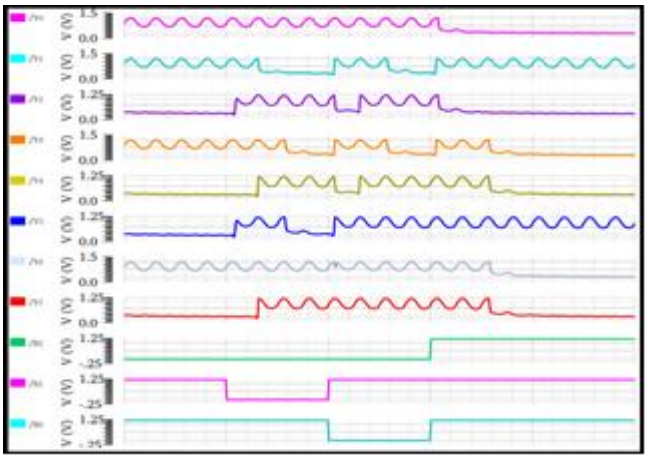

Fig- 9: Simulation results of 8 bit right rotator.

Fig 9: shows the simulation results of 8 bit right rotator. The first set of result corresponds to A= 01011010, B = 011 and Y = 01001011

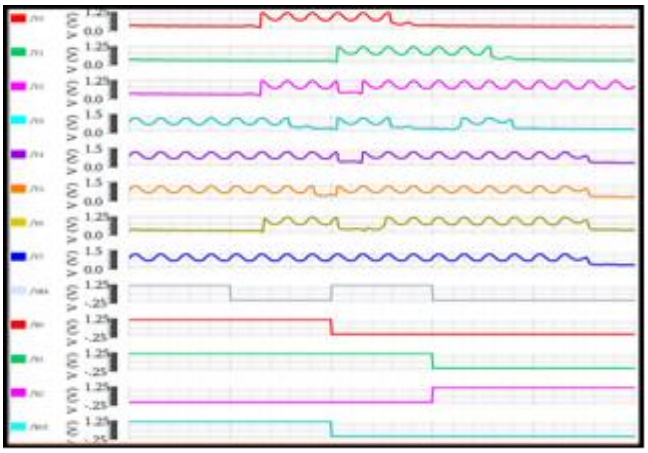

Fig- 10: Simulation results of 8 bit right shift/rotator

Fig 10: shows the simulation results of 8 bit right shift/rotator. The first set of result corresponds to A= 11000101, B = 011 and Y = 10111000.

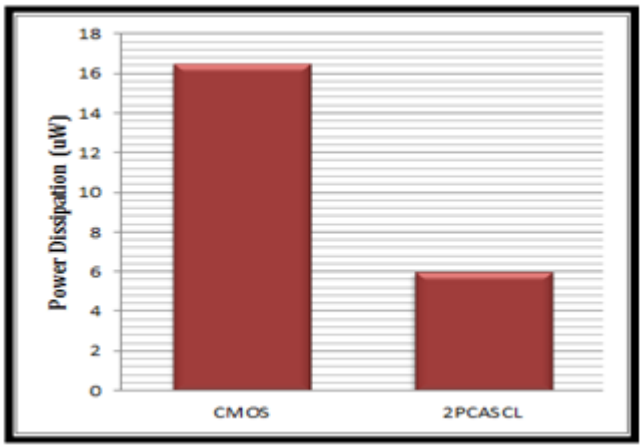

Fig -11: Power comparison chart of barrel right rotator

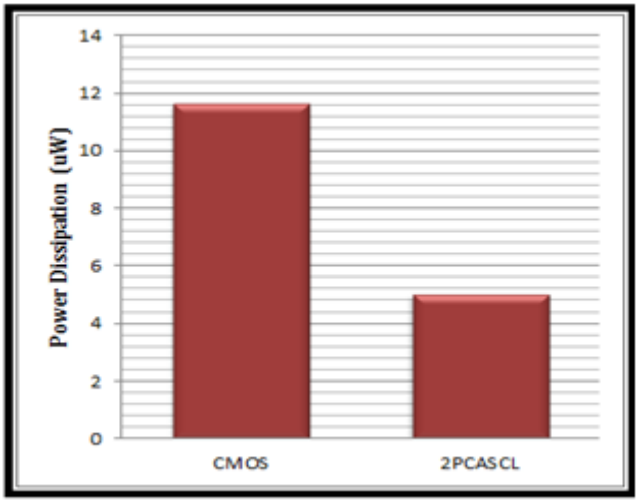

Fig- 12: Power comparison of barrel right shifter

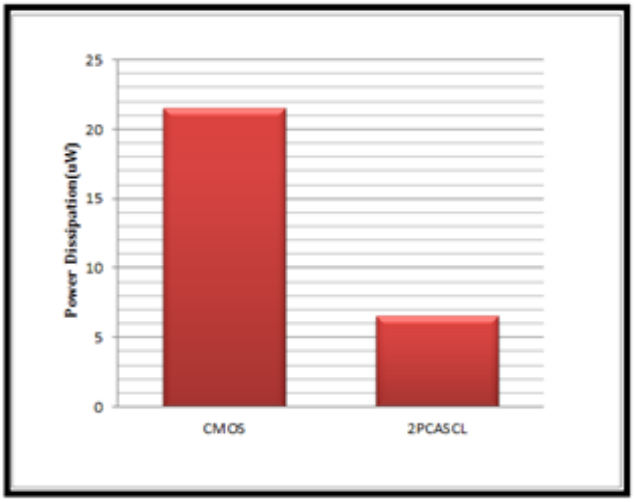

Fig-13: Power comparison of barrel shifter and rotator

Table 1: Power comparison of 2PASCL circuits with Static CMOS logic circuits

Architectures	Power Dissipation (µW)	
	Static CMOS	2 PASCL
BARREL RIGHT SHIFTER	11.62	5.019
BARREL RIGHT ROTATOR	16.46	6.01
BARREL RIGHT SHIFTER/ ROTATOR	21.55	6.545

5. CONCLUSIONS

In this paper low power operation of barrel shifter and rotator are described. The circuits are designed using 2 PASCL and the power dissipation of the circuits are compared to static CMOS logic. From the power comparison table (Table1) it is clear that the 2 PASCL logic circuits provides very less power compared to static CMOS logic. 2PASCL logic can be used for the circuits where low power consumption is a main goal. Barrel shifters designed using 2PASCL can be used in DSP processors and microprocessor where high speed and low power are needed.

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BIOGRAPHIES

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Dr. T. Vigneswaran received the graduate degree in Electrical and Electronics Engineering from Bhartidhasan University in 2000, M.E (VLSI Design) from college of engineering, Guindy Anna University in 2003 and Ph.d degree in Low power design from SRM University. His research interest includes different aspects of Low power design and high speed algorithm and architecture development He is a member of Indian Science Congress. Presently he is working as a professor, SENSE Department in VIT University.