

SET and SEU Analysis of CNTFET Based Designs in Harsh Environments

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Abstract

Over the past decade CNTFET has become one of the strong contender to replace Silicon by offering high performing power efficient nanoelectronics. However, no study has been published that evaluates CNTFETs based designs for SETs and SEUs due to radiation. This paper presents a comparative analysis of existing designs of latches and logic circuits using CNTFETs (32 nm Stanford models) and MOSFETs (45nm IBM FDSOI) for power, performance and radiation robustness. In the analysis CNTFET logic gate designs demonstrated on an average 45% improved resilience to SETs as compared to MOSFET based designs. CNTFET's energy and delay metrics for latches showed an improvement by two orders over MOSFETs with higher robustness. In the interconnect crossbar analysis, the CNTFETs implementation showed better resilience in minimizing the effect of SET transients by occupying 25% lesser area and consuming 4 times lower energy than MOSFETs implementation to handle same levels of Q_{crit} .

Key Words: CNTFETs, Single Event Upset (SEU), Single Event Transient (SET), Radiation Robustness

1. INTRODUCTION

The limitations of Silicon based technology such as increased leakage currents, low drive capability and low ON-current has forced the semiconductor industry to look for an alternative beyond Silicon. Single-Electron Transistor (SET), InGaAs transistor, Rapid Single-Flux Quantum Logic, Quantum Cellular Automata (QCA) and Carbon Nano Tubes (CNT) are among the investigated solutions. However, CNTs implemented with innovative process enhancements have shown to overcome the limitations in developing nanoelectronics.

Since the first CNTFET was reported in 1998 tremendous research work has been carried out in the field of CNTFET science and technology including materials, devices and circuits [1-3]. They have diameters between 1 to 3 nm and having lengths up to several microns. CNTs have been utilized to build both low-resistance high-strength interconnections and highly scalable low-power Carbon Nano Tube Field-Effect Transistors (CNTFET). The unique properties of Carbon Nano materials, in particular Single-Walled Carbon Nano Tubes (SWCNTs), have gained much attention due to their potential as high-performance device [4]. The improved channel transport and high gate capacitance of the CNTFETs fuelled a threefold increase in the ON-current when compared to MOSFETs. Their compatibility with high k-dielectrics is a huge advantage. In addition CNTFETs have four times higher transconductance when compared to MOSFETs. Further, for reliable electronics with CNTFETs, active research is being carried on to overcome the listed challenges. They include: 1) Perfect alignment and positioning of CNTs; 2) Chirality control for metallic or semiconducting properties; and 3) Performance variations; 4) Yield reduction, and 5) Increased susceptibility to noise

1.1 Physical Features of CNTFETs

CNTFET is a Field-Effect transistor that makes use of a single Carbon Nano Tube or an array of Carbon Nano Tubes as the channel material instead of Silicon. A Single-Wall Carbon Nano Tube (SWCNT) is formed by rolling a single sheet of Graphene. A CNTFET is a three-terminal device consisting of a semiconducting Nano Tube bringing two contacts (source, drain) together, and acting as a carrier channel, that is turned on or off via the third contact (gate).

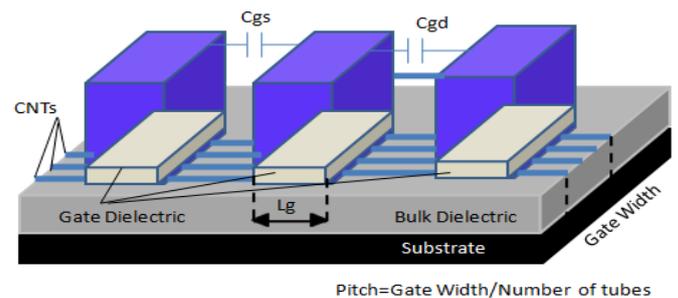


Fig 1: Physical Properties of a CNTFET

The electrical properties of Nano Tubes, deeply depends on its structure. CNTFET can be either metallic or semiconducting, depending on the chirality vector (m , n), i.e. the direction in which the Graphene sheet is rolled. The diameter of the CNT is related to the chirality vector as shown in equation (1)

$$D_{CNT} = (a/\pi) * (m^2 + n^2 + mn)^{\frac{1}{2}} \text{ ----- (1)}$$

Where $a=2.9\text{\AA}$. Also, semi-conducting Nano Tubes are direct band-gap semi-conducting with band-gap $E_g \approx 0.9/d$

(eV). Based on their operation, there are two types of CNTFET. The first type is Schottky Barrier CNTFET where the source and drain junctions are metallic and transportation of electrons occurs through tunneling .The barrier width is modulated by the application of gate voltage and thus the transconductance of the device is dependent on the gate voltage .The second type is a Ballistic CNTFET, where in the channel is intrinsic, source and drain are doped. An electrostatic potential barrier prevents flow of electrons through the channel. With the help of a positive gate voltage the barrier is passed down to allow conduction in the channel. Low-field transport is ballistic with mobility as high as 100Sqm per second.

2. EFFECTS OF RADIATIONS ON MOSFETS AND CNTFETS

Single Event transients (SETs) and Single Event Upsets (SEU) are caused when energetic particles (Alpha, Protons, Heavy Ions, etc) strike active regions of transistors and are of growing concern for digital circuits working in radiation environments. Technology scaling has resulted in greater sensitivity in both design domains to these energetic particle strikes, as depicted in Fig. 2.1a [5]-[7]. When radiation strikes a combinational logic circuit, transients are observed. This event is called Single Event Transient (SET). For this study a valid SET is the change in affected node voltage by at least $V_{dd}/2$ due particle strike. The width of the transient pulse at the node is the time during which the voltage change is greater than $V_{dd}/2$ [8]. The propagation delay is defined as t_{pLH} for an output transition from logical “0” (low) to a logical “1” (high), while t_{pHL} refers to a high to low output transition. The propagation delay is measured between the 50% transition points of the input and output waveforms [9] [10].

Figure 2.1b illustrates the effects of SETs. A transient generated at node Q_1 is propagated along the datapath, which could only be latched in the latching window, during the transition period of the clock as shown in Fig 2.1c. However, an incorrect value could be latched if the transient occurs in the latching window as shown in Fig 2.1d. The relentless desire to extract high performance with each generation of technology scaling the operating frequency of the clock is increased. This in turn widens the window of vulnerability and increases the probability of storing incorrect logic levels for designs susceptible to SETs. Any effort made to minimize the affect either by increasing the clock period or by redundancy could result at the cost of penalizing the performance and power metrics. Hence, the analysis of circuits in harsh environments is of utmost importance.

When radiation strikes the sensitive nodes of a latch or a flip flop, it can lead to an upset of 0 to 1 or 1 to 0. This event is referred to as Single Event Upset (SEU) [11] in a latch circuit. For example, if a latch is storing logic ‘1’, the NMOS corresponding to the latch is susceptible to SEU, because the body voltage is 0 Volt and drain is at logic ‘1’. When the drain voltage of a PMOS is at V_{dd} volts and

NMOS is at 0 Volt, the devices are not susceptible to SEU because the charge deposited does not observe potential difference to travel and cannot cause current flow, it may get recombined in the substrate [12].

Several SEU and SET mitigation techniques have been proposed over the last two decades in order to avoid faults in CMOS digital Circuits. Few of the popular techniques are time redundancy, self-checker techniques, reconfiguration, gate cloning and gate resizing. However, no study so far has evaluated the operability of SEUs in latches and SETs in logic circuits based on CNTFETs. This paper extends the work done on MOSFET circuits to the CNTFETs by using C-elements in latches to avoid the propagation of radiation effects.

Radiation hardness in this paper is captured as Q_{crit} , charge essential to flip a bit and was simulated through insertion of a current source at the sensitive node. For the Q_{crit} analysis, a double exponential current source with rising curve corresponding to the funneling charge collection and slowly decaying curve for the diffusion charge collection was adopted. A rising time constant of 10ps (τ_α) for charge collection and a falling time constant of 500ps (τ_β) for the ion track establishment, was chosen. The time constant values are dependent on the process technology of devices [13]. The equation below is a double exponential current source given by

$$I_p(t) = I_0 \left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}} \right) \quad \text{----- (2)}$$

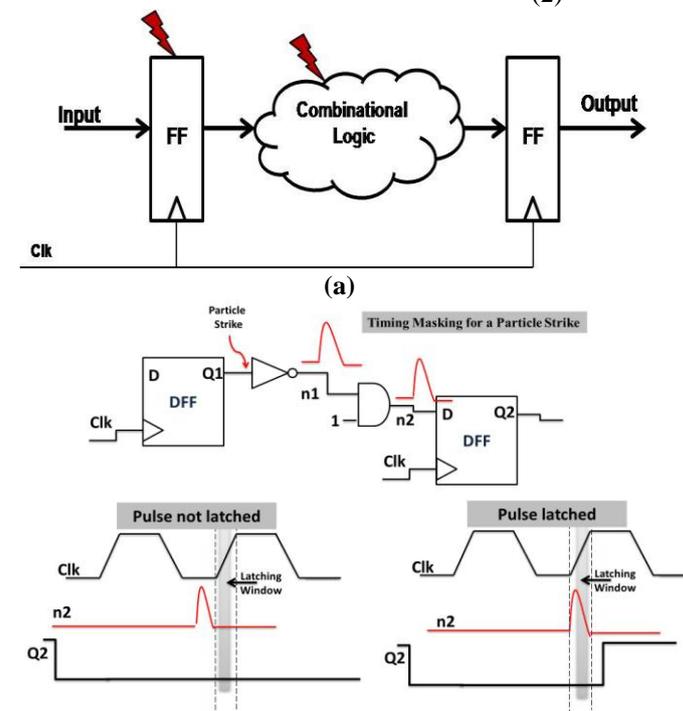


Fig.-2: (a) Fig 2.1 Radiation Strike on a Sequential Circuit (b) Transient propagation in a Datapath (c) Time masking of the transient pulse (d) Transient Pulse results in incorrect value stored at latch

The Q_{crit} was measured by changing the magnitude of the current spike while τ_{α} and τ_{β} were held constant for the above current source setup [14].

3. DESIGN IMPLEMENTATION USING CNTFETS

A. IMPLEMENTATION OF LOGIC GATES

The basic logic circuit that was tested for functionality using CNTFETs was the inverter using Stanford model. Refer Table 1 for properties. The inverter's power and performance analysis was done by varying m, n, pitch and number of tubes. The analysis showed that the properties defined in the Stanford model gave best results with optimum power consumption and delay. With these standard properties NAND and NOR gates were implemented. A comparative analysis was made between logic gates implemented using MOSFETs and CNTFETs for various levels of Q_{crit} .

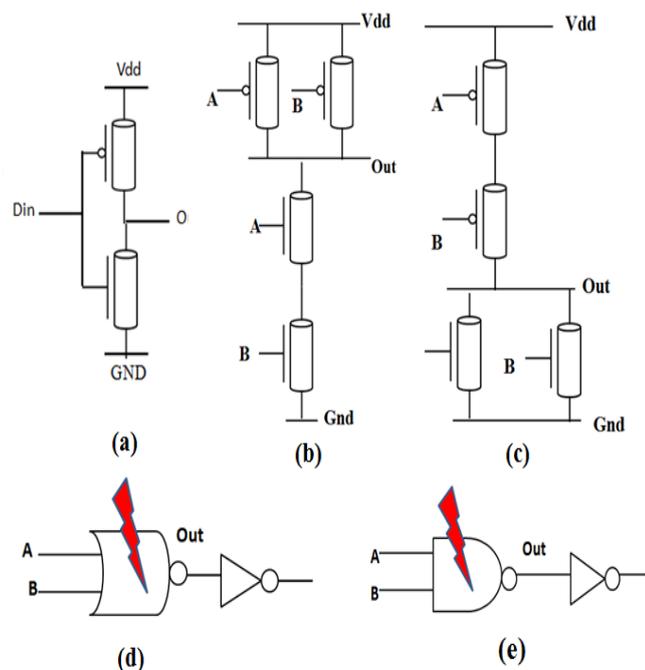


Fig 3.1: (a) Inverter using CNTFETs. (b), (c) Implementation of NAND and NOR using CNTFETs. (d), (e) Depiction of strike on NAND and NOR gates

B. IMPLEMENTATION OF INTERCONNECT

Interconnect crossbar is used to route data between the logic processing elements within a typical FPGA architecture. Applications of FPGAs are more relevant for critical operations like Space electronics which take advantage of their reconfigurability and datapath parallelism. Hence, robust operation of the pass transistors is highly critical to ensure correct operation and extract high performance.

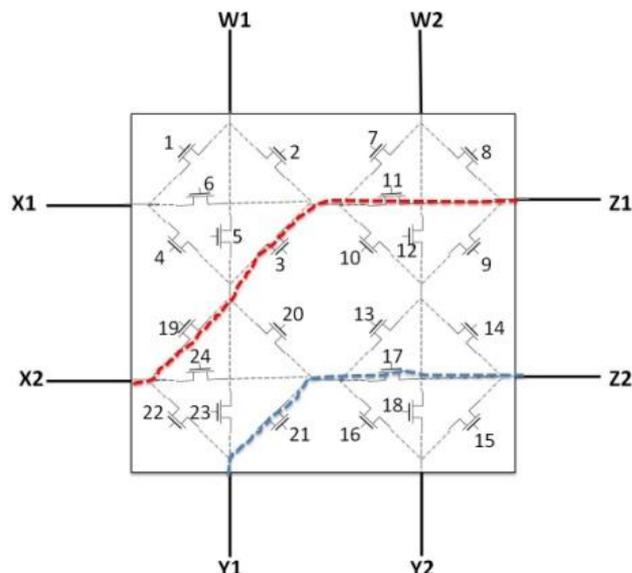


Fig 3.2: Programmable Interconnect Crossbar

Figure 3.2 illustrates a simple interconnection crossbar comprising of pass transistors (NFETs), where in the routing path is selected by programming the configuration cells connected to the gate terminal of the pass transistors. In the implementation shown the crossbar connects X2 to Z1 and Y1 to Z2. A similar setup for CNTFETs was implemented and a comparison for power, performance and radiation robustness was evaluated.

C. IMPLEMENTATION OF LATCHES

Latch_n1 in figure 3.3 is a simple Clocked CMOS latch based on CNTFETs. This latch is susceptible to SEU and vulnerable to the transient pulse induced due to radiation. The model discussed in this paper as shown in Fig 3.4 overcomes the drawbacks of the above latch.

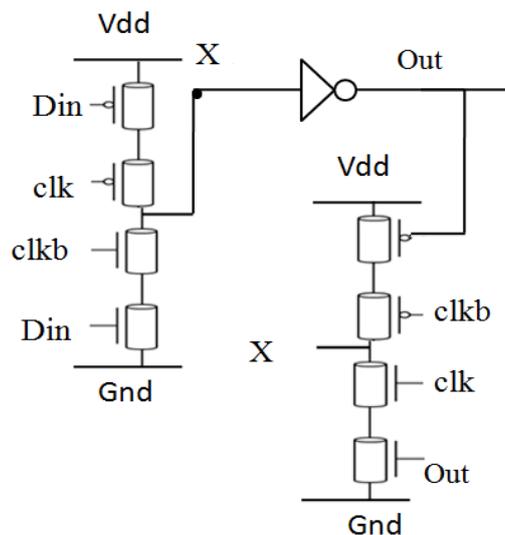


Fig 3.3: Latch_n1 - Simple Latch

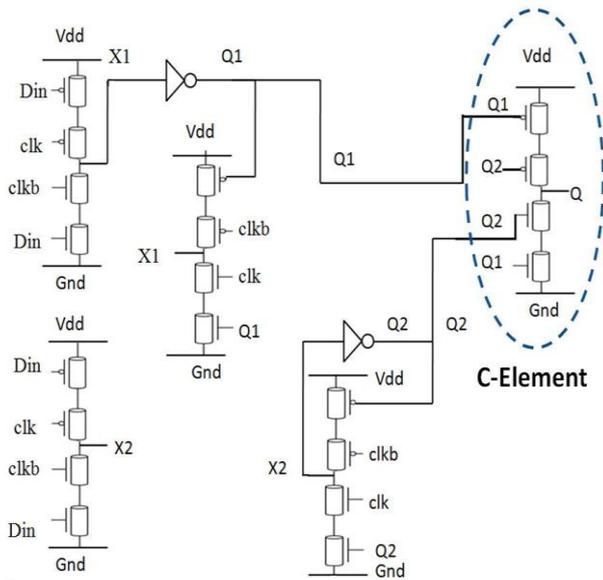


Fig 3.4: Latch_n2 (Proposed Latch with a C-element)

Latch_n2, as shown in Fig 3.4 is a Dual Modular Redundant, SEU tolerant latch which uses C-element. The design comprises of two latches. Each latch in turn is designed in a way that redundant data is stored at two different nodes and provides a recovery path after an SEU. If the internal node Q₁ is injected with external charge such that the logic state of the node is flipped, the redundant node Q₂ will hold the logic state and prevent the a logic state flip in the latch

4. SIMULATION RESULTS

Simulations for robust SEU tolerant latches and SET tolerant logic gates based on CNTFETs and MOSFETs have been carried out and the setup is shown in the table below.

Table -1: Simulation Setup

SIMULATION SETUP		
FETS	CNTFETs	MOSFETs
Device Technology	32 nm Stanford CNTFET Model	45nm IBM FDSOI MOSFET
Device Metrics	(m,n)=(19,0), Pitch=20nm, Dia=1.426nm Number of tubes=5	Width=1u(for logic gate design) Width=0.5u(Latch Design)
Simulator	Synopsys - HSPICE	
Radiation Analysis	Critical Charge (Q _{crit}) - Measured by using an approximate model of double exponential equation current source	

A. PERFORMANCE OF CNTFETS FOR VARYING PROPERTIES OF CNTS

Device parameter, number of tubes between source and drain of the CNTFET, defined here as CNTTUB was varied from 1 to 9, the energy and delay metrics were inferred and as depicted in Fig 4.1 an inverse relationship between energy and delay was seen. When the number of tubes was increased, delay decreased but energy increased and vice-versa.

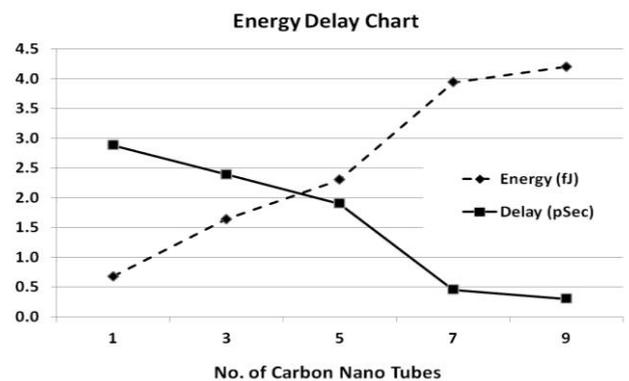


Fig. 4.1: – Energy Delay Chart for varying CNTs

B. SETs IN LOGIC CIRCUITS

As Q_{crit} (external charge deposited) increases, the transient width of the pulse at the node struck in the MOSFET circuit raises up to 76ns. But for the CNTFET circuits as the Q_{crit} is raised gradual change in the transient widths observed as shown in Fig. 4.2. Thus, it signifies that CNTFET’s exhibit far better resilience in radiation environments than MOSFETs.

Table 2- Critical Width Transient Response for Logic Gates

Q _{crit} (fC)	CNTFETs		45nm IBM SOI MOSFET	
	A (nSec)	B (nSec)	C (nSec)	D (nSec)
12.5	0	28.45	0	0
25	26.8	40.71	0	37.98
37.5	34.98	43.91	45.11	65.81
50	39.18	45.13	65.67	70.47
62.5	41.73	47.04	72.85	73.52
75	42.98	48.08	76.57	76.9

From table 2 at low strike rates, MOSFET devices show no effect due to radiation because of the Fully Depleted SOI devices, which consists of an SiO₂ layer between the substrate and active region. This region helps prevent the accumulation of charge making it resilient to radiation at lower charge deposition values. When the NAND and NOR gates of the two device technology were compared, the performance of NAND gates are observed to be much better

than NOR gates when radiation strike occurs. This is because the NAND gate has two PMOS (PCNTFETs) connected in parallel which give better drive strength to overcome the transients.

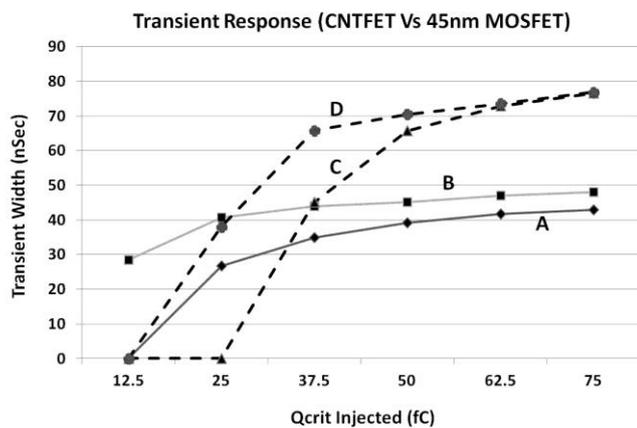


Fig. 4.2: Comparison plot of transient response of NAND and NOR

C. SEUs IN LATCHES

Latch_n1 and Latch_n2 were implemented using both MOSFETs and CNTFETs. CNTTUB used for this simulation was 10. The energy and delay values for both the latches based on MOSFETS showed almost 100-fold increase when compared to CNTFETs. In spite of an increase in area due to C-element in CNTFET latches, the difference in energy observed was only 1.4 fJ.

Table 3- Latches implemented using CNTFETs

Design	Energy(fJ)	Delay(pS)	Qcrit(fC)
Latch_n1	3.43	1.34	22.00
Latch_n2	4.82	7.28	Nil

Table 4 Latches implemented using MOSFETs

Design	Energy(fJ)	Delay(pS)	Qcrit(fC)
Latch_n1	358	331.00	20.00
Latch_n2	390	629.00	Nil

The Q_{crit} at which the logic state is flipped in latch_n1 is higher in CNTFET latches than MOSFET latches. The modified latch which uses C-element in the MOSFET design consumes high energy and produces large delay. Though the MOSFET design is SEU robust, the low energy consumption values and very low delay values, makes CNTET latch a stupendous, robust SEU tolerant design.

The simulation results indicates that a radiation strike at node Q_1 (Sudden Voltage Drop) gives a hassle free output from the latch_n2 (Q) because a redundant node (Q_2) holds the logic value (D_{in}).

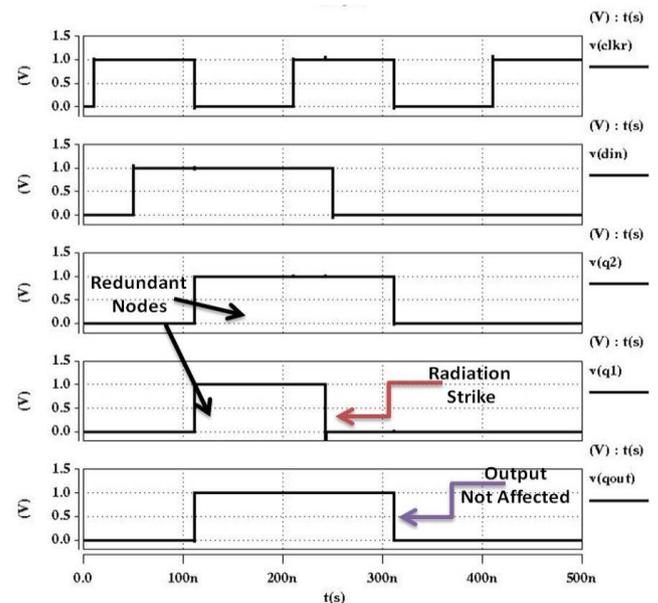


Fig. 4.3: Redundant Latch with C-Element

D. SETs IN INTERCONNECT CROSSBAR

A 45nm IBM FDSOI MOSFET based interconnect was injected with 50fC of charge. This $4\mu m$ (the width of each MOSFET being $1\mu m$) width interconnect crossbar consumed 19fJ of energy and a transient width of 180 pS was observed. A similar design was implemented using CNTFETs as shown in the figure below and was analyzed for energy and critical width of transient for varying number of CNTs.

When CNTTUB was varied from 5 to 51, the maximum energy consumed by the interconnect was 4.03fJ which is almost five times lower in comparison to the energy consumed by a MOSFET based interconnect. By increasing the number of CNTs, the width of the transient decreased gradually due to high drive strength of the CNTFET pass transistors. With 50fC of Q_{crit} , a 180pSec transient width is observed in MOSFET interconnect as well as CNTFET interconnect (CNTTUB=41). From this point, for further increase in CNTTUB, the width is reduced. Hence it is more feasible to use CNTFETs based interconnect not only because of increased resilience to radiation strikes but also due to five-fold lower energy consumption. The total width (Pitch, CNTTUB, Diameter) is 25% lower than a MOSFET interconnect.

When the pass transistors are on, the input is seen at the output. A radiation strike at node 2 induces a transient with amplitude 2V. This transient gradually shortens as it is transferred via the pass transistors (Observe the height of the transient at node 3 and node x). This depicts high drive strength of the CNTFETs to overcome the transients in the interconnect crossbar.

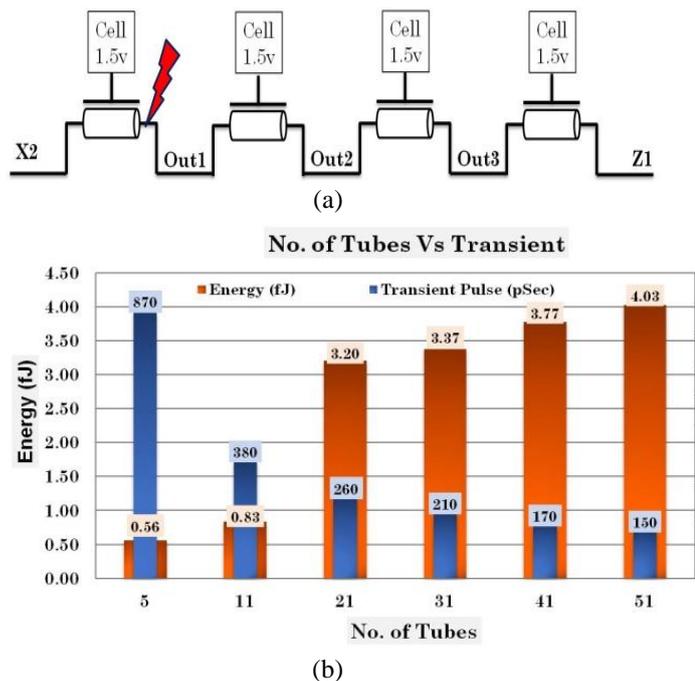


Fig 4.4: (a) Interconnect from X₂ to Z₁ using MOSFETs and CNTFETs. (b) Number of tubes Vs Transient width and Energy

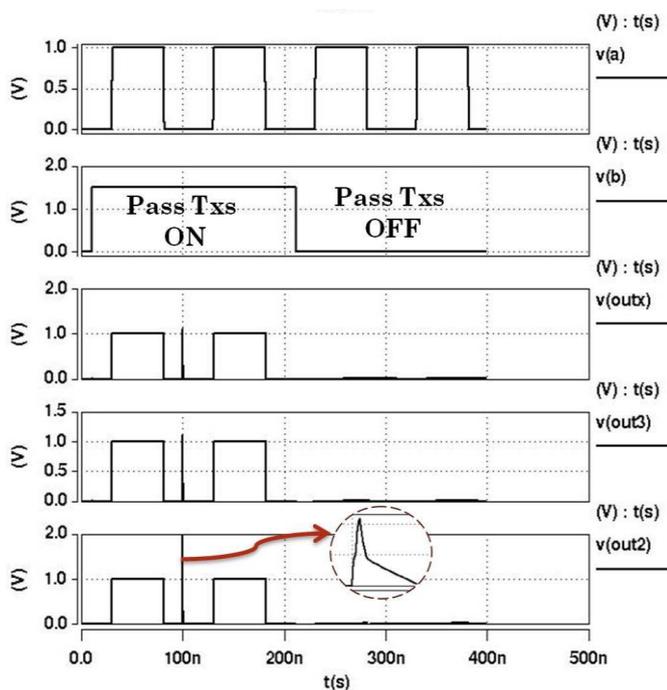


Fig 4.5: Signals at nodes of interconnect crossbar

5. CONCLUSION

SET analysis in logic gates was performed and the simulation results showed the critical width of the transients for CNTFET based logic gates is on an average 45% lower than that of MOSFET devices. Further, the modified latch with C-element based on CNTFETs not only preserved the

stored logic levels but also consumed less energy, 4.82 fJ as compared to 390 fJ of the MOSFET latches. CNTFETs Latches provide improved Q_{crit} values and demonstrated order by 2 reduced energy delay values. The reason can be cited as higher drive strength of CNTFET devices and their excellent ballistic properties. A CNT Interconnect Crossbar not only consumes 25% lower energy but also occupies 78% lesser area. Further the CNTFET Interconnect Crossbar with CNTTUB > 41 showed an overall comprehensive improvement including radiation robustness when compared to the MOSFET design.

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BIOGRAPHIES



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