DESIGN AND IMPLEMENTATION OF HIGH SPEED BAUGH WOOLEY AND MODIFIED BOOTH MULTIPLIER USING CADENCE RTL

Jipsa Antony[1], Jyotirmoy Pathak[2]

[1]*Student, Department of Electronics & Communication, Lovely Professional University, Punjab, India*
[2]*Assistant Professor, Department of Electronics & Communication, Lovely Professional University, Punjab, India*

Abstract

Modified Booth Multiplier is one of the different techniques for signed multiplication. It is used normally as the fastest multiplier. Baugh Wooley Multiplier is another technique for signed multiplication. It is not widely used because of its complexity of its structure. Here design and implementation of 8 bit Modified Booth multiplier and Baugh Wooley multiplier has done using conventional method as well as using High Performance Multiplier Reduction tree (HPM) technique. The comparative analysis of all the design for the delay, area foot print and energy has done using Cadence 180nm RTL complier to show that Baugh Wooley multiplier can become more faster than the Modified Booth Multiplier.

KeyWords:*Multiplier, Baugh Wooley, Modified Booth, HPM, Cadence RTL.*

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1. INTRODUCTION

Multiplication is one of the complex arithmetic operations [6]. In most of the signal processing algorithms multiplication is a root operation whereas multipliers have large area, consume considerable power and long latency. So, in low-power VLSI system design, low-power multiplier design is also an important part. Mostly architecture of parallel multipliers can be classified into three parts: *bit generation of primary partial product* by using simple AND gates or by using any recoding strategies; *bit compression of partial product* by using any irregular array of logarithmic tree or by using a regular array; and the *final addition* [6].

The main part of this paper is the reduction tree technique which is used for designing a new Baugh Wooley multiplier architecture. High Performance Multiplier (HPM) reduction tree [6], [8] is based mainly on the generated partial product compression [1]. It is completely regular and the connectivity of the adding cells in HPM is in the triangular shape. The reason for using triangular shaped is that the triangular cell placement in the reduction tree technique has a shorter wire length [8].

In the paper design and implementation of conventional 8 bit Baugh Wooley and Modified Booth multiplier algorithm has done and compared the result obtained with the new design of 8 bit Baugh Wooley and Modified Booth multiplier algorithm using HPM reduction tree [8], [6]. The comparative analysis has been done to prove that the new Baugh Wooley multiplier design is faster than the conventional Baugh Wooley and conventional as well as HPM Modified Booth multiplier design [9]. The algorithm for 5 bit Baugh Wooley multiplier is shown in Fig 1. And the algorithm for 8 bit Modified Booth multiplier is shown in Fig 2.

					$\boldsymbol{A_4}$	$\boldsymbol{A_3}$	$\boldsymbol{A_2}$	$\boldsymbol{A_1}$	$\boldsymbol{A_0}$	
					$\boldsymbol{X_4}$	$\boldsymbol{X_3}$	$\boldsymbol{X_2}$	$\boldsymbol{X_1}$	$\boldsymbol{X_0}$	
					$\overline{A_4X_0}$	A_3X_0	A_2X_0	A_1X_0	A_0X_0	
				$\overline{A_4X_1}$	A_3X_1	A_2X_1	A_1X_1	A_0X_1		
			$\overline{A_4X_2}$	A_3X_2	A_2X_2	A_1X_2	A_0X_2			
		$\overline{A_4X_3}$	A_3X_3	A_2X_3	A_1X_3	A_0X_3				
	A_4X_4	$\overline{A_3X_4}$	$\overline{A_2X_4}$	$\overline{A_1X_4}$	$\overline{A_0X_4}$					
1				1						
$\boldsymbol{P_9}$	$\boldsymbol{P_8}$	$\boldsymbol{P_7}$	$\boldsymbol{P_6}$	$\boldsymbol{P_5}$	$\boldsymbol{P_4}$	$\boldsymbol{P_3}$	$\boldsymbol{P_2}$	$\boldsymbol{P_1}$	$\boldsymbol{P_0}$	

Fig-1: Illustration of 5 bit Baugh Wooley Multiplier Algorithm.

								A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
								B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
						$\overline{PP_{80}}$	PP_{80}	PP_{70}	PP_{60}	PP_{50}	PP_{40}	PP_{30}	PP_{20}	PP_{10}	PP_{00}
				1	$\overline{PP_{81}}$	PP_{71}	PP_{61}	PP_{51}	PP_{41}	PP_{31}	PP_{21}	PP_{11}	PP_{01}		Neg_0
		1	$\overline{PP_{82}}$	PP_{72}	PP_{62}	PP_{52}	PP_{42}	PP_{32}	PP_{22}	PP_{12}	PP_{02}		Neg_1		
1	$\overline{PP_{83}}$	PP_{73}	PP_{63}	PP_{53}	PP_{43}	PP_{33}	PP_{23}	PP_{13}	PP_{03}		Neg_2				
									Neg_3						

Fig-2: Algorithm for Modified Booth Multiplier.

2. BAUGH WOOLEY MULTIPLIER

The Baugh-Wooley multiplication is one of the efficient methods to handle the sign bots. This approach has been developed in order to design regular multipliers, suited for 2's complement numbers [2]. Let two n-bit numbers, multiplier (A) and multiplicand (B), to be multiplied. A and B can be represented as

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i \quad (1)$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \quad (2)$$

Where the a_i's and b_i's are the bits in A and B, respectively, and a_{n-1} and b_{n-1} are the sign bits. The product, P = A x B, is given by the equation:

$$P = A \times B = \left(-a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i\right) \times \left(-b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i\right)$$

$$= a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2} a_i 2^i \sum_{j=0}^{n-2} b_j 2^j - 2^{n-1}\sum_{i=0}^{n-2} a_i b_{n-1}2^i - 2^{n-1}\sum_{j=0}^{n-2} a_{n-1}b_j 2^j \quad (3)$$

The final product can be generated by subtracting the last two positive terms from the first two terms [2].

Instead of doing subtraction operation, it is possible to obtain the 2's complement of the last two terms and add all terms to get the final product.

The last two terms are n-1 bits in which each that extend in binary weight from position 2^{n-1} up to 2^{2n-3}. On the other hand, the final product is 2n bits and extends in binary weight from 2^0 up to 2^{2n-1}.

At first pad each of the last two terms in the product P equation with zeros to obtain a 2n-bit number to be able to add it with the other terms. Then the padded terms extend in binary weight from 2^0 up to 2^{2n-1} [3].

Let X is one of the last two terms that can represent it with zero padding as

$$X = -0 \times 2^{2n-1} + 0 \times 2^{2n-2} + 2^{n-1}\sum_{i=0}^{n-2} x_i 2^i + \sum_{j=0}^{n-2} \times 2^j \quad (4)$$

The final product [3], P = A x B becomes:

$$P = A \times B = a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2} a_i 2^i \sum_{j=0}^{n-2} b_j 2^j + 2^{n-1}\sum_{i=0}^{n-2} \overline{a_i b_{n-1}}2^i + 2^{n-1}\sum_{j=0}^{n-2} \overline{a_{n-1}b_j}2^j - 2^{2n-1} + 2^n \quad (5)$$

Let A and B are 4-bit binary numbers, then the product [3], P = A x B will be 8 bit long and is

$$P = a_3 b_3 2^6 + \sum_{i=0}^{2} a_i 2^i \sum_{j=0}^{2} b_j 2^j$$

$$+ 2^3 \sum_{i=0}^{2} \overline{a_i b_3} 2^i + 2^3 \sum_{j=0}^{2} \overline{a_3 b_j} 2^j$$

$$-2^7 + 2^4 \qquad (6)$$

The block diagram for 4 bit Baugh Wooley multiplier is shown in Fig 3 and the detailed structure of each block has been shown in Fig 4.

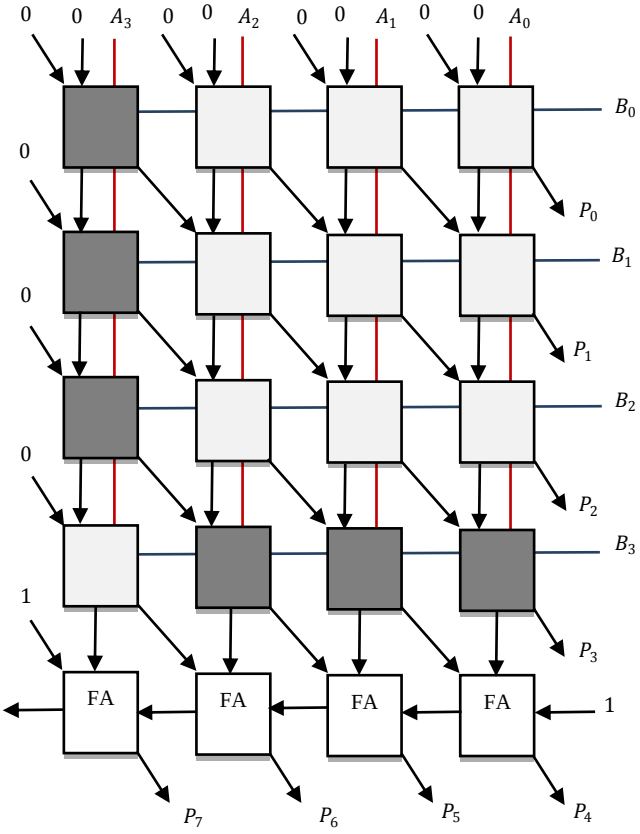

Fig-3: Block diagram of 4 bit Baugh Wooley Multiplier.

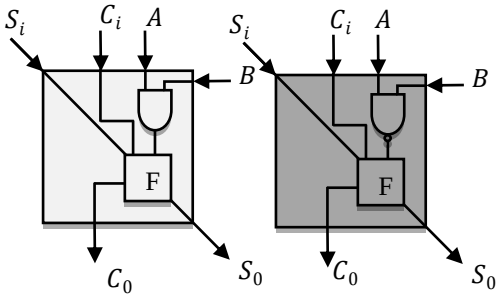

Fig-4: Detailed view of white cell and grey cell of the Baugh Wooley multiplier.

3. MODIFIED BOOTH MULTIPLIER

Let A be the multiplicand and B be the multiplier for multiplication of two n-bit integer numbers which can be represented in two's complement as.,

$$A = -a_{n-1} 2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i \ (7)$$

$$B = -b_{n-1} 2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \ (8)$$

In Modified Booth multiplier, B in (2) becomes.

$$B = \sum_{i=0}^{\frac{n}{2}-1} m_i 2^{2i}$$

$$= \sum_{i=0}^{\frac{n}{2}-1} (-2b_{2i+1} + b_{2i} + b_{2i-1}) 2^{2i} \ (9)$$

Where $b_{-1} = 0$, and $m_i \in \{-2, -1, 0, 1, 2\}$. from the encoding results of B, The booth multipliers chooses the action -2A, -A, 0, A, or 2A to generate the partial product rows shown in Table 1.

Table -1: Truth Table for the E-Cell Of The Encoder

$Y_{i+1}\ Y_i\ Y_{i-1}$	Action	$S_0\ S_1\ S_2\ S_3$
0 0 0	+0	0 1 0 1
0 0 1	+X	1 1 0 1
0 1 0	+X	1 1 0 1
0 1 1	+2X	0 1 1 1
1 0 0	-2X	0 1 0 0
1 0 1	-X	0 0 0 1
1 1 0	-X	0 0 0 1
1 1 1	+0	0 1 0 1

The system of action [8] is partitioned into blocks such as

- the encoder unit that is the e-cell that encodes multiplier bits (Y bits) and then it send signals for the generation of partial products;
- the partial product generator (PPG) which will decodes signals from the encoder as well as the multiplicand X in order to generate the partial products;
- the carry-save adder matrix (CAM) will add all the partial product which obtained during previous operation, and

- The last row of full adders and half adder that is the final product adder (FPA) will add all the value from the CAM and produce the final product [10].

Fig 5 shows the architecture for Modified Booth multiplier [11]. The encoder (e-cell in Fig 6) where the multiplier(Y) encodes and the encoded signal and the multiplicand(X) is given to the partial product generator (g-cell in Fig 7) are the basic units of the Modified Booth multiplier. Both CAM and FPA blocks are made up of full adders as well as half adders [11].

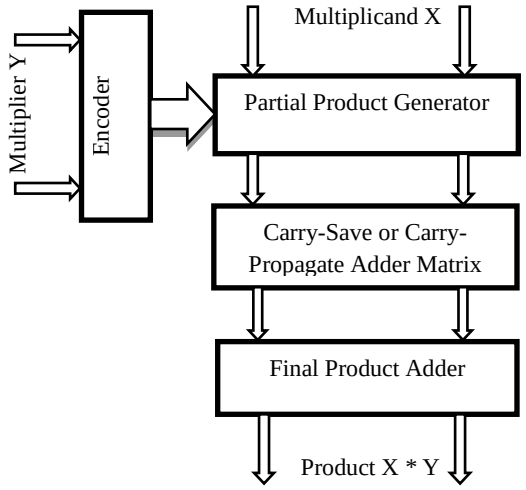

Fig-5: Architecture of Modified Booth Multiplier [6].

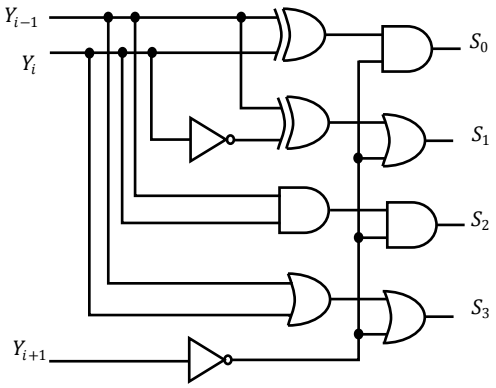

Fig-6: Encoder (E-Cell) of Modified Booth Multiplier.

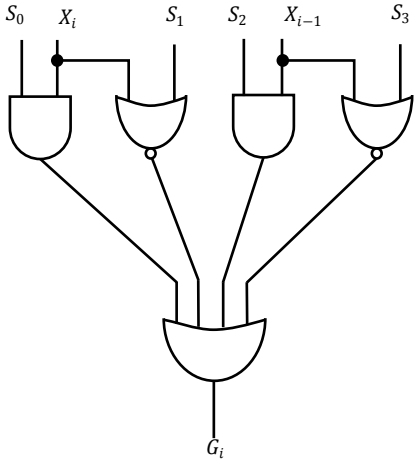

Fig-7: Decoder (G-Cell) partial product generator of Modified Booth multiplier.

4. HIGH PERFORMANCE MULTIPLIER REDUCTION TREE

In High Performance reduction tree technique the primary partial product bits are generated outside the tree. After the generation of partial product bits; these partial products then put into the reduction tree to calculate the product of the multiplier. This can be done using number of half adders and full adders arranged in a tree structure. The routing patterns for half adder, full adder and wiring cells in HPM reduction tree can be shown in Fig 5.

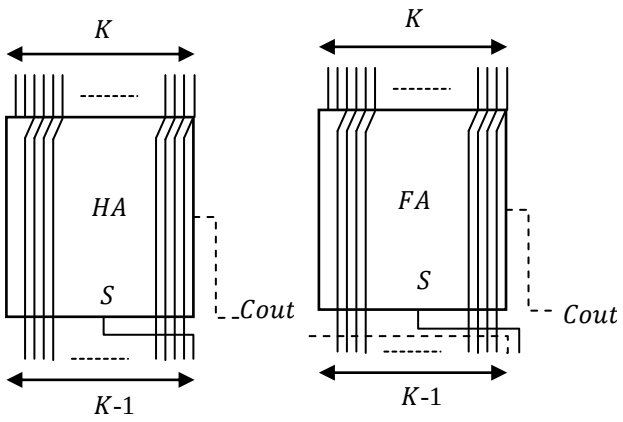

Fig-8: HPM Half Adder and Full Adder Cell.

A K number of partial product bits are enter at the top of the half adder and full adder cell. The main role of the half adder and full adder cell is to reduce this number by one and to produce an output carry that is passed rightwards to the next column.

4.1 HPM Baugh Wooley Multiplier

The illustration of Baugh Wooley algorithm is represented in Fig 1. It is based on Hatamian's scheme [4]. It can be divided into three steps: 1) the most significant bit (MSB) of the partial-products in each N-1 rows and all bits of the last partial-product row, except its MSB, are inverted in the Baugh Wooley algorithm. 2) To the N^{th} column a '1' is added. 3) In the final result the MSB of it is inverted [6].

Implementation of Baugh Wooley multiplier using HPM method [6] is simply a straight forward method which is as represented in the algorithm. The partial products can be calculated using AND gates and the inverted products can be calculated using NAND gates. Insertion of '1' and the partial products are shown in Fig 9 that the block diagram for 8 bit Baugh Wooley multiplier using HPM [5].

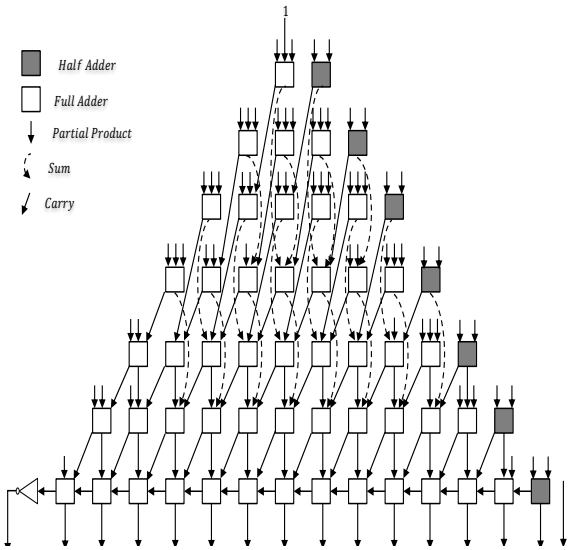

Fig-9: Block diagram for 8 bit HPM Baugh Wooley Multiplier [6].

4.2 HPM Modified Booth Multiplier

The illustration of Modified Booth algorithm is represented in Fig 1. Implementation of Modified Booth multiplier using HPM method [6], [8] is simply a straight forward method which is as represented in the algorithm. The partial products can be calculated using encoder and decoder which are shown in Fig 3 and Fig 4. Insertion of '1' and the partial products are shown in Fig 5 that the block diagrams for 8 bit Modified Booth multiplier using HPM [5].

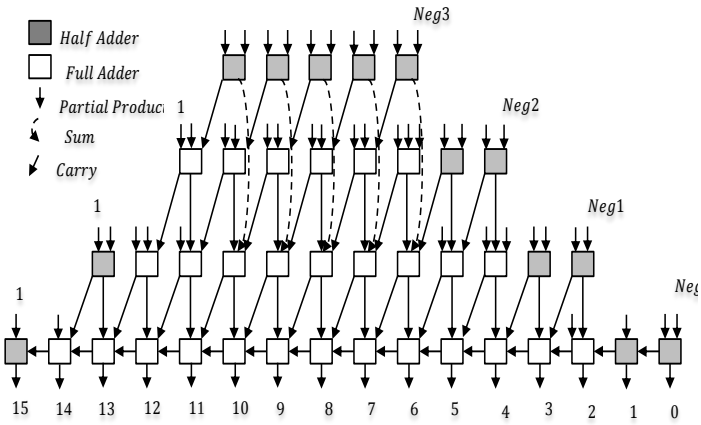

Fig-10: Block diagram for 8 bit HPM Modified Booth Multiplier [7], [8].

5. SIMULATION RESULTS

5.1 Simulation Results of 8 bit Conventional Baugh Wooley Multiplier Using Cadence RTL complier 180nm process technology.

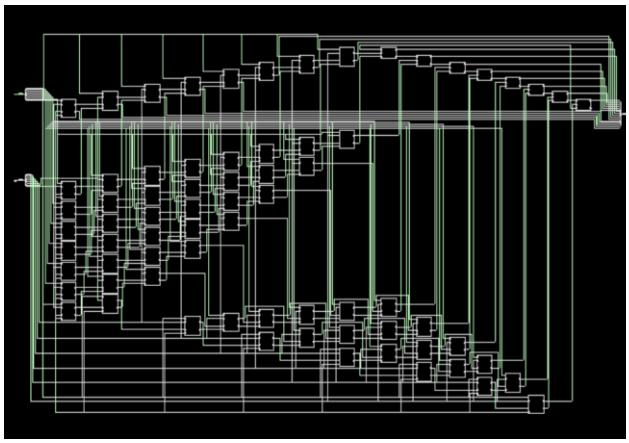

Fig-11: RTL View of 8 bit conventional Baugh Wooley Multiplier.

Fig-12: Worst Case path of 8 bit conventional Baugh Wooley Multiplier.

5.2 Simulation Results of 8 bit HPM Baugh Wooley Multiplier Using Cadence RTL complier 180nm process technology.

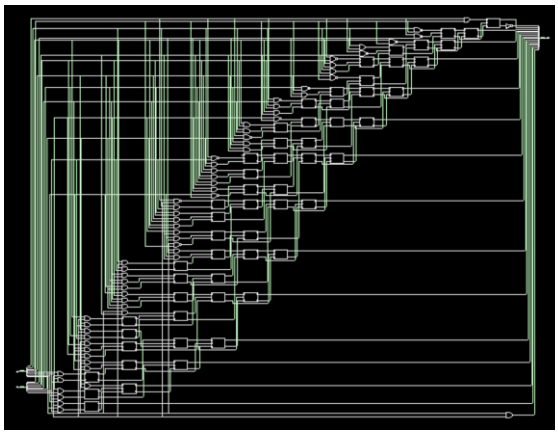

Fig-13: RTL View of 8 bit HPM Baugh Wooley Multiplier.

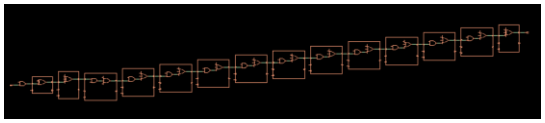

Fig-14: Worst case path of 8 bit HPM Baugh Wooley Multiplier.

5.3 Simulation Results of 8 bit Conventional Modified Booth Multiplier Using Cadence RTL complier 180nm process technology.

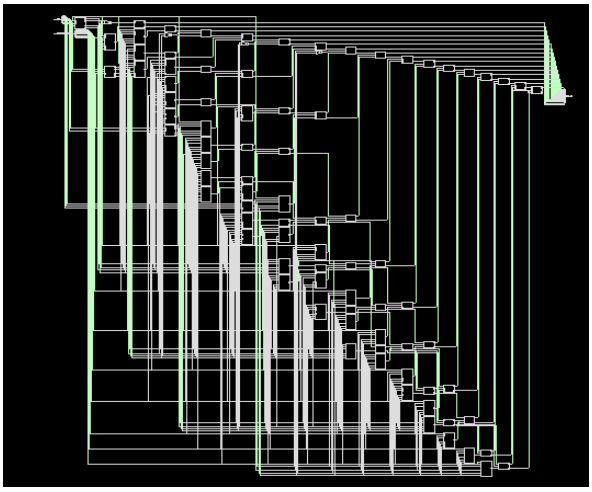

Fig-15: RTL View of 8 bit conventional Modified Booth Multiplier.

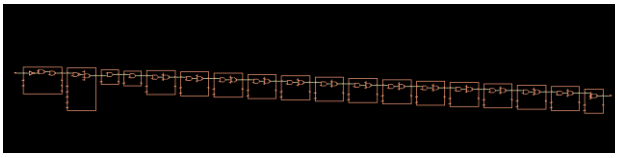

Fig-16: Worst Case path of 8 bit conventional Modified Booth Multiplier.

5.4 Simulation Results of 8 bit HPM Modified Booth Multiplier Using Cadence RTL complier 180nm process technology.

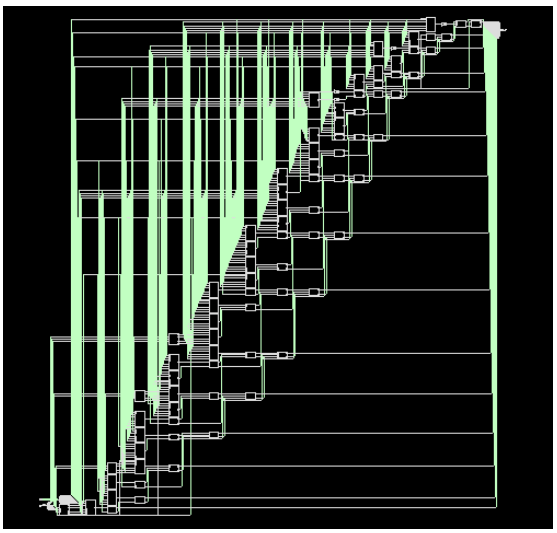

Fig-17: RTL View of 8 bit HPM Modified Booth Multiplier.

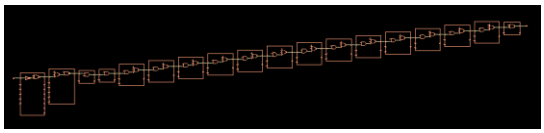

Fig-18: Worst case path of 8 bit HPM Modified Booth Multiplier.

6. COMPARATIVE ANALYSIS

Conventional Baugh Wooley and Modified Booth versus HPM Baugh Wooley and Modified Booth multiplier in terms of the number of power, delay, area footprint and energy. It is shown in Table 2.

Table-2: Observations of Conventional Baugh Wooley and Modified Booth multiplier and HPM Baugh Wooley and Modified Booth multiplier

	HPM Modified Booth	Conventional Modified Booth	HPM Baugh Wooley	Conventional Baugh Wooley
Leakage Power (nw)	1064.86	1090.12	1073.68	1659.01
Net Power (nw)	33455.11	31546.12	27503.72	33713.09
Internal Power (nw)	38571.2	34711.81	37283.85	34400.05
Switching (nw)	72026.31	66257.93	64787.57	68113.13
Data path Area	2474.65	2823.02	2237.39	3411.65
Number of Cells	374	406	324	568
Delay (ps)	1971.6	2102.3	1744.9	2394.9
Energy (fJ)	65.96009488	66.31940808	47.99124103	80.73947924

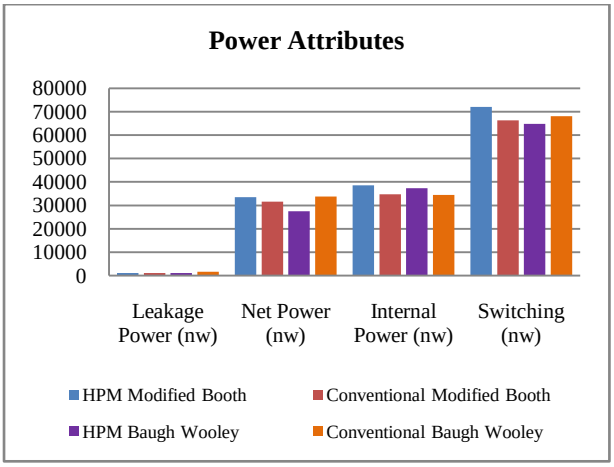

Chart-1: Chart representing comparison of power attributes.

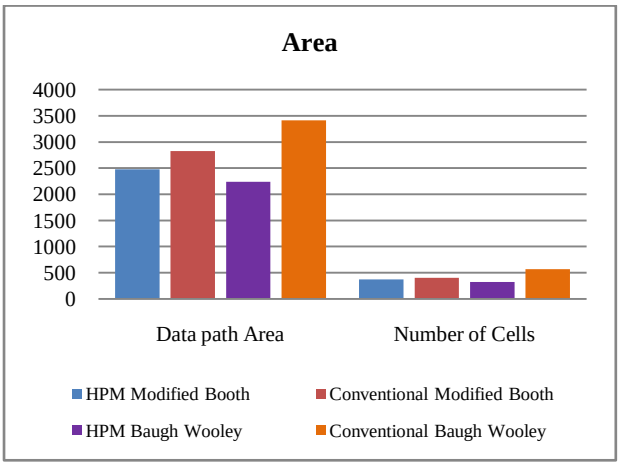

Chart-2: Chart representing comparison of data path area and number of cells.

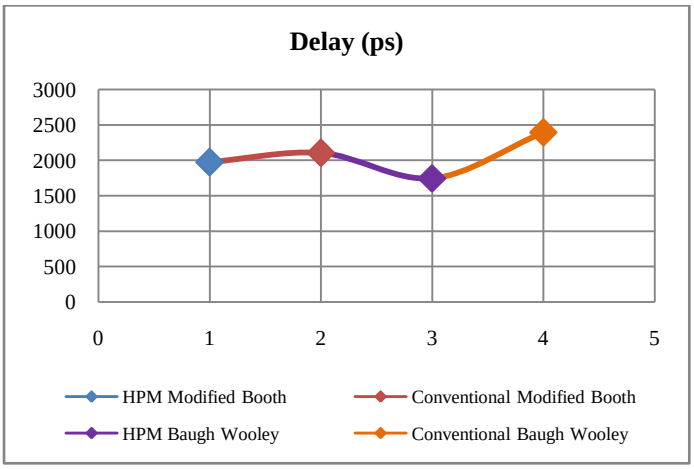

Chart-3: Chart representing comparison of delay.

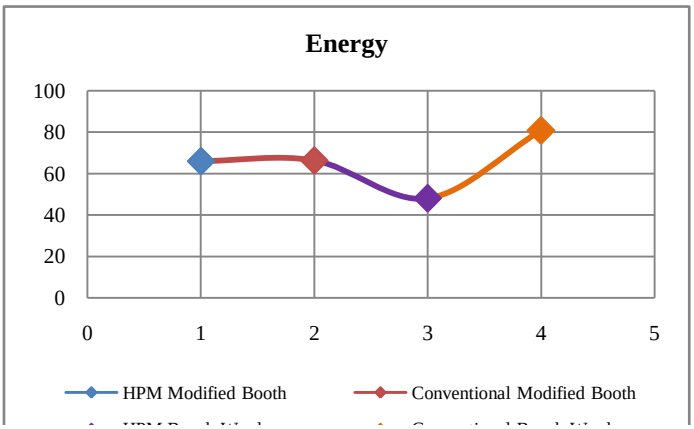

Chart-4: Chart representing comparison of energy.

By comparing Modified Booth and Baugh Wooley multiplier using conventional method and HPM Reduction tree method. It gives the good idea that it is possible to make the Baugh Wooley multiplier faster than the Modified Booth multiplier using High Performance Reduction tree technique with low power, less delay and small area.

7. CONCLUSIONS

Analysis of Modified Booth and Baugh Wooley multiplier using conventional method as well as using HPM reduction tree method has done in Cadence RTL compiler. From the analysis it is clear that HPM Baugh Wooley multiplier is better than Conventional Baugh Wooley multiplier. Like HPM Modified Booth multiplier is better than the Conventional Modified Booth multiplier. Finally the comparative analysis of both the HPM multiplier shows that HPM Baugh Wooley multiplier gives better performance than the HPM Modified Booth multiplier. So from the result the new design of HPM Baugh Wooley multiplier is the fastest multiplier than the HPM as well as Conventional Modified Booth multiplier. In future if it is possible to reduce the internal power again the HPM Baugh Wooley multiplier will become the best.

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BIOGRAPHIES

Jipsa Antony, born in Kerala, India in 1988. She secured B.Tech degree in Electronics &Communication Engineering from College of Engineering, Thalassery (affiliated to Cochin University of Science and Technology) and is pursuing M.Tech in Electronics & Communication Engineering in Lovely Professional University, Punjab. She worked as software engineer in GEOtrans Technologies Pvt Ltd, Trivandrum from 1st Dec 2010 to 13th Jan 2012. Her research interests are in VLSI DSP, VLSI high speed architecture design.

JyotirmoyPathak, born in India in 1986. He has completed his BE in ECE in 2008 and ME in VLSI Design in 2011 from Anna University. He worked as project assistant in CEERI CSIR Chennai from 15thJuly 2008 to16thOct 2009. Now he is working as an Assistant Professor in Lovely Professional University, Punjab from 25th July 2011 onwards. His research interests are in VLSI Signal Processing, VLSI high speed architecture design.