I-SLIP ALGORITHM FOR LOW LATENCY ON HYBRID NOC ARCHITECTURE

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Abstract

With today ASIC technology, a large number of memory can be easily implemented in a single chip. As the fabrication technology continuous to improve smaller feature size, which makes allows increasingly more integration of system onto the single dies. without having the any correct scheduling algorithm, communication between the components can becomes the limiting factor for performance. In this Paper ,we use i-slip scheduling algorithm with mesh router for NOC architecture .The advantages of the algorithm is achieving almost 100% throughput as the result low latency can be provided by desynchronization of the output arbiters . For the reduction of the latency of the latency of the hybrid NOC architecture efficient partition and mapping algorithm is proposed. When compared with the other architecture improvement of 17.6% in latency is been studied.

Keywords— *Hybrid NOC architecture, i-slip algorithm, mesh router, throughput, I P cores, mesh architecture.*

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1. INTRODUCTION

In the evolution of the technology for the embedded system the complexity becomes one of the most constraining aspects . Cost and time issues may also consider as the difficulties on the network on chip (NOC) . Many IP's such as a processor ,core memories and peripheral are placed on the single dies. Semiconductor technology has been advanced very fastly and rapid increased in the technology . Semiconductor technology consist of the IP cores that is functional intellectual property and it is placed on the single chip. If the ip core is increased the communication performance is also been decreased. Network on chip (NOC) system map ips on the block and transmit the data between the ip's using the network communication.

In this paper, we proposed a communication of the data with low latency using bus mesh hybrid architecture for system on chip (SOC). IP are been used which decides the location each of them. Here the communication feature of the IP been extracted. In the proposed hybrid architecture, IP with higher communication affinity are placed in same subsystem, which reduce the hot spot and reduce transmission latency.

Router connects the system and also connects the neighboring routers, also connects the single IP or a bus based subsystem. Reduction in design cost and power consumption with IP's without interphase for each IP.

In the semiconductor technology there is increase in fabrication which improves in small size and allow to integrate component on single dies. If the proper attention is not given high performance interconnect the communication between the components become limited factor. This project implements an on-chip SOC interconnect embodying I-SLIP scheduling algorithm for efficient communication between SOC devices. It provides fast communication and full N-to-N routing capabilities. But efficiently we will focus on the i-slip scheduling algorithm, which will help in reduction in the low latency on chip communication.

The design challenges are discussed in section II, followed by proposed work in section III, and the related work is visited in section IV followed by the conclusion in section V.

2. DESIGN CHALLENGES

In the system, here the hybrid architecture is used ,and the hybrid architecture is explain. The hybrid system consist of several bus based subsystem and its based on NOC architecture. IP's with heavy traffic are placed in same subsystem. The fig shows hybrid NOC architecture. Here R denotes the router, S denotes the sub system, C denotes the single IP core, B denotes the bridge of NOC and bus. These are the important components. Every subsystem consist of certain architecture NOC and bus architecture is interphase by the bridge. If data is transfer from subsystem to network, bridge serve as a slave component of bus which is use to receive control signal. Bridge help to packetize them into packet and deliver the packet to router. When data transfer from network to subsystem bridge serve as a master component and depacketize the packet, then serve all the data to corresponding IP's.

The i-slip algorithm is explained in the section. The i-slip uses extra state to store one pointer to each input port and output port. The scheduling in i-slip is done in round robin and derandomization is achieved in round robin fashion using the concept of except and grand pointer. The iteration consist of three phases. The Request, grand and accept. The output port is maintain a grant pointer G and the input port maintain an accept pointer A. The multiple packets from

input to output port, this pointers are resolved and vice versa. Section A will explain the three phase of i-slip algorithm.

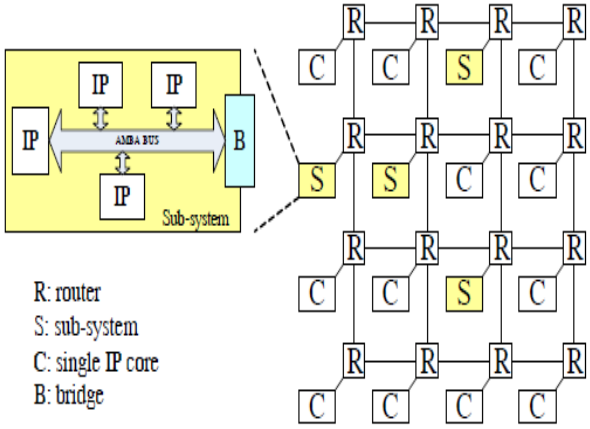


Fig. 1. Hybrid NoC architecture

2.1 Phases of I-Slip Algorithm

Step 1: The unmatched inputs send a request to the every output and confirms to form a queue .This is called as **REQUEST** phase.

Step 2: When unmatched output recives an request ,it choose the path having higest priority in round robin manner . and output notifies input that request is granted. This phase is known as **GRANT** phase.

Step 3: when unmatched input receives a grant then it accepts the one which has a highest priority in round robin. This phase is known as **ACCEPT** phase.

For different application ,bandwith is consider. Ip are mapped on same platform and graph it such that it requiresd less hardware and bandwidth. The proposed work is done using VHDL or VERILOG. This is done in the proposed paper using VHDL ,using modelsim 6.3f software.

3. PROPOSED WORK

This paper proposed a system which consist of mesh architecture having four by four matrix. The data is been passed through the matrix i.e. ip's. they are passed with the help of routers. The logic is set such that the data is been passed in the matrix which search their path which occupies the less time and hence latency is been decrease. The i-slip algorithm to route the data is been used. The hardware required for the proposed work is less than as compared to other router proposed.

The algorithm work as follows, the data is passed has specific source address and destination address. They are as a format x,y and x,y. When the data start communicating they will search in positive x then positive y and then negative x and negative y. Priority will be given as for first positive x,y then negative x,y. The data is not passed diagonally and hence some delay is been reduced. The input is been of 16 bit which is of frame format and output is of 8 bit. The detailed is specified below

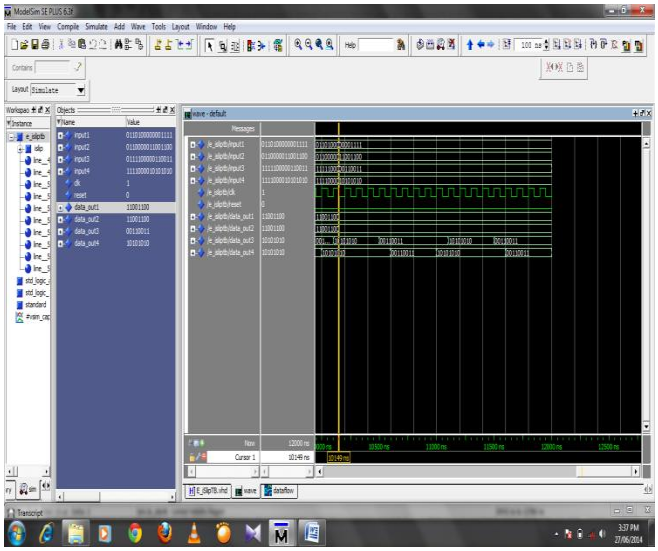
If we consider the mesh of four by four, then the input is specified as four inputs P1,P2,P3,P4. The first input P1 the row consider as naming 0,0; 1,0; 2,0; 3,0 which specified x,y coordinate. The second input P2 the row consider as 0,1; 1,1; 2,1; 3,1. The third input P3 the row consider as 0,2; 1,2; 2,2; 3,2. Now the fourth input P4 the row is specified as 0,3; 1,3; 2,3; 3,3. For example consider 1,0. 1 is address of x point and 0 is address of y point. This x and y address is used in frame format which is of 16 bit. Then logic is set as the data will pass in positive x and y direction and then the negative x and y direction.

The detail of the frame format used as input is specified as the first 0 to 7 bit is of data the given data is been specified.then the 8 to 10 bit is of don't care we can specified as 0 or 1.then then the 11 to 12 bit gives the destination y address and 13 to 14 bit gives the destination x address .15 bit is the request bit .this frame format specified is used as the input which is of fifteen bits.

Consider the following example we made the programming of the four by four matrix and we want to pass the data from the matrix 0,1 to 3,0 using I-Slip Algorithm data is of 8 bit format from 0 to 7 bit in frame format, let the data be11001100 .8 to 10 bit is don't care. 11,12 bit is address of y i.e. 11 and 13,14 bit is address of x i.e. 11 and the 15 bit is to enable so the frame format is 1111100000001111. Now in islip it will check or compare with the x and y destination coordinate. consider 0 is greater than three no then it will go to positive y direction .it will reach to 0,0 .after that it will check if two is greater than 0 ,yes it satisfied then it will go in positive x direction till it reaches to 3,0 .hence the output is given at 3,0. The output is shown in the given diagram.

4. RELATED WORK

Here the data is passed in the mesh hybrid NOC architecture with the help of the i-slip algorithm. The latency of the data communication is been observed and found its been reduced. The related work proposed for this paper is that this four by four matrix the data is assed with i-slip algorithm router is then combined with other four by four matrix which uses X-Y router to pass the data is been combined. And hence the communication latency of the data is been verified for the combined NOC architecture.



5. CONCLUSIONS

The proposed work uses the I-slip algorithm. The I-slip algorithm is guarantee the fast algorithm, since it completes in most N iteration. The I-slip algorithm is simple to implement. It is also a starvation free. It has high throughput. In proposed work ,since the data is travelled in the proper format and the required logic make the data communication between the ip's which is routed by the routers which have considered the concept of the bandwidth constrain take less time and hence the latency has been reduced over the data communication.

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