COMPARATOR DESIGN USING FULL ADDER

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Abstract

In this paper designing of comparator is done with the help of Full adder which is an important part of ALU and basically a basic functional unit of the DSP & microprocessors. In today's world of technology it has become very essential to develop such new design techniques which must reduce the power or area consumption. So here comparator are developed using various styles of full adder with the help of DSCH and Microwind tool with 120 and 70 nm technology.

Keywords: *Arithmetic Logical Unit (ALU), Full Adder (FA), Magnitude Comparator, Speed.*

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1. INTRODUCTION

Comparator is basically one of the basic and useful arithmetic components of digital systems and there are various approaches for designing CMOS comparators with different noise margin, operating speed, power consumption, and its complexity. In this paper Comparator design implementation is done by Full Adder which is one of the basic building blocks of many of the digital VLSI circuits. Several refinements approaches [1], [2] have been made regarding its structure since its invention even one can implement the comparator by flattening the logic function directly too. The main aim of those refinements is to reduce the transistors numbers which in term reduce the power consumption and increase the speed of operation [3]. One of the basic major advantages in reducing the number of transistors is to put more devices on a single chip there by reducing the total area.

In this paper, design techniques are implemented using Microwind Software which helps in drawing the layout of the CMOS circuit. And in digital system arithmetic, Magnitude comparator is used for comparison.

Magnitude comparator is such combinational circuit which compares two numbers say A and B, and then their relative magnitude is determined and outcome specified by three states which indicate whether A>B, A=B and A<B shown in figure 1.

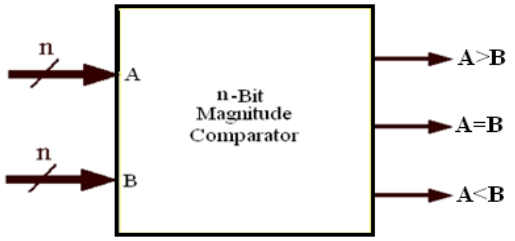


Fig-1: Block Diagram of n-Bit Magnitude Comparator

As said here we design comparator using Full Adder so here we design it as of 2-Bit so that analysis can be done. So FA based comparator (as said of 2-bit comparator) consist of full adders, inverters at one of the input and AND gate at the output side with two output shown in figure 2 and its truth table is shown in Table 1 below

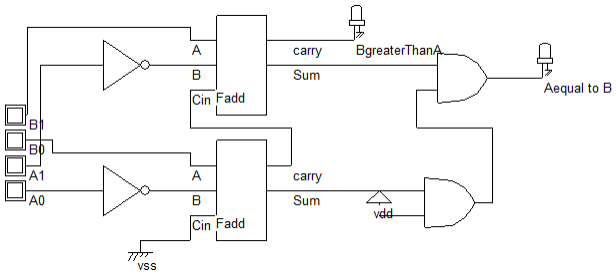


Fig-2: Basic Diagram of Full Adder based Comparator

Table -1: Truth Table of full adder based 2-bit comparator

A1	A0	B1	B0	B>A	A=B
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	1

2. DESIGN IMPLEMENTATION

Firstly a brief discussion is done about basic Full adder [4], [5] which consist of three inputs and two outputs as sum and carry. The logic circuit diagram of this full adder can be implemented with the help of various gates as XOR, AND and OR gates. Here the logic for sum requires XOR gate while the logic for carry requires AND, OR gates. The basic

diagram for full adder using its Boolean equations with basic gates can be represented shown diagrammatically in figure 3.

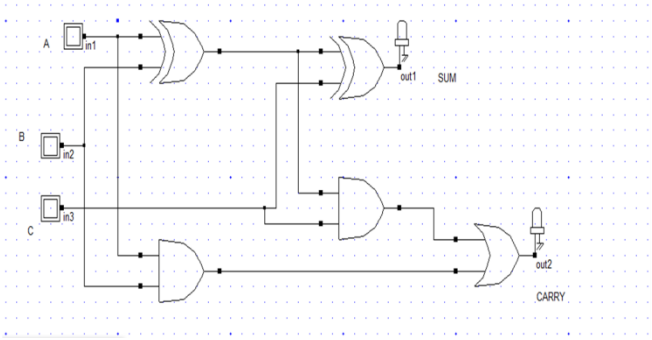


Fig -3: Basic Full Adder Logic

In designing of Full adder XOR gate plays an important role as using it performance of the full adder can be improved.

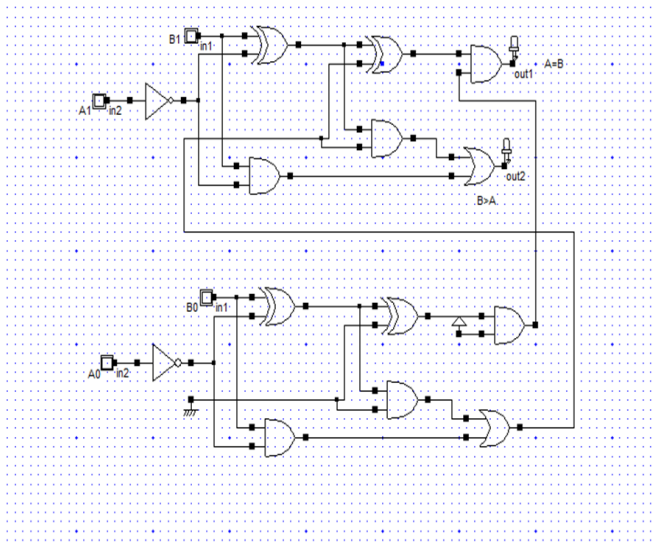
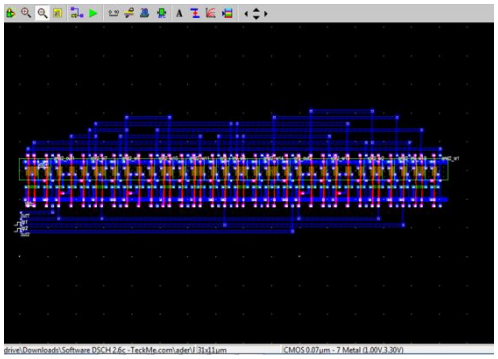
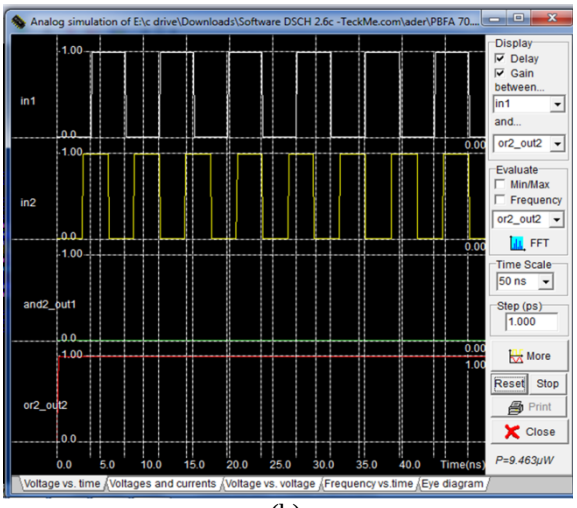


Fig -4: Basic Full Adder Based Comparator

The layout design of the basic full adder based comparator is shown in figure 5(a) and its analog simulation in figure 5(b).



(a)



(b)

Fig -5(a-b): (a) Layout Diagram (b) Analog Simulation of Basic Full Adder Based Comparator

Then another design of comparator using hybrid full adder is shown in figure 7 using figure 6.

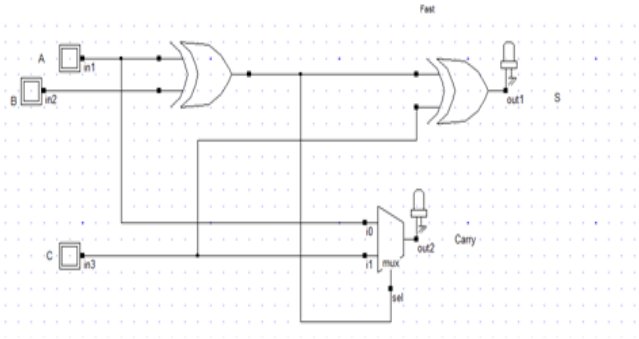


Fig -6: Basic Hybrid Full Adder

This comparator consists of XOR gate, MUX, NOT and AND gate with four input (A1, A0, B1, B0) and two output (A=B, B>A) as shown below.

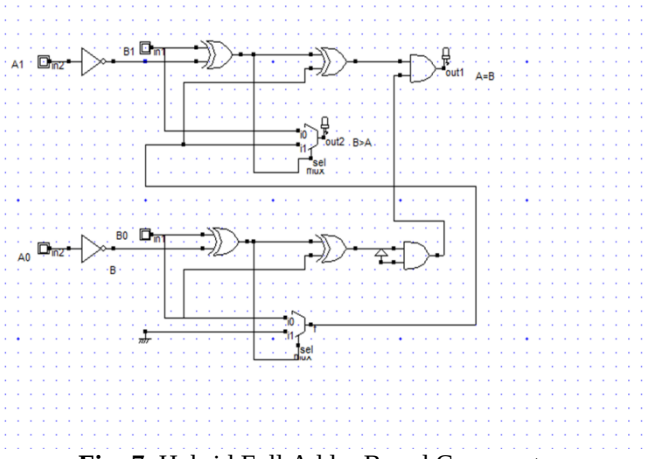
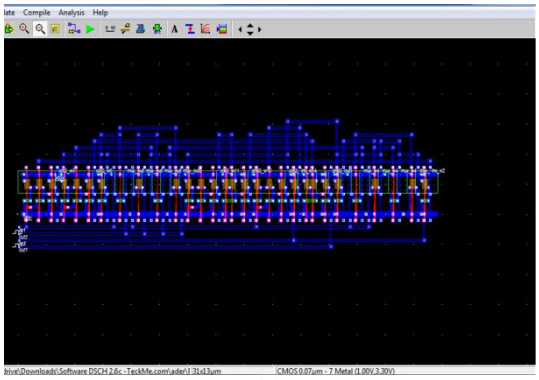
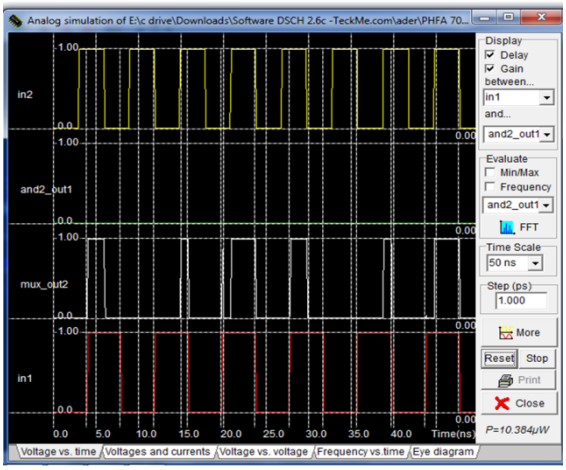


Fig -7: Hybrid Full Adder Based Comparator

The layout design of hybrid full adder based Comparator is shown in figure 8(a) and its analog simulation in 8(b).



(a)



(b)

Fig -8(a-b): (a) Layout Diagram (b) Analog Simulation of Hybrid Full Adder

As said earlier one can implement the comparator by flattening the logic function directly which is shown in figure 9.

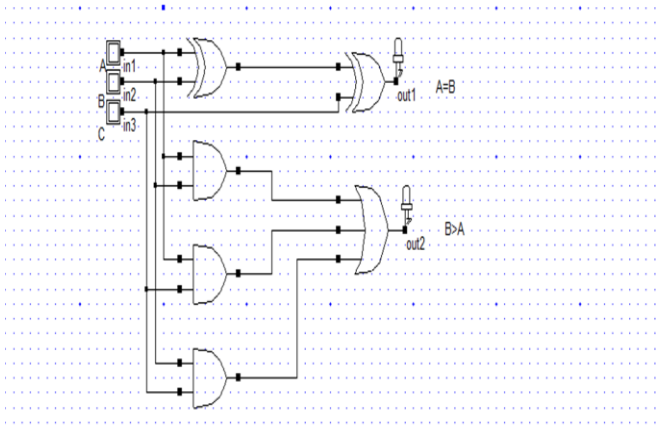


Fig -9: Direct Logic Based Full Adder

So another design of comparator can be in such way shown in figure 10 which is based on direct logic with four input (A1, B1, A0, B0) and two output (A=B, B>A).

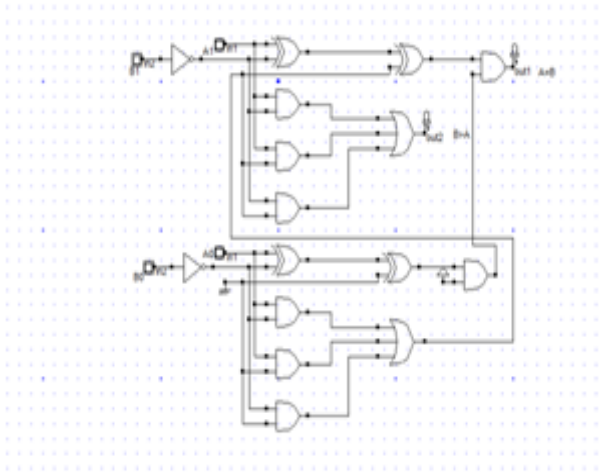
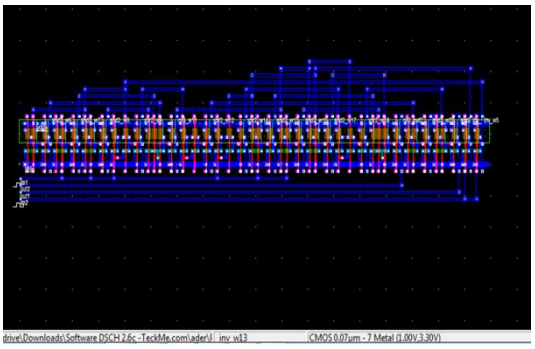
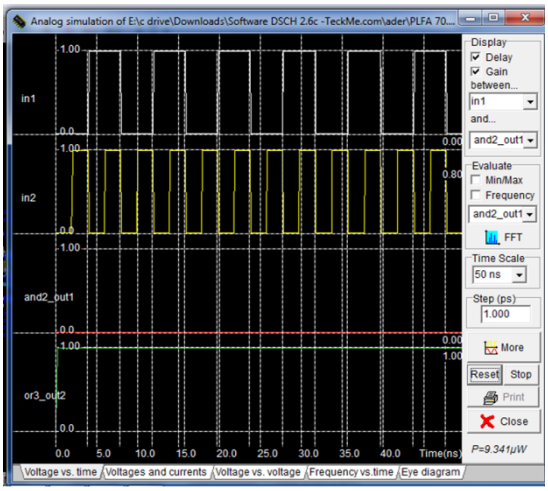


Fig -10: Direct Logic Based Adder Based Comparator

The layout design of comparator using direct logic of full adder is shown in fig.11 (a) and is analog simulation in fig. 11(b).



(a)



(b)

Fig -11(a-b): (a) Layout Diagram (b) Analog Simulation of Direct Logic Full Adder Based Comparator

3. RESULT ANALYSIS

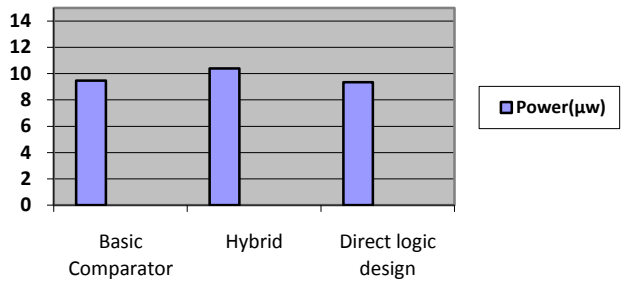
Here analysis and comparison of different logic styles of comparator using various logic styles of full adder is shown in table.2 based on simulation obtained from in Microwind

Tool or Software. Simulation is done in various steps. As to obtain simulations compile the Verilog file in Microwind and that Verilog file is created from the schematic circuit diagram, which is designed DSCH part of Microwind software. Here we design schematic diagram in DSCH at 120nm technology and simulation is at 70 nm technology at room temperature.

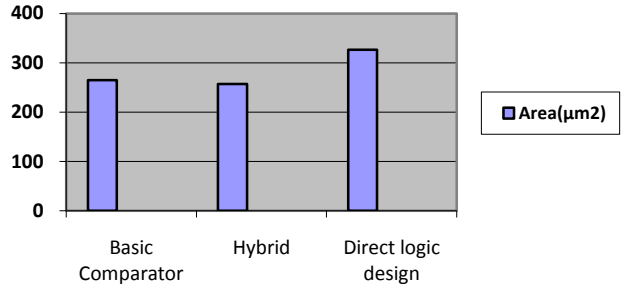
Table -2: Comparison of various Full Adder Based Comparator based on simulation

Full Adder Based Comparator Design	Area(μm^2)	Power(µw)	Routed wires
Basic Full Adder	264.7	9.463	25
Hybrid	257.1	10.384	36
Direct logic design	326.2	9.341	30

All these analysis is shown by graphical way in form of chart below



(a)



(b)

Chart -1(a-b): Comparison Chart of various Full Adder based Comparator based on (a) Power (b) Area

4. CONCLUSIONS

This paper describes various logic styles of full adder for designing a comparator and found that each has its own advantage and its specification as one has less power consumption or less area or routing wires numbers than other as shown in Table 2. So it depends on the designer and its requirement which logic style is to be used and can be helpful in implementation of higher design of comparator and performance.

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