IMPLEMENTATION AND ANALYSIS OF POWER REDUCTION IN 2 TO 4 DECODER DESIGN USING ADIABATIC LOGIC

Ranjan Kumar Singh[1], Rakesh Jain[2]

[1]*M.Tech student, Department of ECE, SGVU, Jaipur, Rajasthan, India*
[2]*Assistant Professor, Department of ECE, SGVU, Jaipur, Rajasthan, India*

Abstract

This paper presents 2 to 4 decoder structure design using CMOS and adiabatic technique. The paper discussed Power consumption in 2 to 4 decoder circuit using adiabatic technology, because now a day's power consumption is the important and basic parameters of any kind of digital integrated circuit (IC).And there is a challenge to compensate power and performance to meet the systems requirement, because cost of the system is directly affected by power. It is done through the adiabatic techniques because adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging and which recycle the energy from output nodes instead of discharging it to ground. In this paper we have reduced the power consumption of 2 to 4 decoder circuit. We have taken a time varying source instead of DC supply and obtained the further results. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage Vdd and discharging it to ground respectively. All simulation result and analysis are performing on 250nm MOSIS technology using tannerEDA tool.

Keywords: *Adiabatic process, power consumption, VLSI design, switching activity.*

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1. INTRODUCTION

Now a day's power reduction is a major issue in technology world. The low power design is a major issue in high performance digital system, such as microprocessors, digital signal processor (DSPs) and other applications. Chip density and higher operating speed lead to the design of very complex chips with high clock frequencies [1]. So designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products. In this paper 2 to 4 decoder is designed by using adiabatic technology.

There is always a tradeoff between power and performance to a VLSI system. Paper discussed about the design of 2 to 4 decoder circuit by using adiabatic technology.

Paper discussed the design of 2 to 4 decoder by adiabatic logic technologies and compared the power dissipation at various frequency labels

Adiabatic logic: In this section we have discussed about the adiabatic logic, it is used to reduce power dissipation in the circuit. Since power dissipates in cmos circuits due to the charging and discharging process of the output capacitor. If we reduce the number of switching activity of charging and discharging process then we can reduce the power dissipation in the VLSI designed circuit

In adiabatic logic we replace the main VDD by the time verying source through which we can reduce the time for reduced the switching activity.

This paper is organized as follows. Section II explains the previous work using adiabatic logic using DC source, whereas section III contains the proposed 2 to 4 decoder using adiabatic logic. Section IV describes the implementation results and detailed comparison of 2 to 4 decoder using various sources.Section V gives Conclusion of proposed work. In section VI, the Future scope of this paper is written.

2. PREVIOUS WORK

Design and analysis of CMOS cells using adiabatic logic: we have discussed about two types of inverter structure design using CMOS and adiabatic technique.the important and basic parameters of any kind of digital integrated circuit (IC) is power consumption. To meet the systems requirement we will have to manage between power and performance. Cost is also a basic parameter because System cost is directly affected by power. Adiabatic circuits works on the principle of adiabatic charging and discharging and which recycle the energy from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage Vdd and discharging it to ground respectively. All simulation result and analysis are perform on 180nm TSMC technology using tanner tool[2-4].

2.1 Proposed Adiabatic Logic Inverter

Adiabatic switching is commonly used to minimize energy loss during the charge/discharge cycles because during the adiabatic switching techniques all the nodes are charged/discharged at a constant current to minimize energy dissipation. As opposed to the case of conventional charging we will have to decrease the rate of switching transition in adiabatic circuits because of the use of a time varying voltage source instead of a fixed voltage supply. This is

accomplished by using AC power supplies to charge the circuit during the specific adiabatic phases and subsequently discharge the circuit to recover the supplied charge.

Let us assume, during evaluation phase the input (In) is high and input (InB) goes low accordingly, consequently M3 is conducting and output (OutB) follows the power supply Va, and at the same time M1 gets turned ON by output (Out) and thus reduces the charging resistance. Being in parallel with M3 and during hold phase, charge stored on the load CL flows back to power supply through M1. So that power dissipation is reduced. The proposed circuit uses two MOS diodes, one is connected to Out and Va and other diode is connected between Common source of M5-M6 and other power supply VaB, Both the MOS diodes are used to increase the discharging rate of internal nodes capacitance.

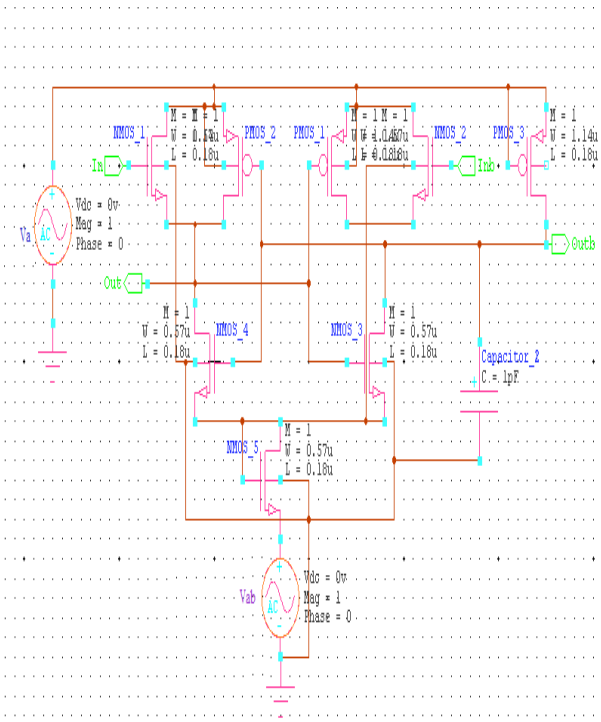
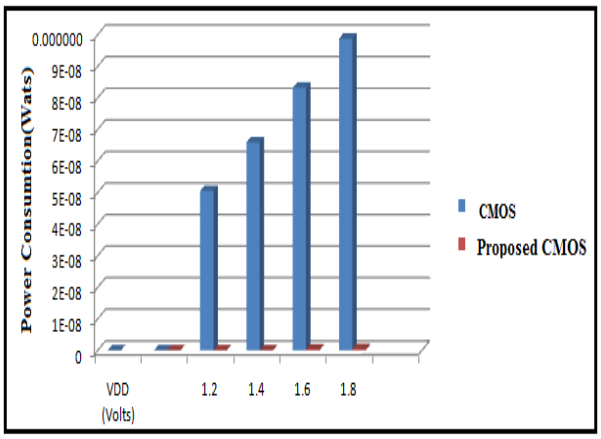


Fig1: Proposed adiabatic logic Inverter circuit

The proposed circuit uses two MOS diodes, one is connected to Out and Va and other diode is connected between Common source of M5-M6 and other power supply VaB, Both the MOS diodes are used to increase the discharging rate of internal nodes. these are all about the previous work which is done on the adiabatic inverter due to inverter circuit is very comfortable for adiabatic logic technique

2.2 Power Consumption Comparison of Proposed Inverter vs. CMOS at Power Supply



3. PROPOSED POWER ANALYSIS ON 2 TO 4 DECODER CIRCUIT

Now a day's power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. So designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products..In this paper 2 to 4 decoder is designed by using adiabatic technology. Paper discussed the design of 2 to 4 decoder by adiabatic logic technologies and compared the power dissipation at various frequency labels.

3.1 DC Source Adiabatic Logic Circuit

In the 2 to 4 decoder circuit when we apply DC source then there is no change in frequency. And dissipated energy depends upon the switching activity in the circuit. So power consumption in DC source circuit is greater than others. The decoder circuit is same for both analysis only sources is changed. So in the given design of decoder circuit there are two inputs A and B which is passed through inverter circuit and makes their Abar and Bbar. There are four outputs F1, F2, F3, F4 obtained from NAND gate. Here F1,F2, F3,F4 is taking input AbarBbar, Abar B, ABbar and AB respectively. In decoder design using VDD source the charging and discharging process is takes place through constant current. So there is more power dissipated in decoder circuit using constant source. For this problem we will use time varying source instead of constant source.

3.2. Time Verying Source Adiabatic Logic 2 To 4 Decoder Circuit

In the previous section (A) we have written circuit description. In that description we have discussed that if we will use time varying source instead of VDD source then

there will be less power dissipation in decoder designed circuit.

So now we are going to explain that how it will reduce power dissipation. Let we are taking output part F1 in the decoder circuit, then If we use time varying source then for the positive half cycle the output capacitor is charged through PMOS transistor and for the discharging time we reduce frequency means we will increase the time period so that there will take less discharging through NMOS transistor. So that's why it reduced power dissipation in the circuit.

In the time verying source we can change the time,meance for the minimum power consumption we will have to increase the time of switching activity and due to time verying source we increase T

Systematic Diagram of Time Varying Source 2 to 4 Decoder Circuit

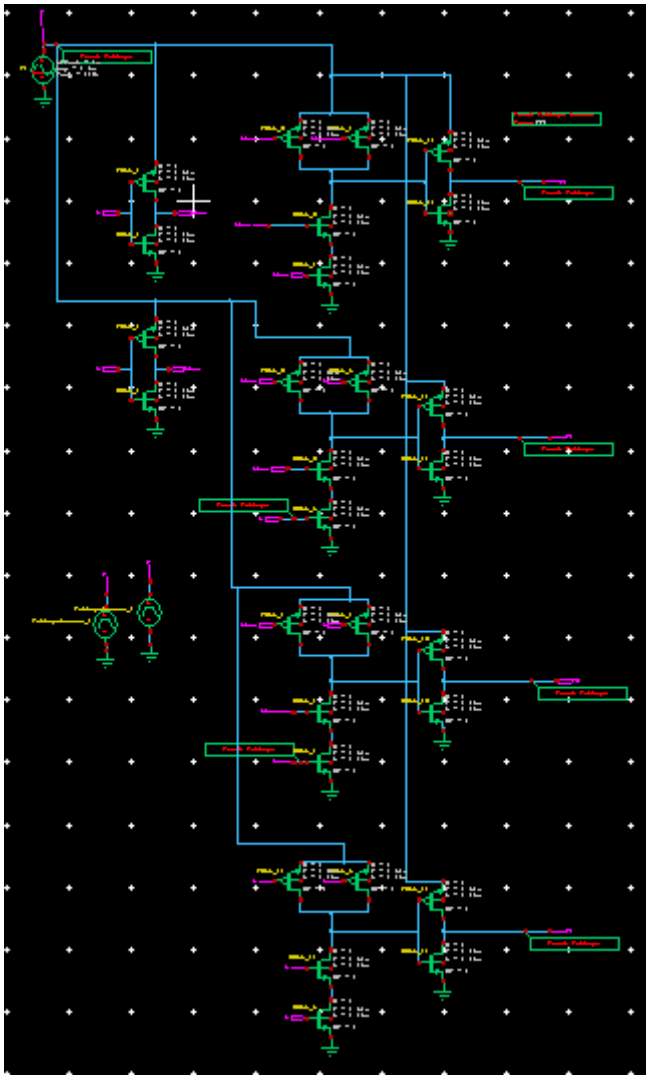


Fig 2 Systematic diagram of time varying source 2 to 4 decoder circuit

means $E_{AL} = 2\,RC/T\,(CVDD^2)$

If we increase T then it will further decrease of frequency. So for minimum power consumption we will decrease our source frequency.

4. RESULTS AND COMPARISON

In this paper we have worked on the power analysis on the 2 to 4 decoder circuit using adiabatic technology. if we use any where decoder circuit using DC source then it will consume more power ,so for this we are using Adiabatic techniques, Means we will use time varying source with different frequencies. Here we have taken a 2.5V source then power consumed is 1.888681e-

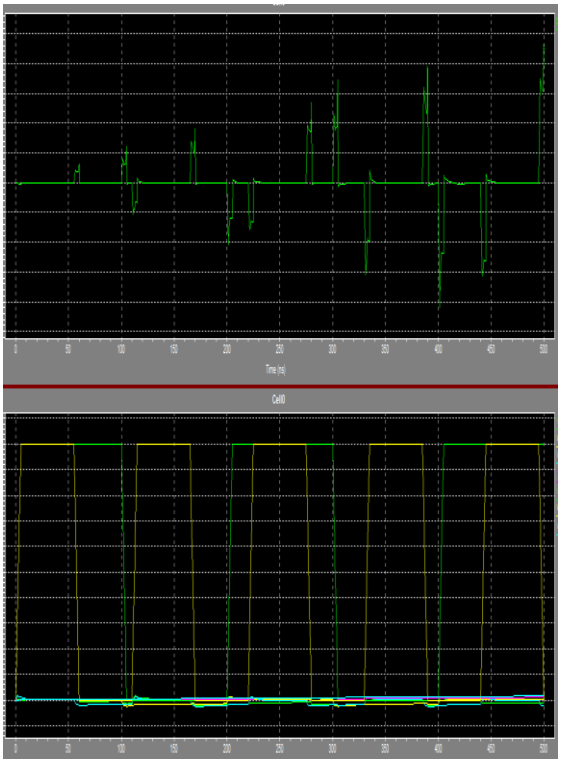


Fig. 3: Output waveform of time varying source adiabatic logic 2 to 4 decoder circuits

02 watts and when we took time varying source at frequency 100000 Hz at same magnitude then power consumed is 2.221764e-005 watts means power dissipation is less than DC source circuit.

Power Analysis Table of 2 to 4 Decoder Circuit is given below

In this section we are going to do analysis of power reduction in 2 to 4 decoder design. As we mentioned that the power reduction in VLSI designed system is achived less by using adiabatic logic as compare with conventional CMOS logic design.

In this table we have analyze that power consumption in 2 to 4 decoder circuit design is less by using time varying source as compare to by using VDD source.

Table 1 Power analysis in 2 to 4 adiabatic decoder

	Using DC source	Using time varying source at			
		100000hz	10000hz	100hz	
Power analysis of 2 to 4 decoder circuit	1.888681e-002 watts	2.221764e-005 watts	8.509453e-010 watts	2.805546e-012 watts	

5. CONCLUSIONS

In the proposed design, we have achieved low power consumption after applying adiabatic techniques on 2 to 4 decoder designed circuit for high-performance DSP applications and integrated circuits.2 to 4 decoder circuits are designed using GATE into MOS. The proposed 2 to 4 decoder design provides noticeable consumption in power and high speed operation. In this paper we have achieved less power consumption in 2 to 4 decoder circuit than conventional decoder design. Simulation results obtained from the proposed decoder and CMOS gate at low frequency. The comparison of the power consumption of the proposed decoder circuit with other conventional methodologies has proved that power consumption with the proposed adiabatic logic is far less as compared to CMOS based technique.

All simulation result and power analysis are performing using 250nm MOSIS technology using tannerEDA tool.

6. FUTURE SCOPE

Now a day's power and performance are most valuable point in electronics world, adiabatic technique is used to reduce power consumption but this technique has not used at wide range, So in the future it will bring revolution in power consumption in many circuit design. Because this logic is very easy to apply and works on low cost. Every user wants high power backup in electronics devices so in future this logic will apply on more vlsi design and will make better.

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BIOGRAPHIES

[1]Ranjan Kumar Singh, a M.Tech student (V.L.S.I) at Gyan Vihar School of Engineering and Technology, Jaipur, Rajasthan. He has completed his B.Tech (Electronics and Communication) in 2013 under dual Degree Program at Gyan Vihar School of Engineering and Technology, Jaipur. His main research interests are in Implementation and analysis of Power reduction in 2 to 4 decoder design using adiabatic logic.

[2]Rakesh Jain, is an Assistant Professor at Gyan Vihar School of Engineering and Technology. He has completed his M.tech (V.L.S.I) from Mewar University in 2012, He has completed is B.E in Electronics and Communication from Rajasthan University in 2009. His main research interest is in Low- power Digital Design.