POWER ANALYSIS OF 4T SRAM BY STACKING TECHNIQUE USING TANNER TOOL

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Abstract

As the technology in electronic circuits is improving, the complexity in these circuits also increases. The complexity in the circuits leads to the need of that type of circuits which are portable and fast circuits. The portability in the electronic circuits are achieved by the use of battery. So we have to develop such type of circuits that consume very less power. The major focus in designing a high performance digital system such as microprocessors and various Digital signal Processors is given to low power design. The main part of any digital system is its memory unit. It is not possible to design a digital system without memory. So we can say that memory is the main part which utilize the maximum power in the system. The most used memory cell in the digital systems is the SRAM cells. They are the static RAM cells. Low-power Random Access Memory (RAM) has seen a remarkable and rapid progress in power reduction. The high density and low power SRAMs are needed for application such as hand held devices, laptops, notebooks, IC memory card because of the fact that they are portable devices and uses batteries for power source so they must consume power as low as possible. The power dissipation reduction is not only due to power supply voltage reduction, but also can be done by low power circuit techniques. It should be designed such that it provides a non- destructive read operation and reliable write operation [1].The proposed 4-Transistor with resistive load memory cell makes use of Stacking effect to reduce the leakage current. The stacking effect is used by switching off the stack transistor when the memory is in ideal mode. So the stacking transistor implemented in the circuit behaves like a switch which remain in off state when the cell is in off state and it remain in ON state when Write or Read operation is performed in the memory cell. The tool used is TANNER EDA for schematic simulation. The simulation technology used is MOSIS 250nm.

Keywords- *4T SRAM, Stacking Effect, Conventional SRAM, TANNER EDA Tool, Tail NMOS*

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1. INTRODUCTION

The SRAM cells are the main memory devices that are being used in the modern digital system. These are the semiconductor memories that are used as a storage unit. Before SRAMs various other storage devices were used like magnetic tapes, optical discs and drives. But after the SRAM were manufactured these become the most widely used storage device. SRAM is one of the two type of RAM, the other one is the DRAM. SRAMs are the volatile storage device, means the data stored on it are not permanent. Here data is lost when power is removed. Unlike DRAM, SRAM does not require data refresh, means the data in SRAM does not 'leak away', so no need to refresh cycle in SRAM. These memory devices can be manufactured on a single chip. The single chip fabrication increase the density of components on the chip thus causing increase in power dissipation. So there is requirement of such design which dissipates low power. For low power operation unnecessary usage of power should be reduced. The main parameter causing increase in power dissipation is Leakage current. Leakage power contains mainly three components, they are Gate Leakage, Sub threshold Leakage and Junction Tunneling Leakage In this paper the leakage current will be reduced by using tail NMOS, i.e. Stacking Effect [2].

2. CONVENTIONAL 4T SRAM CELL

The 4T SRAM consists of two cross coupled inverters and two access transistors. The load devices used in this design are made of poly silicon resistors or it can be depletion type nMOS or pMOS. The enhancement type nMOS are used as the pass gates which acts as the data access switches. The use of resistive load

Inverters with un doped poly silicon resistance in the latch structure results in a significantly more compact cell size as compared to the other SRAM design. The value of the resistance used in this design should be low such that it can attain acceptable noise margin for the resistive load inverter. On the other hand, a high value of load resistance is used to reduce the amount of standby current being driven by the memory cell. So there is a balance between high resistance required for power and to provide wider noise margin[3].

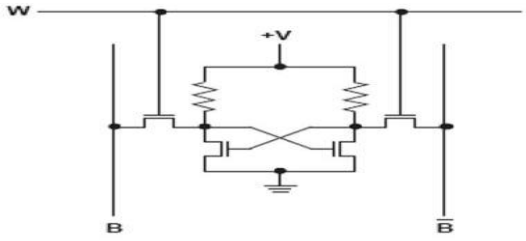

Fig-1: 4T SRAM Cell

2.1 Operation of 4T SRAM

The basic operation of any SRAM is performed in three different modes. The modes are Standby Mode, Write Mode and Read Mode. These operation are performed by using two nMOS, two pass transistor both of which are driven by row select line or the 'word line'. The 4T SRAM Cell is accessed through two Bit Lines. This arrangement is more reliable.

2.1.1 Standby Mode

In this mode the word line is not asserted. The pass transistor will disconnect the cell from the bit lines. So if the word line is not asserted then the access transistor or pass transistor does not let the memory cell to connect with the bit lines (Bit and Bit bar).This will cause the two cross coupled inverter formed to continue to strengthen each other to the supply. When cell is in standby mode no action could be taken and to store the data more power is consumed by the SRAM. So there is need of techniques to reduce the leakage current.

2.1.2 Read Mode

The read operation is started by enabling the word line (WL) and joining the bit lines Bit and Bit bar to the internal nodes of the cell. The voltage of column Bit is remained high and volume of Bit bar is pulled down. Now the difference in the voltages of both the columns are detected and the difference is amplified as a logic '1' output. The read operation for '0' is performed vice-versa. The difference between Bit and Bit bar should be minimum and this difference is sensed and amplified as logic '0' [3].

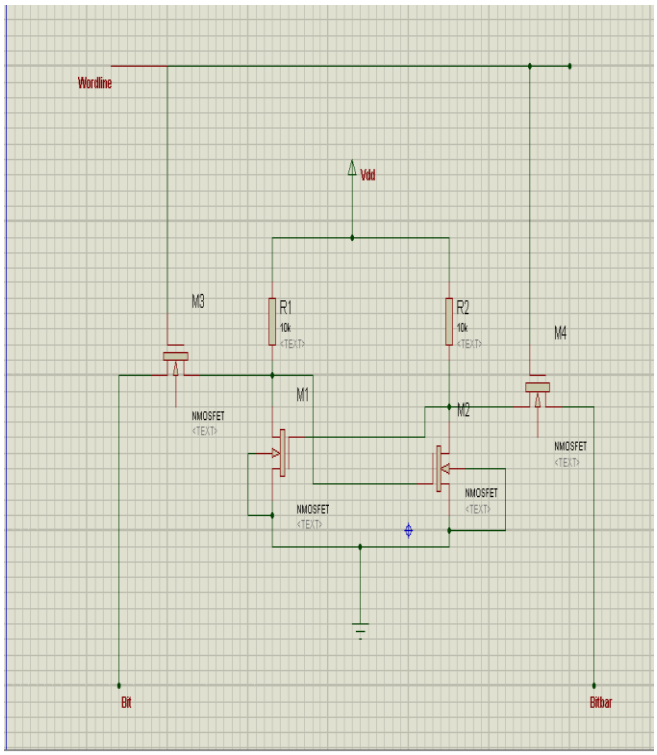

Fig-2: Design of Basic 4T SRAM Cell

2.1.3 Write Mode

The write operation is performed by applying the desired value to the bit line 'Bit'. Like if we wish to write logic '1' then we make 'Bit' to high and 'Bit bar' to low. Similarly if we want to write logic '0' then we perform the operation in vice-versa. The word line WL should be asserted for this mode.

3. PROPOSED SRAM CELL DESIGN

The proposed SRAM cell design is shown in Figure-3. In the proposed design the assimilation of power and area are put together as compared to the previous design. The propose design targets the 4T SRAM Cell with no functionality disorder, at the same time it also uses the stacking at the tail transistor with suitable aspect ratio (W/L) ration for the transistor.In Stacking Technique both NMOS transistor and PMOS transistors in various logic circuits can be split into two transistors. The current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the NMOS transistor and also due to an increase in the drain to source voltage in the NMOS transistor. The proposed SRAM cell design is based on the fact that the barrier height of hole (4.5 eV) is greater than the barrier height of electrons (3.1 eV). Due to this fact, when the nMOS is in OFF state the leakage current will be lower[4]. The main reason of stacking the nMOS transistor in leakage power reduction is due to the self reverse biasing of the transistor connected in series[4]. Here the tail transistors are connected the control signal 'CS'. When the word line is asserted means when word line= '1', the cell behaves as a normal 4T SRAM cell and the pass transistor are turned ON. When word line is not asserted means word line = '0', then the pass transistor is OFF and is operated in standby mode.

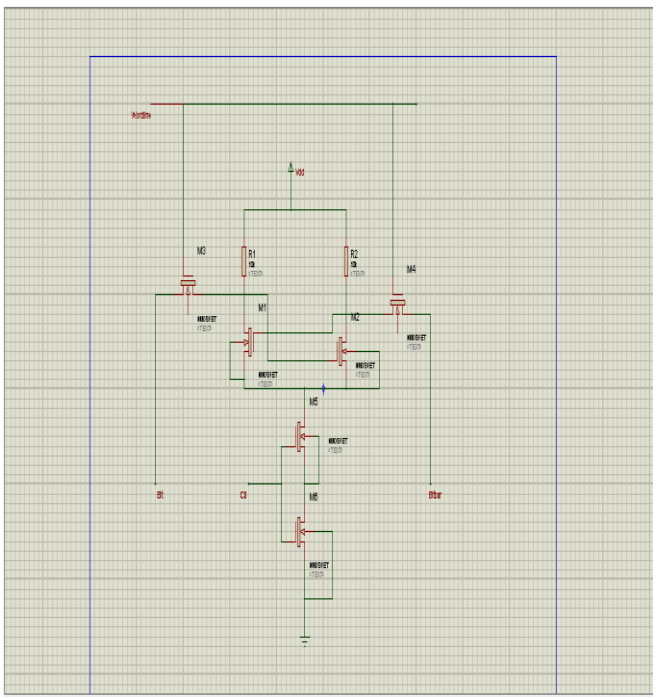

Fig-3: Proposed SRAM Cell Design

The stacking transistor is controlled by control signal CS. These nMOS transistor behaves as a switch. It depends on the input signal CS. If CS = '1' the transistor will work as close switch or ON and when CS = '0' then the transistors will act as open switch or OFF state. The read, write and standby operation is same as the conventional 4T SRAM. The stacking effect depends on the control signal CS. To sink the leakage current the stacking transistor should be in ON state. Hence the control signal should be '1' means CS= '1'. This arises the need of transistor of larger size. The increase in size of transistor will improve the read time of cell. This will affect the threshold voltage and thus reduce the speed. The external control signal can be produced through a separate row decoder and this circuit is activated before the word line is activated for the read, write operation [4].

4. SIMULATION ANALYSIS

The tool used for schematic simulation of conventional SRAM Cell and the proposed SRAM cell is TANNER EDA for. The simulation technology used is MOSIS 250nm. The parameters of the circuits and simulation conditions are summarized in Table-1.

Table:1 Parameters of the circuits

Device Name	**MOS Size(nm)**
nMOS(NMOS_1,2,3,4)	W/L=2.25/2.50
nMOS(NMOS_5,6)	W/L=1.25/0.25
Simulation Condition	
Vdd	2.5V (DC)
Word line	5.0V (Pulse)
Bit line	2.5V (DC)

5. RESULTS AND CONCLUSIONS

The simulation of conventional as well as the proposed cell has been performed according to the parameters shown in Table-1. The results we obtain shows that the power consumption of proposed cell is much less than the conventional SRAM cell. The comparison of both the circuit for write '1' operation can be given with the help of Table-2.

The proposed SRAM Design is intent to realize to consume less area as well less power compared to previous design; the incorporation of Stacking Technique in the proposed design is intent to bring a significant reduction in power consumption as compared to design in Figure-2. So we found that we can reduce the power consumption in SRAM by using stacking technique.

Table-2: Comparison of both circuits for write '1'

Conventional SRAM cell	**Proposed SRAM Cell**
P_{max}≈9.9381µw	P_{max} ≈8.5974µw
P_{min}≈ 7.9882µw	P_{min}≈ 6.5542µw
P_{avg}≈ 8.9203µw	P_{avg}≈ 7.4822µw

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BIOGRAPHIES

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