

A COMPARATIVE STUDY OF FULL ADDER USING STATIC CMOS LOGIC STYLE

Manisha¹, Archana²

¹Student, Electronics and Communication Engineering, DCRUST Murthal (Sonapat), Haryana, India

²Student, Electronics and Communication Engineering, DCRUST Murthal (Sonapat), Haryana, India

Abstract

In this review paper 1-bit CMOS full adder cells are studied using standard static CMOS logic style. The comparison is carried out using several parameters like number of transistors, delay, power dissipation and power delay product (PDP). The circuits are designed at transistor level using 180nm CMOS technology. Different full adders are studied in this paper like Conventional CMOS (C-CMOS), Complementary pass transistor logic (CPL), Double pass transistor logic (DPL), Transmission gate (TGA), Transmission function (TFA), New 14T, Hybrid CMOS, HPSC, Pseudo nMOS, GDI full adders.

Keywords: PDP, CMOS full adder, power dissipation, low power, logic style.

-----***-----

1. INTRODUCTION

The addition is a basic arithmetic operation and act as the core of other arithmetic operations like multiplication, division, subtraction, address generation etc. Adders are the key element in many VLSI systems such as microprocessors, ALU's, multiplexers, comparators, parity checkers, digital signal processing (DSP) architectures, code converters etc. The most required feature of modern electronics is low power energy efficient building block that enables the implementation of long lasting battery operated systems [1]. There is no a single type of 1-bit adder which can be used for all type of applications, so, different type of logic styles are used for designing a full adder cell to cover a wide range of performance characteristics to satisfy different applications [2].

For performance analysis of various full adders different parameters are measured like power dissipation, delay, number of transistors used and power delay product of circuit. In a design it is optimised desired that the circuit consume less power, have very less delay, low supply voltage and avoid degradation in output voltage [3]. In the last decades many logic styles have been proposed and each design has its own merits and demerits. It is very important for circuit design to have good drivability under different load conditions and also balanced output to avoid glitches. The time delay depends on size of transistors, number of transistors used, logic depth, parasitic capacitance and capacitance due to intercell and intracell routing and also on number of inversion levels [5]. Power dissipation depends on switching activity, the number and size of transistors, node capacitance, wiring complexity etc.

$$P_{avg} = P_{static} + P_{dynamic} + P_{short-circuit}$$

The energy consumed by gate per switching element is known as PDP. The power delay product is a measure of efficiency in an adder circuit. There is a tradeoff between

power dissipation and speed and is very important when low power operations are needed [3]. It is given by

$$PDP = \text{Power} * \text{DELAY}$$

Reducing the number of transistors may lead to reduced power but sometime does not improve. The die area depends on number and size of transistors and routing complexity. All these characteristics of full adder vary from one logic to another logic [4].

In this paper different full adders are compared at transistor level using 180nm CMOS technology.

This paper is organised as follows:- Section-II gives the review of different CMOS logic styles. Different 1-bit full adders are reviewed using static CMOS logic in section III. In section IV comparison of delay, average power and PDP are compared. Finally in section V conclusion of paper is given.

2. LOGIC STYLE USED

The CMOS logic circuits are categorised into two categories:- static and dynamic logic circuits. These different logic styles are used according to design requirements such as power consumption, speed and area.

In a static logic circuit a logic value is retained by using the circuit states while in a dynamic logic circuit a logic value is stored in the form of charge [5]. So, in static logic circuit each output of the gate assume at all the times the value of Boolean function implemented by the circuit. So, at every point the output will be connected to either V_{dd} or gnd via a low resistance path [4]. The static logic eliminates precharging and decreases extra power dissipation, thus, widely used for low power circuit designs.

Static logic is further of two types:- single rail and dual rail logic. Single rail uses its input either true or complementary output signals [5]. However dual rail uses its input either true or false and yield both true or false signals as their output at the same time. Most commonly used static logics are Pseudo-nMOS, fully CMOS, transmission gate logic (TGL), pass transistor logic (PTL), gate diffusion input logic (GDI), complementary pass transistor logic (CPL), double pass transistor logic (DPL) [3][4][5][9].

3. FULL ADDER CELLS USING STATIC LOGIC

Adder is a circuit that operates for a given three 1-bit inputs A, B, C and two 1-bit outputs sum and carry.

$$S = A \oplus B \oplus C \quad (i)$$

$$S = C' \cdot (A \oplus B) + C(A \odot B) \quad (ii)$$

$$\begin{aligned} \text{Carry} &= A \cdot B + C(A \oplus B) \\ &= C(A \oplus B) + A(A \odot B) \end{aligned} \quad (iii)$$

$$A \oplus B = A'B + AB' \quad (iv)$$

$$A \odot B = A \cdot B + A'B' \quad (v)$$

Many full adder cells designed with the help of static logic in 180 nm CMOS technology [1][2][3][4].

3.1 Pseudo-nMOS Full Adder

This adder cell is operated by Pseudo-nMOS logic (ratioed logic). The CMOS pull up network is replaced by a single pMOS transistor with its gate grounded. Since the pMOS is not driven by signals, it is always 'on'. The effective gate voltage seen by the pMOS transistor is V_{dd} . When the nMOS is turned 'on', a direct path between supply and ground exists and static power will be drawn [9]. It uses 18 transistors to make full adder cell. The operation is realized by negative addition [5].

Advantage of using Pseudo-nMOS logic is that it gives high speed and less number of transistors than CCMOS and disadvantage is that it has reduced output swing, increased power consumption of pull up transistor and more susceptible to noise.

3.2 Conventional CMOS Full Adder

This adder cell uses 28 transistor based on regular CMOS structure (pull-up and pull-down networks). Complementary transistor pairs make the circuit layout straight forward. CCMOS generates carry through a static gate [6]. The advantage of using CCMOS is that it has layout regularity, high noise margins and stability at low voltage due to complementary transistor pair and smaller number of interconnecting wires [7] and disadvantage is that it uses C_{out} signal to generate sum which produces an unwanted additional delay. It has weak o/p driving capability due to series transistors in output stage and consumes more power and large silicon area [4].

3.3 Full Adders using Pass Transistor Logic

3.3.1 Pass Transistor Logic

In this logic either nMOS or Pmos is sufficient to perform logic operation, so, number of transistors and i/p load decreases and also the V_{dd} to gnd paths are eliminated [7]. It is used for low power applications.

3.3.2 Complementary Pass Transistor Logic

This adder cell uses 32 transistors. It is based on multiplexer logic so it needs all inputs in true as well as in complement form. In order to drive other gates of the same type, it must produce the outputs also in true and complement forms. So each signal is carried by two wires [9]. Hence CMOS output inverters with pass transistor logic to give complementary inputs and outputs. To generate sum out and carry out signal are used in this adder cell so, it is not suitable for low power applications. Advantage of CPL is that it is faster than CCMOS full adder and disadvantage is that it is not suitable for low power applications and it has wiring complexity and high delay [4].

To reduce power consumption of CPL SR-CPL (swing restored CPL is used to overcome multi-threshold voltage drop) and LCPL (single rail pass transistor logic) logics are used.

3.3.3 Double Pass Transistor Full Adder

It uses 28 transistors. In this adder cell both nMOS and pMOS logic networks are used so, it reduce the threshold loss problem [8]. It is a modified version of CPL and for full swing operation it uses complementary transistors. Advantage of DPL is that it reduces the problem of CPL (noise margin and speed degradation at low power supply). It also avoids series sizing and balanced input capacitance. Disadvantage is that it requires large area due to presence of pMOS transistors.

3.4 Full Adders using Transmission Gate Logic

3.4.1 Transmission Gate Logic

A CMOS transmission gate is constructed by parallel combination of nMOS and pMOS transistors, with complementary gate signals. It gives full swing output so, its use give better speed in CMOS circuit but there is no isolation between input and output.

3.4.2 Transmission Gate CMOS Full Adder

This adder cell uses 20 transistors. It has good delay, power dissipation and PDP than CCMOS and CPL. It gives better speed than static CMOS, CPL and requires less number of transistors. It has high number of internal nodes which leads to an increase in parasitic capacitance [5]. In large arithmetic circuits it gives poor performance. Additional buffers are required at each output due to their weak driving capability which increases power consumption and area.

3.4.3 Transmission Function Full Adder

This adder cell uses 16 transistors. Its operation is also based on transmission gate logic. In its circuit there are two possible short circuit paths to ground. To derive the load pull-up, pull-down and CPL are used in its circuit. It gives same delay for sum and carry output. It consumes less power and less area [2].

3.4.4 XOR and Transmission Gate Full Adder

This adder cell uses 14 transistors for adder operation. A XOR gate and transmission gates are used in combination for its design [2]. It is also known as 14T adder. The half sum is generated by XOR gate and transmission gates will generate the sum and carry output [4]. This adder cell occupies less area. It has low activity factor so consumes less power.

3.4.5 New 14T Full Adder using Transmission Gate

This adder cells uses 14 transistor to perform full adder operation as the name indicates. It uses hybrid logic style (use more than one logic style). It uses a XOR/XNOR circuit with feedback loop and transmission gates in its implementation. This adder has improved output than single logic adders. This adder has reduced number of transistors and power dissipating nodes but it has less driving capability and noise immunity [3].

3.5 Gate Diffusion Input Technique based Full Adders

It is a simple cell like inverter whose both nMOS and pMOS are connected to N or P respectively. This cell is a multifunctional device which gives different Boolean function with three inputs G, P and N [10]. It improves design complexity, transistor count, swing level of logic and static power dissipation but it requires twin well CMOS process.

3.5.1 GDI XOR Full Adder

This adder cell uses 10 transistors. It uses two GDI XOR gates and a multiplexer. It consumes less power, less internal capacitance and less area. There is very less static power loss so power loss is dynamic power loss. But it is more expensive.

3.5.2 GDI XNOR Full Adder

This adder cell uses 10 transistors. It uses two GDI XNOR gates and a multiplexer. It consumes less power, less internal capacitance and less area. There is very less static power loss so power loss is dynamic power loss. But it is more expensive.

4. DIFFERENT ADDER CIRCUITS AND THEIR COMPARISON

Different full adder circuits are given here and simulated using cadence tool. The simulation is carried out in 180 nm

CMOS process technology at 1.8V V_{dd} . The comparison of various full adders is done using different parameters like average power dissipation, delay, PDP and number of transistors used and simulation results of adders discussed above are given in the table 1.

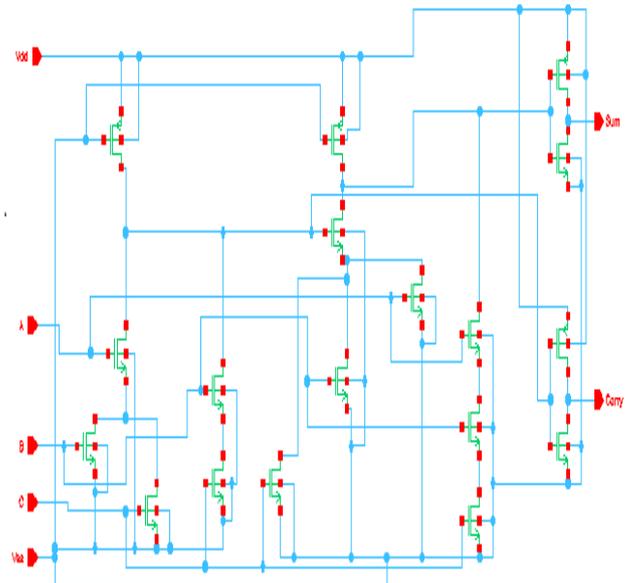


Fig 1 Pseudo nMOS Full Adder [4]

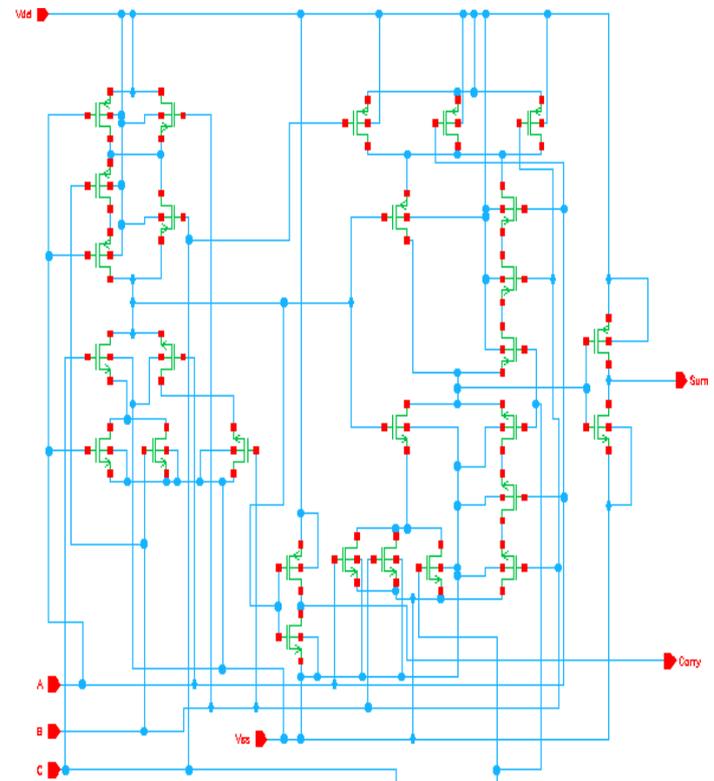


Fig 2 C-CMOS Full Adder [7]

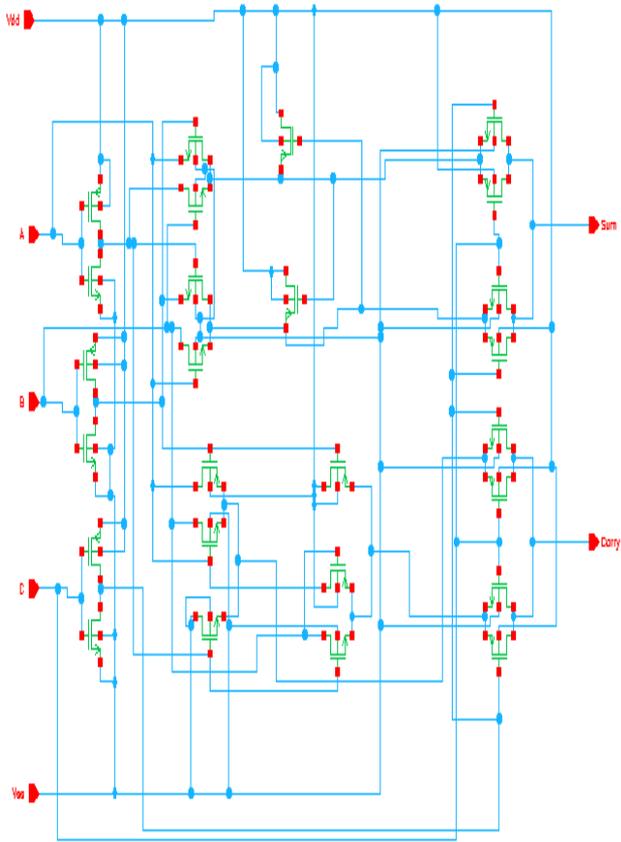


Fig 3 CPL Full Adder [1]

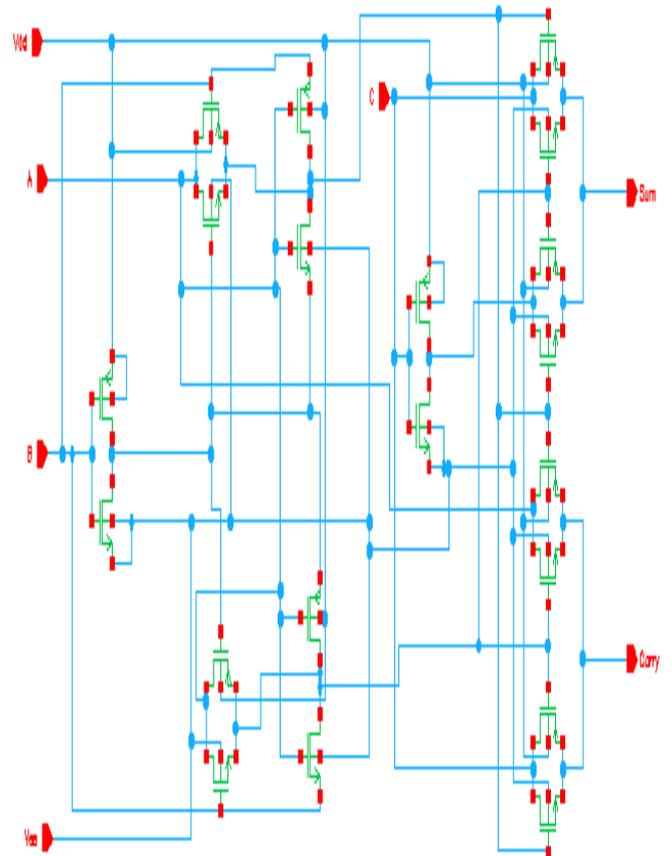


Fig 5 TGA Full Adder [5]

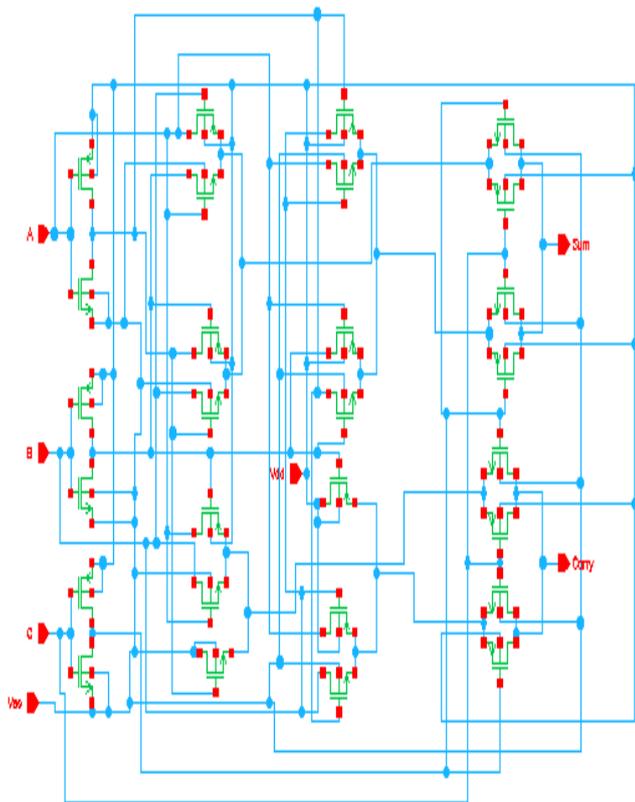


Fig 4 DPL Full Adder [1]

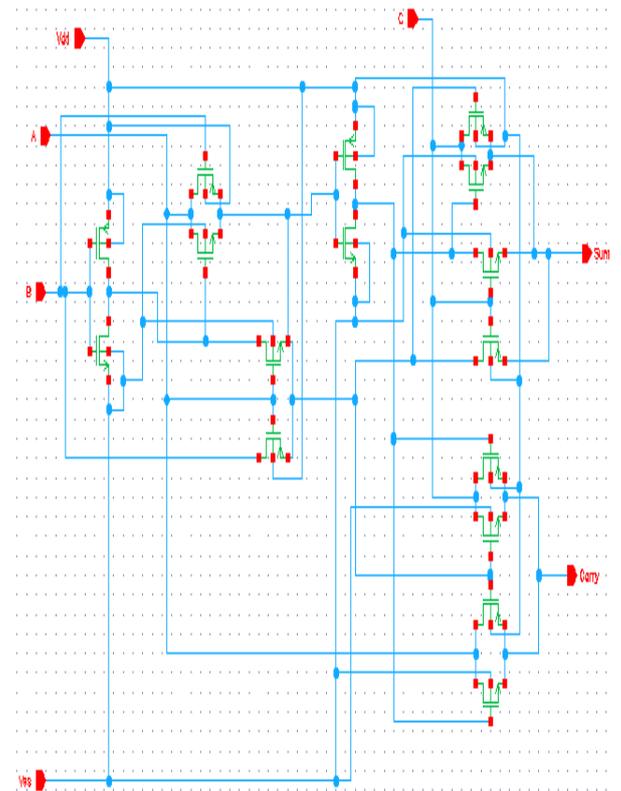


Fig 6 TFA Full Adder [2]

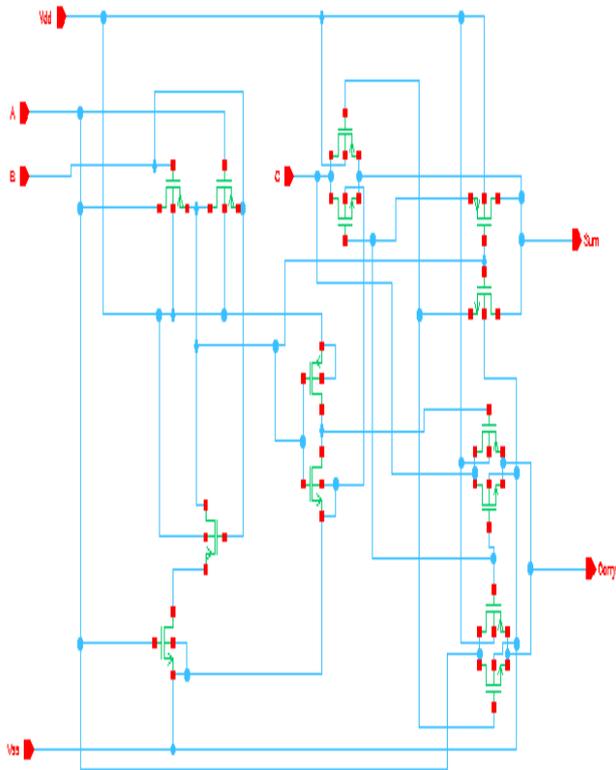


Fig 7 TGA XNOR Full Adder [4]

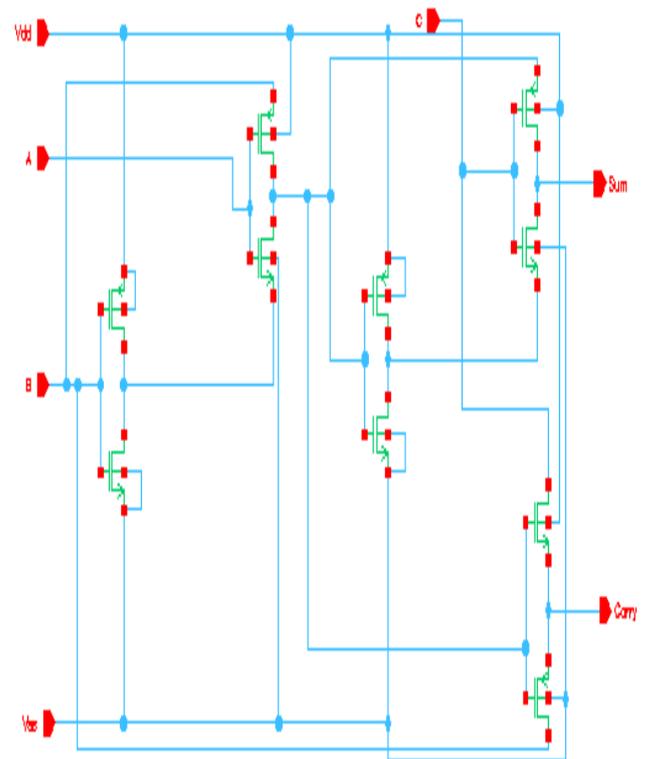


Fig 9 GDI XOR Full Adder [9]

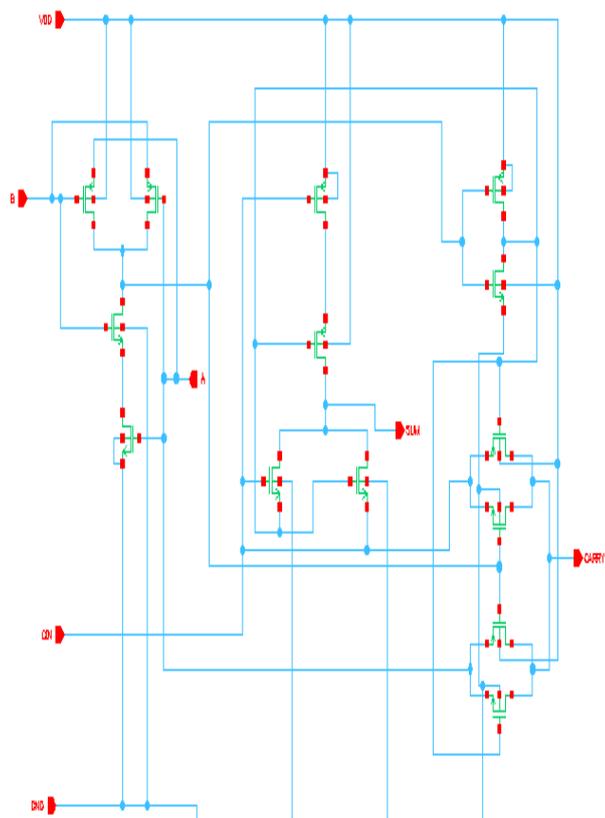


Fig 8 14T Full Adder using TG logic [2]

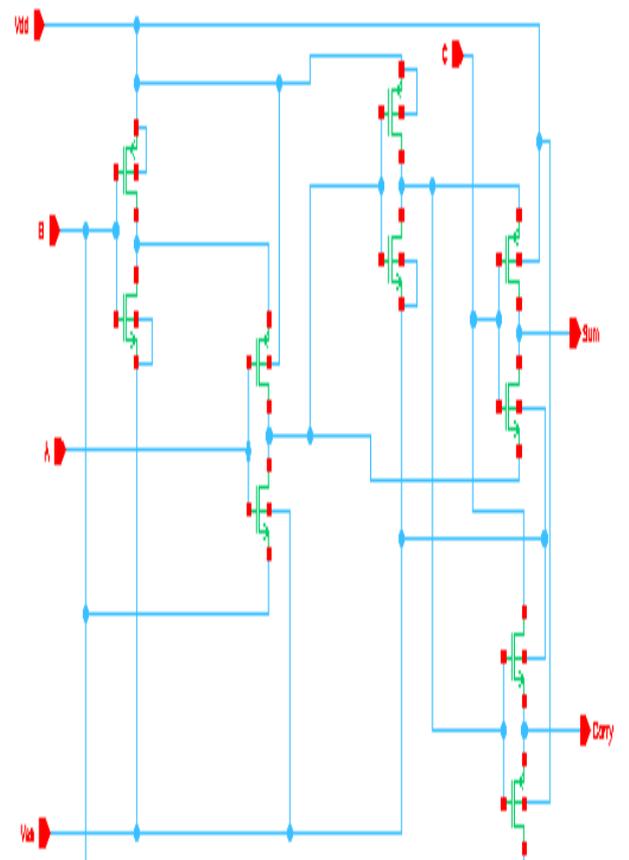


Fig 10 GDI XNOR Full Adder [9]

Table-1 Simulation Result of Various Full Adder Cell at V_{dd}=1V, Delay (ps), Avg Power (μ w), PDP (e-15 Js) Using 180 nm CMOS Process Technology.

S.No.	Cell Name	Delay	Avg Power	PDP	Transistors
1	CCMOS	0.195	0.345	0.067	28
2	Pseudo nmos	0.182	0.297	0.054	18
3	CPL	0.089	0.367	0.032	32
4	DPL	0.167	0.361	0.06	28
5	TGCMOS	0.135	0.305	0.041	20
6	TFA	0.353	0.044	0.015	16
7	14TNEW	0.548	0.049	0.026	14
8	TGXOR	0.125	0.103	0.012	14
9	GDXOR	0.161	1.384	0.223	10
10	GDXNOR	0.266	0.055	0.014	10

5. CONCLUSIONS

The performance of various full adders given in Table-1 shows that different adders have different parameter values no single adder have less delay, power and PDP. So there is a trade off between these parameters. The results help us to choose an adder which can give us desired result according to a specific application.

REFERENCES

- [1] Mariano Aguirre-Hernandez and Monico Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications," in *Proc. IEEE VLSI SYSTEMS*, 4, April 2011, vol. 19, pp. 718-721.
- [2] A. M. Shams, T. K. Darwish, and M. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 1, pp. 20-29, Feb. 2002.
- [3] S. Goel, A. Kumar, and M. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1309-1320, Dec. 2006.
- [4] Amir Ali Khatibzadeh, Kaamran Raahemifar, "A study and comparison of full adder cells based on the standard CMOS logic," *IEEE Trans. CCECE, Niagara Falls*, May 2004 0-7803-8253, pp. 2139-2142
- [5] Ming-Bo Lin, "Introduction to VLSI systems A logic, circuit and system perspective," Taylor & Francis group, ch. 7
- [6] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *IEEE Proc. Circuits Devices Syst.*, vol. 148, no. 1, pp. 19-24, Feb. 2001.
- [7] S. Wairya, Himanshu Pandey, R. K. Nagaria and S. Tiwari, *Member, IEEE*, "Ultra Low Voltage High Speed 1-Bit CMOS Adder," 978-1-4244-8542-0/10/2010 IEEE
- [8] Uming KO, Poras T. Balsara, and Wai Lee, "Low-Power Design Techniques for High-Performance CMOS Adders," *IEEE Trans VLSI Systems*, vol-3, No. 2, pp. 327-332, June, 1995.

BIOGRAPHIE



Manisha, is presently pursuing her M. Tech. studies in the Department of Electronics and Communication Engg. Deen Bandhu Chhotu Ram University of Science and Technology, Murthal, Sonapat, Haryana. She received her B.tech. Degree in Electronics & Communication Engineering from Bhagwan Parshuram College Of Engineering, Gohana, Sonapat, Haryana in 2010. Her area of interest is CMOS, VLSI Technology.