LOW POWER SRAM CELL WITH IMPROVED RESPONSE

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Abstract

In SRAM memory cells power dissipation through standby leakage and dynamic loss is a major problem especially in low power fabrication with modern technology scaling and for high temperature operations. This paper is based on low power operation and delay of SRAM cell. Paper presents a novel technique to reduce dynamic power loss during switching activity. The modified SRAM cells with proposed technique are compared with their basic SRAM cells on CADENCE VIRTUOSO on 90nm technology scale. The average power of SRAM cells decreases and the write delay is also slightly improves compared to their parent architecture at the mentioned scale.

Keywords: *Dynamic power loss, leakage current, Power consumption, Standby current, Write delay.*

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1. INTRODUCTION

On chip memory circuits have become very popular system in many VLSI circuits, specially system on chip (SOC), and range of single chip memory has reached terabyte. But with the increase of size and interconnections between the cells in the circuits, power consumption and delay also increases which restricts the size of memory cells and its packaging [1]. On low power VLSI lots of research has been done to reduce power consumption but generally degrade response time. In this paper we have introduced new technique, which can be applied to all SRAM architecture and reduces power consumption and improve write delay.

The power consumption of the system on chip having SRAMs increases largely with technology scaling because at low scale gate leakage current, sub-threshold current [2][3], tunneling [6] plays a significant role in the SRAM operation. The modified SRAM cells with proposed technique shows better performance with reduced power consumption against conventional SRAM cells. All the comparison is done on CADENCE VIRTUOSO at 90nm technology scale.

2. BASIC SRAM ARCHITECTURE

The basic SRAM cell design used bi-stable latching circuitry to store each bit. The two bi-stable states are 0 and 1, which are stored in cross coupled inverters. Both inverters have opposite values. The basic SRAM cell structure and the two stable states of the inverters are shown in fig-1(a) and 1(b) respectively. 6T SRAM cell is considers as the basic cell architecture, other kinds of SRAM architectures used 4, 8, 9, 10T or even more transistors to store single bit.

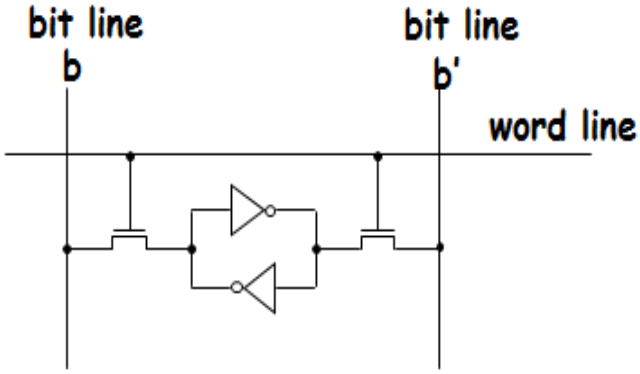

Fig-1(a): Basic SRAM structure.

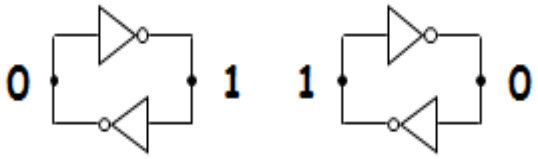

Fig-1(b): The two stable states of cross coupled inverters in SRAM cell.

3. 6T SRAM CELL

The architecture of 6T SRAM basic cell is considered and shown in fig-2. The 6T SRAM cell is made by using six MOSFETS (two PMOS and four NMOS). Four MOSFETS (P1, P2 N1 and N2) are used in cross coupled inverters and rest two MOSFETS are used as pass transistors.

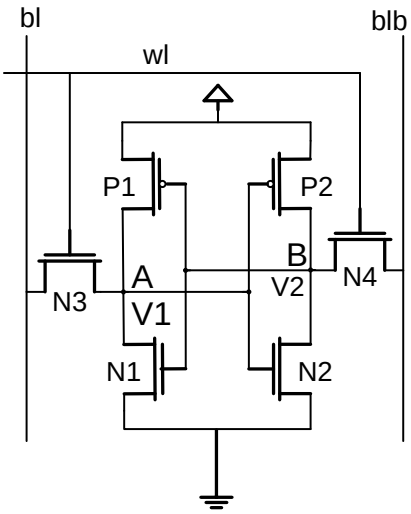

Fig-2: Basic 6T SRAM architecture.

1.1 Write Operation

Data to be written into the cell is applied to the bit lines (bl and blb). The access transistors (N3 and N4) are enabled by applying word line signal WL equal to'1' to the gates. When proper voltages are applied at bit lines and word line is enabled the node will get the value from the bit line. It is very essential that for easy write operation the W/L ratio of the pull up device to that of access transistor should be small [1],[5].

1.2 Read Operation

During read operation The Bit lines of the cell are pre-charged. The access transistors are enabled by applying word line signal WL equal to '1' to the gates of them. This results in the current flow from the bit line to low storage node of the cell and therefore a voltage drop is created on this bit line which is sensed and amplified by the sense amplifier to read the contents of the cell. For the easy read operation RSNM of at least 25% of VDD is generally considered to have excellent read stability [4] and the W/L ratio of the pull down N transistor to that of access transistor should be large enough. Which mean the standard 6T cell is sized to maintain pull-up (PU) devices <pass-gate (PG) devices<pull-down (PD) [1],[5].

4. POWER DISSIPATION IN SRAM

Power is necessary for the proper functioning of an active memory latch: if the cell is to be overwritten during a write cycle, the capacitive loads at nodes A and B each have to either be charged or discharged. However, there are wasteful sources of dynamic power consumption that result from short circuits that exist when the memory cell is switching. There are three different short circuits VDD-to-Zero, One-to-GND, and Short-VDD-GND, displayed in Fig-3 using line, dotted line and hashed line respectively. Other forms of wasteful power dissipation occur when the SRAM is inactive. These static power losses include sub-threshold conduction, junction leakage, and gate tunneling. Leakage current and its consequences will not be analyzed in this thesis. Instead, dynamic power and delay are the main focal points.

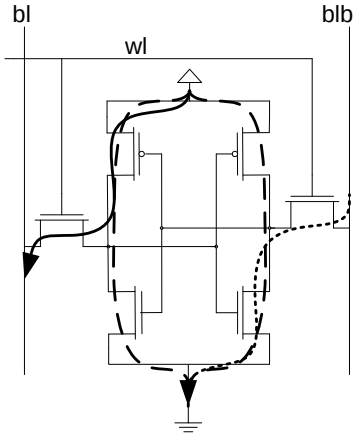

Fig-3: Dynamic power dissipation due to short circuit.

5. OTHER IMPORTANT SRAM ARCHITECTURE

6T SRAM is one the most popular and widely used SRAM architectures, there are several other important architecture which are very important in the memory world. Two of them are 8T and 10T SRAM architecture. 8T and 10T SRAM are shown in fig-4 and fig-5 respectively.

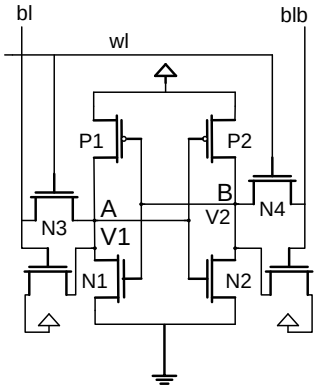

Fig-4: Basic 8T SRAM architecture.

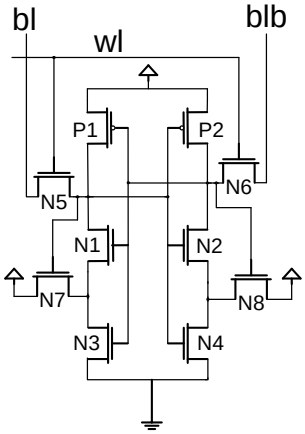

Fig-5: Basic 10T SRAM architecture.

6. PROPOSED TECHNIQUE TO REDUCE POWER CONSUMPTION AND DELAY

The proposed technique is presented in fig-6. In this novel technique two pass transistors are inserted at the two end of the SRAM cell. The idea is to break any short circuitry in the cell. In this technique a PMOS is inserted between VDD and the cell keeping its gate low and a NMOS is inserted between cell and the ground keeping its gate high.

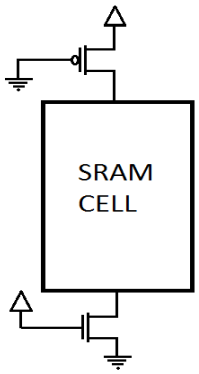

Fig-6: Proposed technique to reduce power consumption.

7. PROPOSED TECHNIQUE APPLIED ON 6T, 8T AND 10T ARCHITECTURE

The architecture of basic 6T, 8T and 10T SRAM are modified using the proposed technique. In the modified architecture the threshold voltages, W/L ratios of all the NMOS and PMOS transistors and the power supply were same as of the parent architectures and two pass transistors are inserted at the two end of the SRAM cell as per the proposed technique. The architectures of modified 6T, 8T and 10T cells are shown in fig-7, fig-8, and in fig-9 respectively.

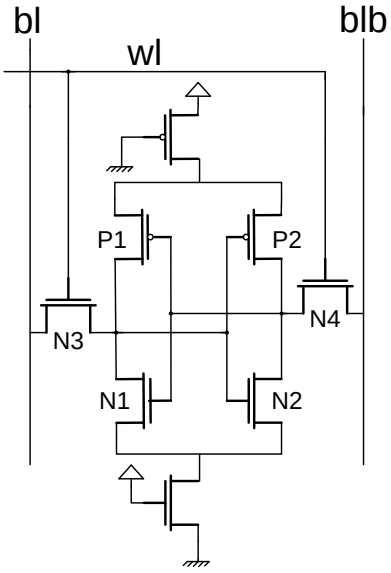

Fig-7: Proposed technique applied on 6T SRAM.

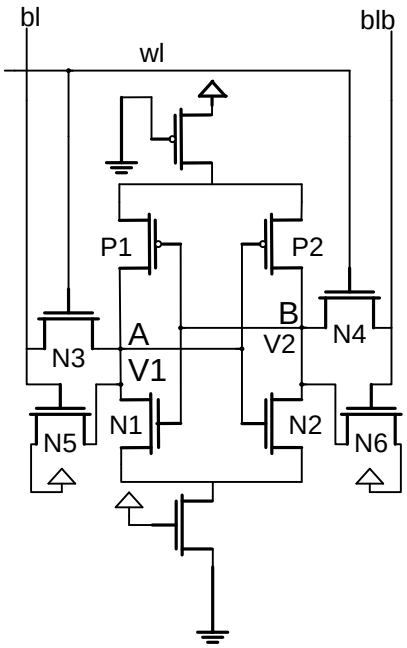

Fig-8: Proposed technique applied on 8T SRAM.

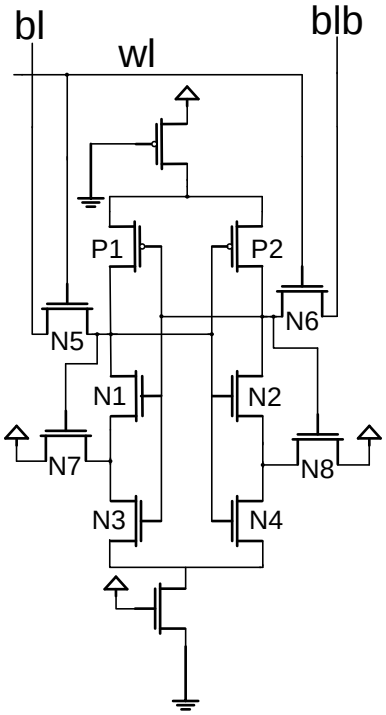

Fig-9: 10T SRAM cell with proposed technique

8. SIMULATION RESULT

The proposed and conventional 6T, 8T and 10T SRAM cells are simulated on CADENCE VIRTUOSO and all the measurement are done for 50ns time scale. Fig-10 shows the simulation result for conventional basic 6T SRAM. In the simulation results the horizontal axis represents the timing in nano-seconds and the vertical axis represents the voltage level in volts. Improvements have been seen in write delay and power dissipation, were quite significant.

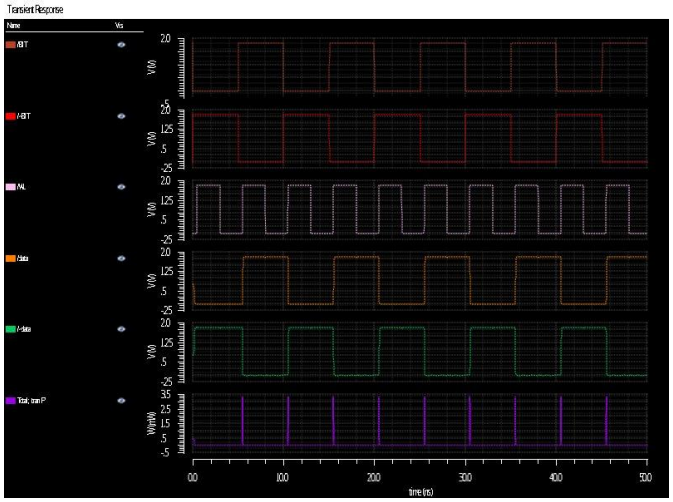

Fig-10: Simulation result for parent 6T SRAM cell.

Fig11(a) and Fig-11(b) shows the simulation results of 6T SRAM for parent and its modified version respectively.

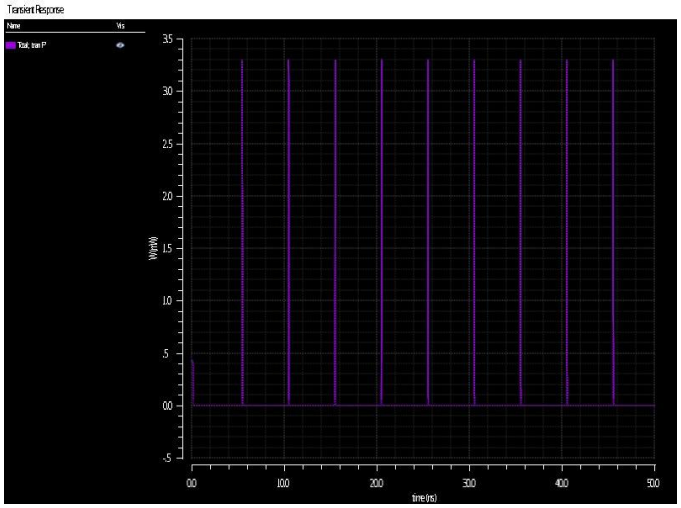

Fig-11(a)

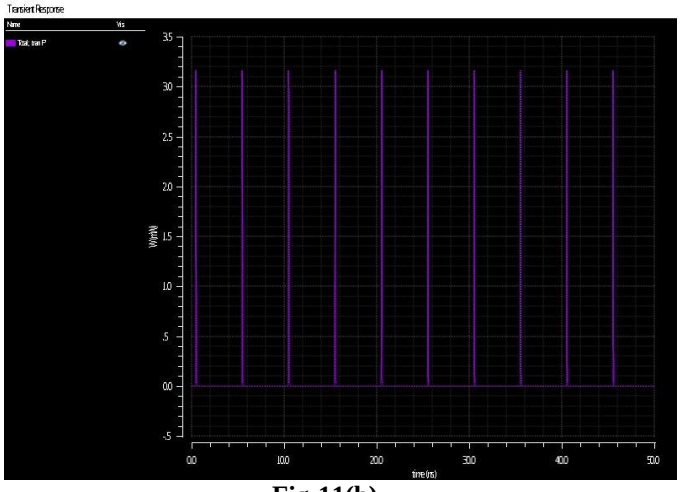

Fig-11(b)

Fig-12(a) and fig-12(b) shows the average power of 8T SRAM for parent and its modified version respectively.

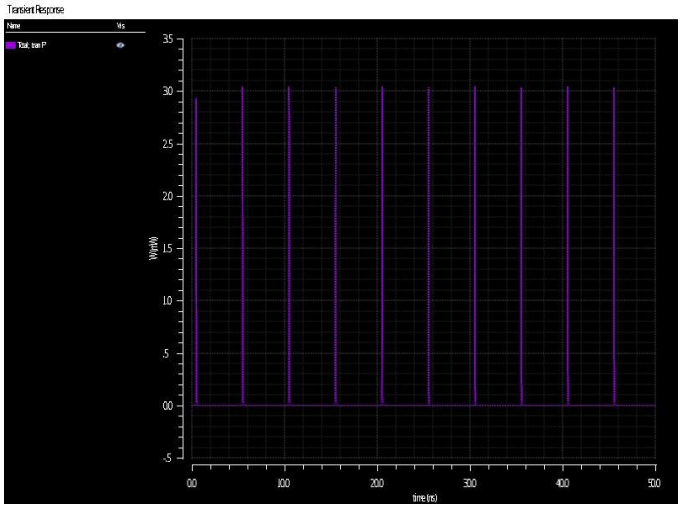

Fig-12(a)

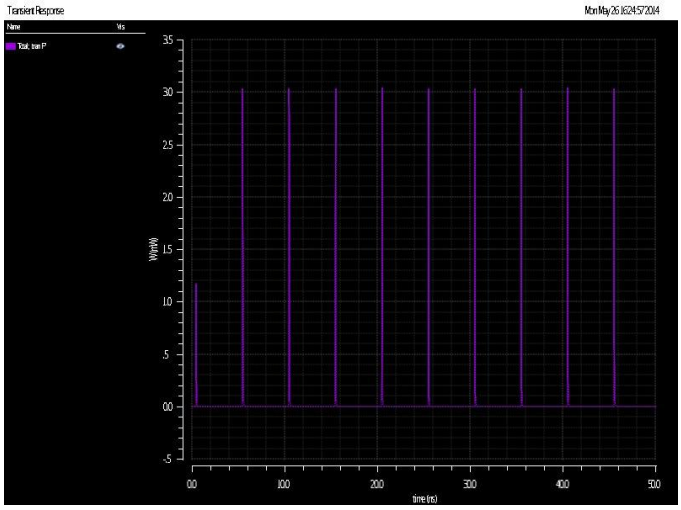

Fig-12(b)

Fig-13(a) and fig-13(b) shows the average power of 10T SRAM for parent and its modified version respectively.

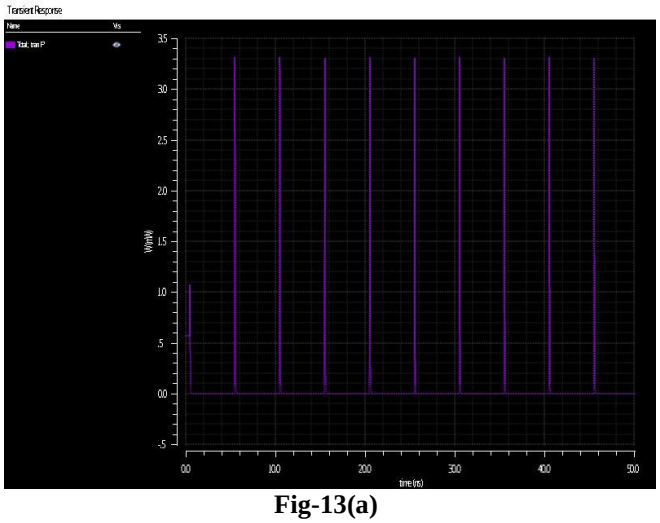

Fig-13(a)

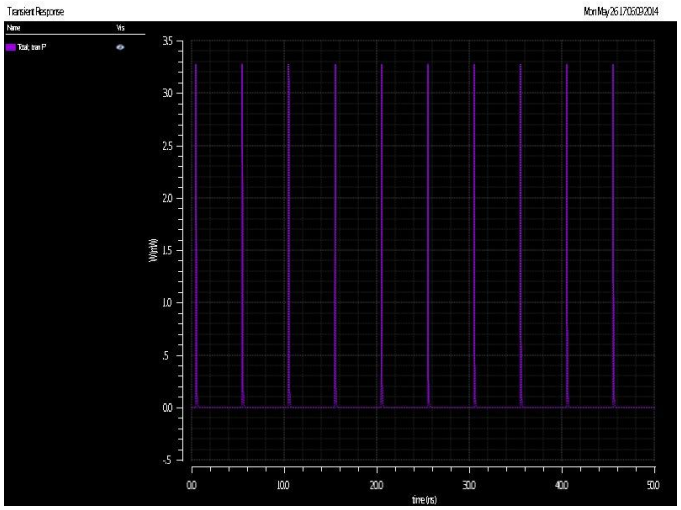

Fig-13(b)

9. PERFORMANCE ANALYSIS

The results obtained from the simulation has been analyzed and it is found that power consumption and write delay of the modified SRAM architectures is better than its parent SRAM architecture. The comparison between the parent and the modified architectures are shown in table-1.

Table -1: Performance parameter of basic SRAM architecture and its modified version (as per the proposed technique)

S.No	SRAM Arch.	Write Delay (in ps)	Power consumption (in µW)
1	6T	37.67	9.89
2	Modified 6T	31.47	8.19
3	8T	31.17	8.69
4	Modified 8T	28.60	6.83
5	10T	21.88	16.72
6	Modified 10T	13.98	15.51

10. CONCLUSIONS

This paper proposes a novel technique for reducing power consumption and write delay than conventional SRAM cells. The proposed novel technique is then applied to three different SRAM architectures. The comparisons of simulated results for all cases are shown in table-1. In 6T modified architecture power consumption and write delay are improved by 12% and 16% respectively and these in 8T modified architecture are improved by 7% and 8% respectively and in 10T modified architecture improved by 18% and 36% respectively.

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BIOGRAPHIES

Anant Anand Singh received the B.Tech. degree in electronics and communication engineering from Madan Mohan Malaviya Engineering College, Gorakhpur, India (now converted to autonomous university and known as MMMTU), in 201. He is currently working toward the M.Tech degree in the field of very large scale integrated (VLSI) design and embedded system with the Department of Electronics Engineering, National Institute of Technology, Jamshedpur, India.

Arvind Choubey received the Bachelor & M.Tech degree in Electrical Engineering from Bihar University and IIT- BHU, Varanasi in 1984 & 1987 respectively. He received PhD degree in signal processing and digital communication from Ranchi University, Jharkhand, India, in 2009. He joined as the Assistant Professor in National Institute of Technology (NIT), Jamshedpur, India, in 1987 & become Associate Professor in 1997. Presently, he has been working as a Professor in the Dept. of ECE at NIT Jamshedpur since 2009. He honored the chair of Head of the ECE department during tenure from Dec' 2000 to Jan'2005 and from June 2011 to May 2013. His present research interests are Digital Signal Processing, Digital Communication, Antenna Design,

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