A NOVEL APPROACH TO EXTEND STANDBY BATTERY LIFE FOR MOBILE DEVICES

Tejas H[1], B S Renuka[2], Vikas Mishra[3]

[1]*Industrial Electronics, SJCE, Mysore*
[2]*Department of Electronics and Communication, SJCE, Mysore*
[3]*Mobile Communication Group, Intel Technology India Ltd, Bangalore*

Abstract

Mobile devices are an essential need for most of us in this modern world. Current generation of mobile devices, such as smartphones and tablets are equipped with high speed multi core processors with advanced features to uplift the user experience. However, advances in battery technology continue to lag with the advancement of mobile technology, especially for the compact form-factor devices. Cutting down energy consumption is one of the most crucial design factors for a mobile device.

This paper will emphasize on a new power optimization technique and focus on the expected power saving by theoretical calculations. Analysis of the actual power saving by experimenting on a reference tablet platform and highlight the results of power saving achieved by optimization on the reference tablet.

Keywords: *Standby, battery life, tablets, phones, power delivery*

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1. INTRODUCTION

Mobile devices have become a popular platform for both personal and commercial applications. The increased use of these devices has in turn emphasized the demand for maximizing their battery lifetime, making power efficiency a critical design goal. Indeed, in order to enable these devices for end users, it is often necessary to employ software techniques in addition to hardware optimizations to achieve the battery lifetimes required by end users.

Despite of operating system's ability for power saving by switching to low-power states [1], it is analyzed that there is a scope for power optimization in standby state of mobile devices. As the handheld devices has greater residency in standby state [2], optimizing power consumption in this state will have a significant impact on the battery life. This paper concentrates on optimizing power in standby state by reducing the voltage or turning off partially functioning/ not functioning components in standby to save power.

Currently 'Dynamic voltage scaling' (DVS) technique [3] is used in mobile device to optimize the power. DVS scales the operating voltage of the component depending on the system requirement. This is possible because of static CMOS logic that is used in the vast majority of microprocessors. Today processors have a frequency-dependent maximum operating voltage. When used at a reduced frequency, the processor can operate at a lower supply voltage. Since the energy dissipated per cycle with CMOS circuitry scales down by four folds to the supply voltage. DVS has potentially provided a very large net energy savings through voltage scaling (Dynamic voltage scaling) and by transitioning components into low-power states (dynamic power management).

2. STANDBY POWER OPTIMIZATION OPPORTUNITY

Battery backup of the mobile device depends on the power consumption of all the components on the platform. To increase the battery backup the power consumption of the platform should be reduced. Currently there are various method's used to bring down the power consumption [4] [5]. This paper draws attention about a new approach to reduce the power consumption on the mobile platform.

Figure1 explains how battery supplies power to various components on the reference platform.

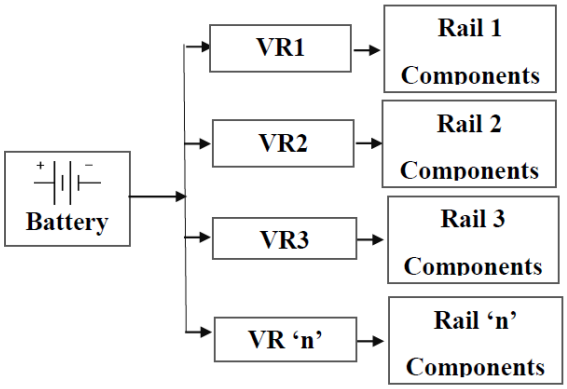

Figure 1: Indicative power supply tree

From Figure1 we observe that various voltage regulators (VR) draw power from the battery and supply to various rails/components on the reference device. The total power consumption by the device or the total power drawn from the

battery would be the sum of power consumed by individual VR's that is

$$P_{Platform}=P_{VR1}+P_{VR2}+P_{VR3}+P_{VRn} \quad (1)$$

Where, $P_{Platform}$ = power consumed by platform and P_{VR1}, P_{VR2}, P_{VR3}, P_{VRn}= power consumed by respective VR's

Now, let's look at one of the rail to understand the power consumption by individual rail/component in the platform, Figure 2 illustrates Battery supplying power to a rail that is regulated by a Buck converter and in turn supply to the load.

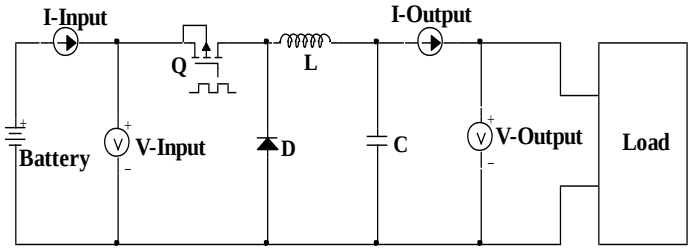

Figure 2: Example of battery supplying the load through a VR

Power consumption by the rail considered is given by

$$P_{VR} = \text{V-Input} * \text{I-Input} \quad (2)$$

Where, V-Input = battery voltage and I-Input = current consumed by the VR.

Now, battery backup can be increased by reducing P_{VR}. As the input voltage is fixed (battery voltage) the only way to reduce P_{VR} is by reducing I-Input.

But, I-Input depends on the power consumed by the load component

So,

$$P_{Out} = \text{V-Output} * \text{I-Output} \quad (3)$$

Where, V-Output = voltage at the load and I-Output = current consumed by the load component.

During standby state when the modules are switched to low power sleep mode, the current to the component is decreased to minimum value. So, I-Out during standby state is already reduced to minimum value by the operating system. This can be inferred as P_{out} totally depends on V-Output during standby.

$$P_{out} \alpha \text{ V-Output} \quad (4)$$

Hence, during standby I-Input can be reduced by reducing V-Output in order to save power (reduce P_{VR}). As leakage current reduces with reduction in voltage [6], reducing V-Out would further reduce the current (I-Output) proportionally. This further adds to the platform power saving $P_{Platform}$.

So far only one rail was considered. The proposed method of reducing V-Output can be applied to all other rails that are 'ON' during standby state to achieve more power saving.

The Operating System dynamically reduces the rail voltage during standby and restores back the voltage to default value on standby exit. Figure 3 explains the flow of the proposed optimization at a system level.

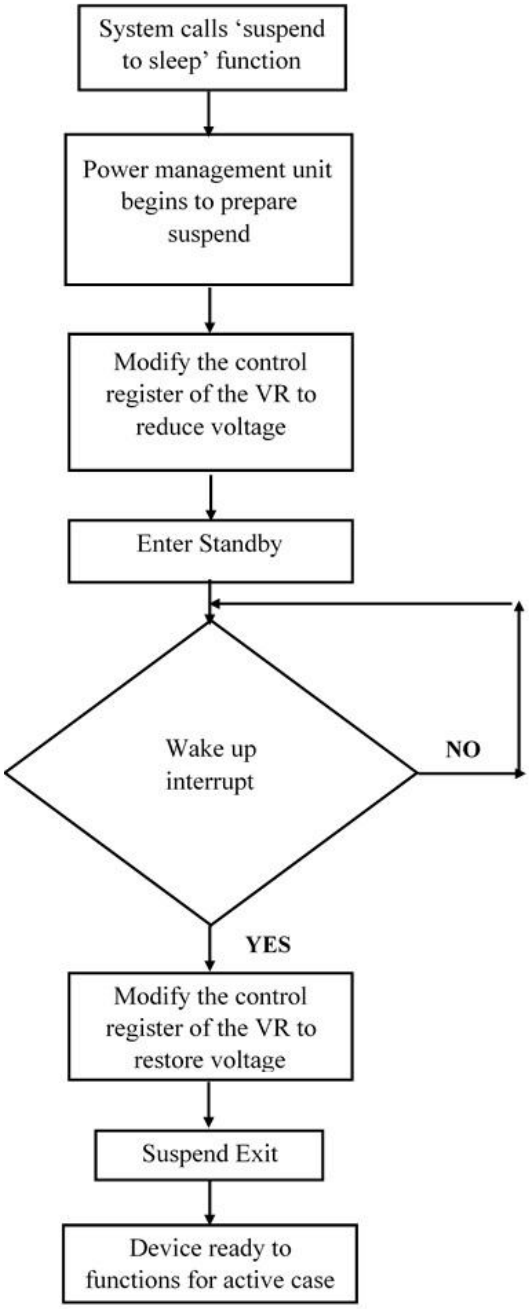

Figure 3: Flow chart of system flow to standby state

3. EXPECTATION ON A REFERENCE PLATFORM

Before reducing the rail voltage and identifying the rails to be optimized .A good understanding of the components on the rail and their behavior in various power states is required.

Here, we try to identify few rails in standby mode and optimize the power consumption.

Firstly, let's understand the power map of a reference tablet during standby mode. Figure 4 is an indicative power map of a tablet during standby state [7].

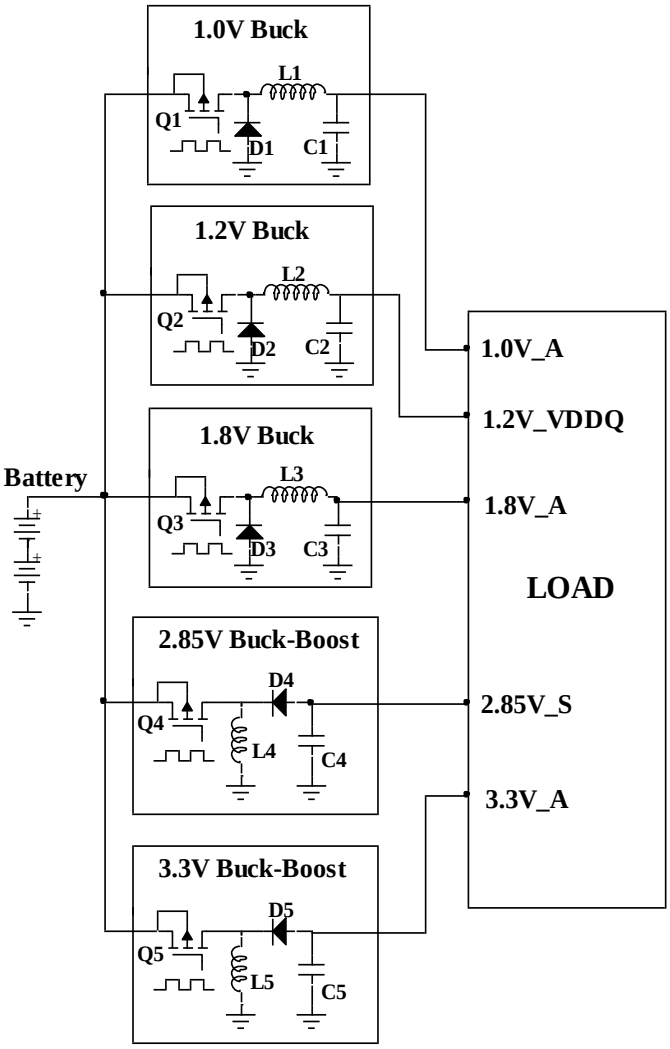

Figure 4: Reference Tablet Power Map in Standby State

From the above power map it is observed that, there is better scope in optimizing the power consumed by 1.2V_VDDQ, 1.8V_A, 3.3V_A rails in standby state. For experiment let's take up these rails to optimize the power consumption.

Let's discuss the percentage of voltage that can be reduced and the expected power saving on each of the above mentioned rail.

3.1 Optimizing 1.2V_VDDQ Power Rail

Major component on 1.2V_VDDQ rail is LPDDR3 (RAM), with rail voltage of 1.2V. In order to save power in standby state, the voltage of this rail is reduced to the V_{min} allowable by the RAM, i.e. 10% lower. Hence, during standby mode the voltage can be reduced by 10% that is 1.08V.

Default power consumption by 1.2V_VDDQ rail before optimization is given by

$$P_{1.2V\_VDDQ} = V_{1.2V\_VDDQ} * I_{1.2V\_VDDQ} \quad (5)$$

Where $V_{1.2V\_VDDQ}$ = Default operating voltage $I_{1.2V\_VDDQ}$ = current in this rail at Default voltage.

Expected Power Saving

Operating voltage of this rail is 1.26V and reducing this voltage to 1.080V would be 14.28% reduction in the voltage, this would reduce the current proportionally.

So Power consumption by 1.2V_VDDQ rail operating at 1.080V assuming current is reduced by 10% is

$$P_{1.2V\_VDDQ\,@1.080V} = V_{85.7\% *} I_{90\%.} \quad (6)$$

Figure 5 shows the trend of power consumption with various voltages.

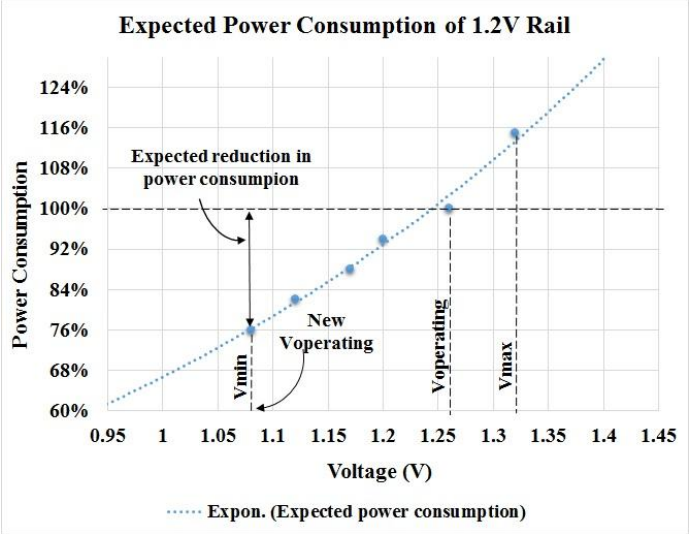

Figure 5: Expected power consumption trend of 1.2V

Power saving expected is P_{saving} = $P1.2V_{\_VDDQ}$ - $P_{1.2V\_VDDQ\,@1.080V}$ ≈ 24% of P1.2V_VDDQ.

3.2 Optimizing 1.8V_A Power Rail

This rail is the source of self-refresh voltage to Emmc (flash memory) with default voltage of 1.80V. To save power in standby mode, this rail voltage can be reduced by 10%. As per the flash memory self-refresh, the tolerable minimum voltage is 1.620V.

Default Power consumption by 1.8V_A rail before optimization is given by

$$P_{1.8V\_A} = V_{1.8V\_A} * I_{1.8V\_A} \quad (7)$$

Where $V_{1.8V\_A}$ = Default voltage, $I_{1.8V\_A}$ = Current in this rail at default voltage.

Expected Power Saving

Operating voltage of this rail is 1.86V and reducing this voltage to 1.620V would be 14.28% reduction in the voltage. This would reduce the current proportionally.

So Power consumption by 1.2V_VDDQ rail operating at 1.080V, assuming current is reduced by 10% is

$$P_{1.8V\_A\ @1.620V} = V_{85.7\%} * I_{90\%.} \quad (8)$$

Figure 6 shows the trend of power consumption with various voltages.

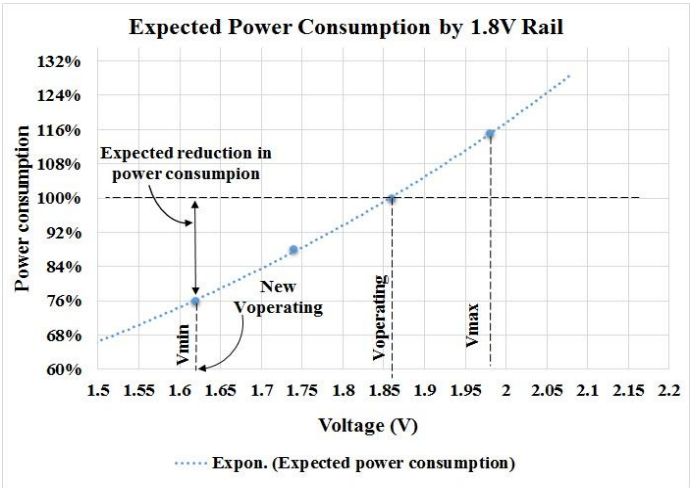

Figure 6: Expected power consumption trend of 1.8V rail

Power saving expected is $P_{saving} = P_{1.8V\_A} - P_{1.8V\_A\ @1.620V} \approx$ 24% of $P_{1.8V\_A.}$

3.3 Optimizing 3.3V_A Power Rail

This rail supplies various modules in the platform and it has a default voltage of 3.3V. Many sub rails are derived from 3.3V_A; various modules on this rail can tolerate ±5. Hence, to save power during standby the voltage can be reduced by 5% (V_{min}) that is 3.135V.

Default Power consumption by 3.3V_A rail before optimization is given by

$$P_{3.3V\_A} = V_{3.3V\_A} * I_{3.3V\_A} \quad (9)$$

Where $V_{3.3V\_A}$ = Default voltage, $I_{3.3V\_A}$ = Current in this rail at Default voltage.

Expected Power Saving

Operating voltage of this rail is 3.33V and reducing this voltage to 3.135V would be 6% reduction in the voltage. This would reduce the current proportionally.

So Power consumption by 1.2V_VDDQ rail operating at 1.080V assuming current reduced by 5%

$$P_{3.3V\_A\ @3.315V} = V_{94\%} * I_{95\%.} \quad (10)$$

Figure 7 shows the trend of power consumption with various voltages.

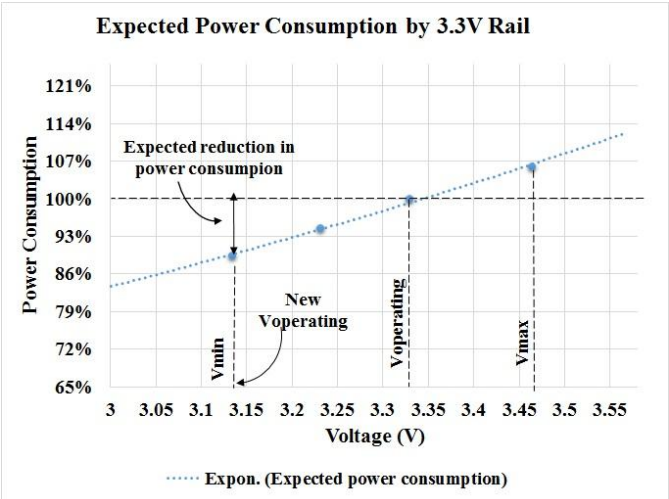

Figure 7: Expected power consumption trend of 3.3V rail

Power saving expected is $P_{saving} = P_{3.3V\_A} - P3.3_{V\_A\ @1.620V} \approx$ 11% of $P_{3.3V\_A}$

3.4 Impact on VR Efficiency

The operating system dynamically modulates the rail voltage by controlling the voltage regulator; this may impact the efficiency of the voltage regulator. The impact on the VR efficiency [8] due to optimization is monitored during actual experiment on the reference platform.

4. RESULTS AND ANALYSIS

To know the actual reduction in power consumption by the proposed method of optimization, the above mentioned rails was subjected to optimization on a reference platform by modifying the voltage regulator control settings to modulate the voltage during stand by state. Following section will summarize the comparison between the expected power saving and actual power saving achieved.

4.1 1.2V_VDDQ Power Rail

Figure 8 gives a comparison between the theoretical expected power saving with the actual power saving on a reference platform for 1.2V_VDDQ rail

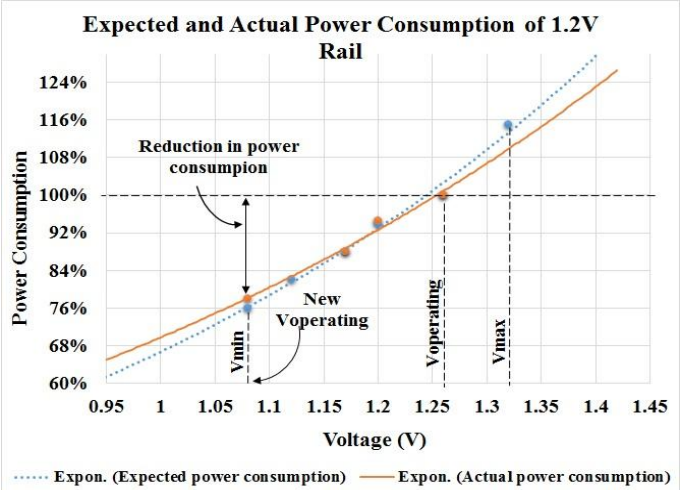

Figure 8: power consumption trend of 1.2V rail

From figure 8 we can observe that expected reduction in power consumption was around 24% but due to the VR efficiency and increase in the leakage losses the actual power saving observed is around 22% by reducing the voltage to $V_{min.}$

4.2 1.8V_A Power Rail

Figure 9 gives a comparison between the theoretical expected power saving and the actual power saving on a reference platform for 1.8V_A rail

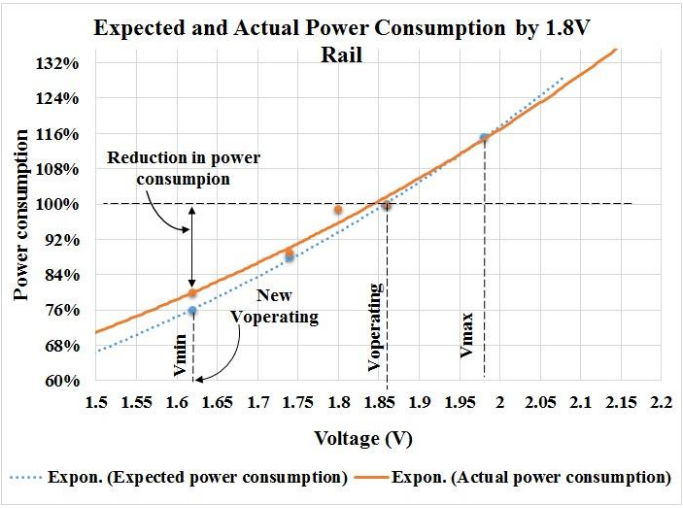

Figure 9: Actual and Expected power consumption trend of 1.8V rail

From figure 9 we can observe that expected reduction in power consumption was around 24% but due to the VR efficiency and increase in the leakage losses the actual power saving observed is around 20% by reducing the voltage to V_{min}.

4.3 3.3V_A Power Rail

Figure 10 gives a comparison between the theoretical expected power saving and the actual power saving on a reference platform for 3.3V_A rail

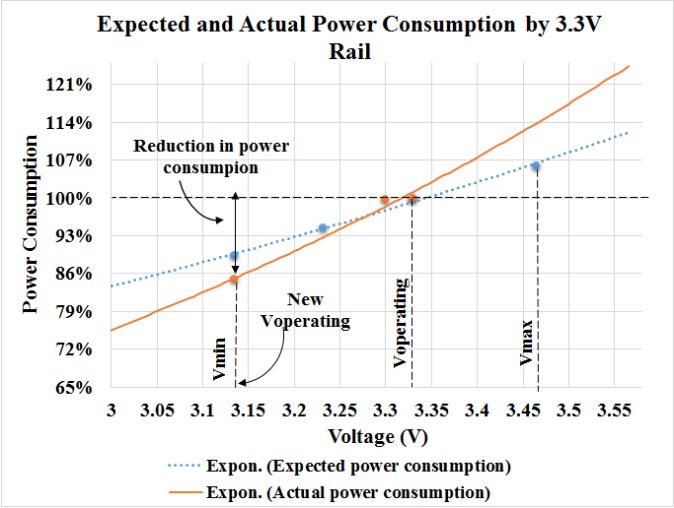

Figure 10: Actual and Expected power consumption trend of 1.2V rail

From figure 10 we can observe that expected reduction in power consumption was 11%, due to increase in the efficiency of FET switch supplying the sub rail 3.3V_S. the actual power saving observed is around 15% by reducing the voltage to $V_{min.}$

4.4 Impact on Platform Power Consumption

Due to Dynamic modulation of voltage the impact on VR efficiency in turn impacts on the platform power consumption. So VR efficiency is monitored before and after optimization, table 1 will summarize the VR efficiency due to optimization.

Table 1: Impact on efficiency by optimization

Rail Name	Before optimization	After optimization
1.2V_VDDQ	80%	80%
1.8V_A	79%	78.6%
3.3V_A	54%	56%

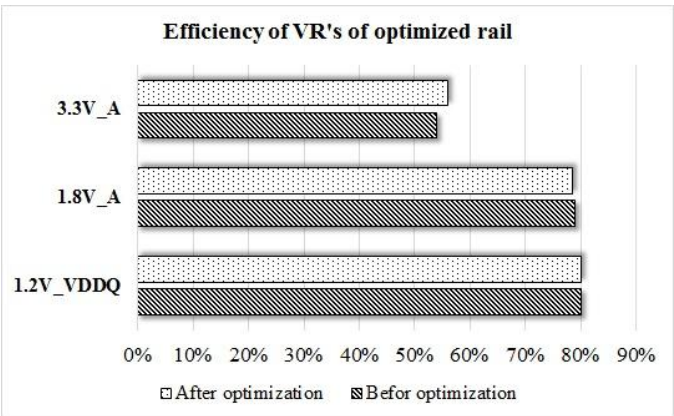

Figure 11: Impact of optimization on VR efficiency

The power saving achieved by optimization of individual rail and the impact of VR efficiency will sum up to reduce the

overall platform power consumption. The overall platform power saving achieved can be presented as:

$$P_{Total\_saving} = P_{Default} - P_{Optimized} \quad (11)$$

Where, $P_{Default}$ = Total platform power consumption before optimization and $P_{Optimized}$ = Total platform power consumption after optimization

It is observed that total power saving contributed by optimizing 1.2V_VDDQ, 1.8V_A and 3.3V_A rails to the overall platform (battery terminal) power consumption is around 11.5%

5. CONCULSIONS

In order to extend the standby battery life of mobile device, this paper has put forward a new method for optimizing power by reducing the voltage of the platform components during standby state. Later expected power saving has been calculated for a reference tablet platform and new power optimization method is experimented to analyze actual power savings achieved.

Based on theoretical calculations and the actual power measurements on the reference device, we can conclude that the proposed method has a significant impact on power saving during stand by state. The reference tablet considered in this paper exhibited around 11.5% of reduction in total platform power consumption during standby state.

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