

# DESIGN AND IMPLEMENTATION OF SYNCHRONOUS 4-BIT UP COUNTER USING 180NM CMOS PROCESS TECHNOLOGY

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## Abstract

In this paper design of synchronous 4-bit up counter is proposed using master-slave negative pulse-triggered D flip-flops. The master slave D flip-flop is implemented using 8 nand gates and an inverter. The counter is provided with additional synchronous clear and count enable inputs. The main objective is to optimize the layout of the synchronous 4-bit up counter in terms of area. The design is implemented using Cadence Virtuoso schematic editor and simulated using Cadence Virtuoso analog design environment at 180nm CMOS process technology. The optimized layout of the counter is designed using Cadence Virtuoso Layout Suite. The counter has transistor count of 210. The estimated power of the counter is 97.90 $\mu$ W and delay is 20.39ns.

**Keywords:** Area, Cadence, Counter, Delay, Master-slave D flip-flop, Nand gate, Power and Synchronous.

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## 1. INTRODUCTION

Counting is a fundamental function of digital circuits. A digital counter consists of a collection of flip-flops that change state (set or reset) in a prescribed sequence. The primary function of a counter is to produce a specified output pattern sequence. For this reason it is also a pattern generator [2]. This pattern sequence might correspond to the number of occurrences of an event or it might be used to control various portions of a digital system. In this latter case each pattern is associated with a distinct operation that the digital system must perform.

There are tremendous applications of a counter in the digital consumer electronics market. A counter can play a vital role in several circuits ranging from a simple display to complex microcontroller circuits. Some of the apparent applications of a counter are: frequency divider in phase-locked loops, frequency synthesizers, signal generation and processing circuits, microcontrollers, digital memories and in digital clock and timing circuits.

A counter is another example of a register [2]. As in the case of a register each of the 0-1 combinations that are stored in the collection of flip-flops that comprise the counter, that is the output pattern, is known as a state of the counter. The total number of states is called its modulus. Thus if a counter has 'm' distinct states, then it is called a modulus-m counter or mod-m counter. The order in which the states appear is referred to as its counting sequence.

The proposed synchronous 4-bit up counter is implemented using Cadence EDA tool [1]. The tool provides sophisticated features such as Cadence Virtuoso schematic editor which provides sophisticated capabilities which speed and ease the design, Cadence Virtuoso Visualization and Analysis which efficiently analyzes the performance of the

design, Cadence Virtuoso Layout Suite that speeds up the physical layout of the design and Cadence Assura Physical Verification reduces overall verification time because it incorporates a fast and intuitive debug capability integrated within the Virtuoso custom design environment. It helps to easily recognize, fix, extract and compare errors.

Several counter circuits have been proposed targeting on design accents such as power, delay and area. Among those designs synchronous counters using master-slave D flip-flops have been widely used. The paper is organized as follows: in section 2, the design of the proposed counter is presented. In section 3, the schematic and layout are presented. In section 4, the simulation results are given and discussed. The area, power and delay of the counter are estimated. Finally a conclusion will be made in the last section.

## 2. THE PROPOSED COUNTER

Synchronous counter is the most popular type of counter. It typically consists of a memory element, which is implemented using flip-flops and a combinational element, which is traditionally implemented using logic gates. Logic gates are logic circuits with one or more input terminals and one output terminal in which the output is switched between two voltage levels determined by a combination of input signals. The use of logic gates for combinational logic typically reduces the cost of components for counter circuits to an absolute minimum, so it remains a popular approach.

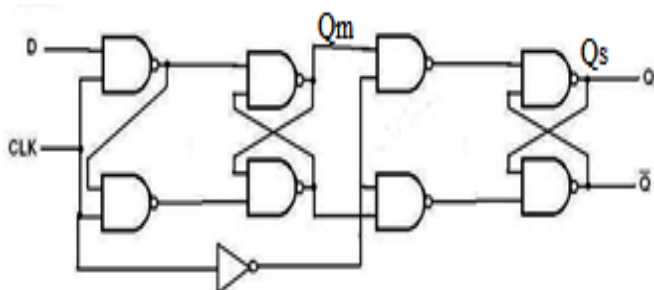
Synchronous counters have an internal clock, whereas asynchronous counters do not. As a result, all the flip-flops in a synchronous counter are driven simultaneously by a single, common clock pulse. In an asynchronous counter, the first flip-flop is driven by a pulse from an external clock and each successive flip-flop is driven by the output of the

preceding flip-flop in the sequence. This is the essential difference between synchronous and asynchronous counters. The propagation delay of synchronous counter is comparatively lower than asynchronous counter. Its performance is also better from a reliability perspective because there is no glitch.

**2.1. Master-Slave D Flip-Flop**

A master-slave D flip-flop is created by connecting two gated D latches in series and inverting the enable input to one of them. It is called master-slave because the second (slave) latch in the series only changes in response to a change in the first (master) latch [2]. The term pulse-triggered means that data is entered on the rising edge of the clock pulse, but the output does not reflect the change until the falling edge of the clock pulse. Master-slave flip-flops can be constructed to behave as a J-K, R-S, T or D flip-flop.

The purpose of master-slave flip-flops is to protect a flip-flop's output from inadvertent changes caused by glitches on the input. Master-slave flip-flops are used in applications where glitches may be prevalent on inputs. The master-slave configuration has the advantage of being pulse-triggered, making it easier to use in larger circuits, since the inputs to a flip-flop often depend on the state of its output.



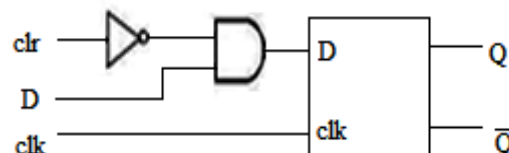
**Fig-1:** Master-slave D flip-flop

Fig.1 shows negative pulse-triggered master-slave D flip-flop. It responds on the negative edge of the enable input (usually a clock). The circuit consists of two D flip-flops connected together. When the clock is high, the D input is stored in the first latch, but the second latch cannot change state. When the clock is low, the first latch's output is stored in the second latch, but the first latch cannot change state. The result is that output can only change state when the clock makes a transition from high to low.

**Table-1:** Truth table of master-slave D flip-flop

Clk	Q <sub>n+1</sub> (next state)
0	D
1	Q <sub>n</sub> (present state)

Master changes its state when clock is high while the latter changes its state when clock is low. When the clock is high the master tracks the value of D but since the slave is in inactive state, Qs also remains unchanged. When the clock signal goes low, the master goes to inactive state and the slave which is now in active state tracks the value of Qm. While clock is low, Qm does not change its value. Thus only once during the clock cycle the slave can undergo change in its value. It can also be observed that only during the transition from high to low, the output gets change. This transition is referred to as "negative pulse-triggered" [5].



**Fig-2:** Master-slave D flip-flop with clear input

Fig.2 shows the implementation of master-slave D flip-flop with clear input. The circuit is designed using the truth table given in table.2. When the clr (clear) input goes high, irrespective of the inputs D and clock, the output goes low.

**Table-2:** Truth table of master-slave D flip-flop with clear input

Clr	Clk	Q <sub>n+1</sub> (next state)
0	0	D
0	1	Q <sub>n</sub> (present state)
1	X	0

**2.2. Synchronous 4-Bit Up Counter**

The proposed synchronous 4-bit up counter has 3 AND gates, 4 XOR gates and 4 master-slave D flip-flops. Same clock pulse is given to each flip-flop. So with every clock pulse the counter counts one step up. It is an up counter and starts from 0000. Then with clock pulse counts like 0001, 0010, 0011, 0100 up to 1111. Then it starts from 0000 again. Q0 is the LSB and Q3 is the MSB.

The master-slave D flip-flop actually works at the falling edge of the clock. But because it is a master slave configuration [8], it actually stores the input at rising edge and it is given to the output at the falling edge of the clock. So change in counter output is observed in the falling edge of the clock.

There are 2 additional inputs in the counter, count enable (CE) and clear (clr).

1. Count Enable (CE) input: If CE=0, then counter stops counting. IF CE=1, each clock pulse results in a counting action.

- Clear (clr) input: If clr=1, then the counter output clears to 0000. If clr=0, each clock pulse results in a counting action.

The control logic of the counter is as follows: The XOR gate complements each bit. The AND chain causes complement of a bit if all the bits toward LSB from it equal 1. The Count Enable forces all outputs of AND chain to 0 to “hold” the state.

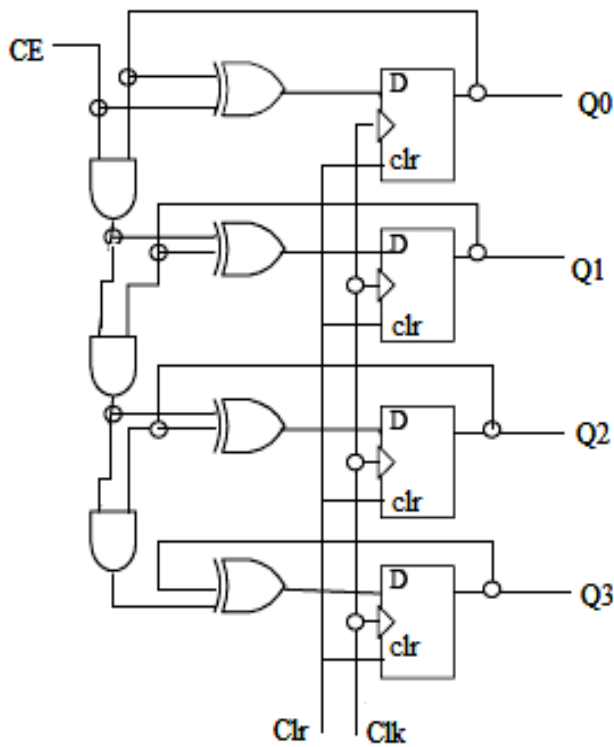


Fig-3: Synchronous 4-bit up counter

### 3. SCHEMATIC AND LAYOUT

The proposed counter is implemented in Cadence EDA tool. The transistor level diagram is implemented using Cadence Virtuoso schematic editor [1]. The optimized layout is designed using Cadence Virtuoso Layout Suite.

#### 3.1. Schematic

The implementation of the synchronous 4-bit up counter will be performed progressively by implementing and creating instances of the components of the counter independently and subsequently using all the components together to create the counter. The schematic diagram of all the components are built using PMOS and NMOS transistors with the following specifications.

Length	: 180 nm
Total width	: 2 μm
Finger width	: 2 μm
Fingers	: 1
S/D metal	: 400 nm
Threshold	: 800 nm

The schematic diagram of inverter, NAND gate, AND gate and XOR gate are as shown in fig.4.

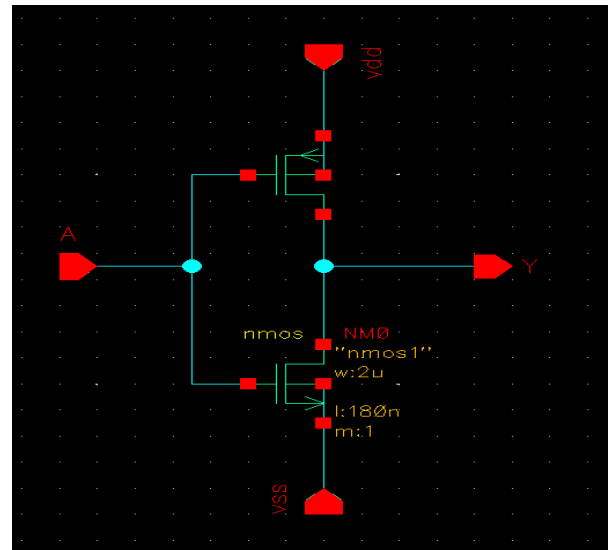


Fig-4(a): Inverter schematic diagram

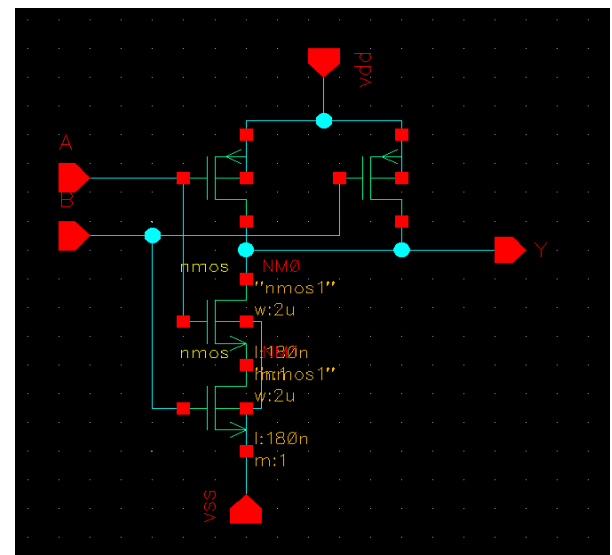


Fig-4(b): NAND gate schematic diagram

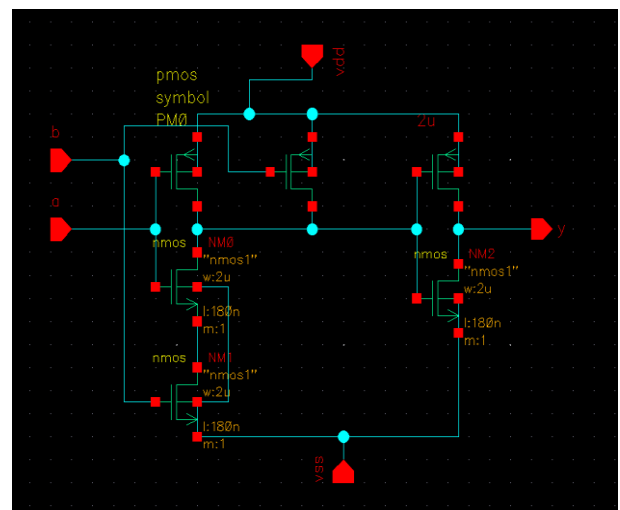
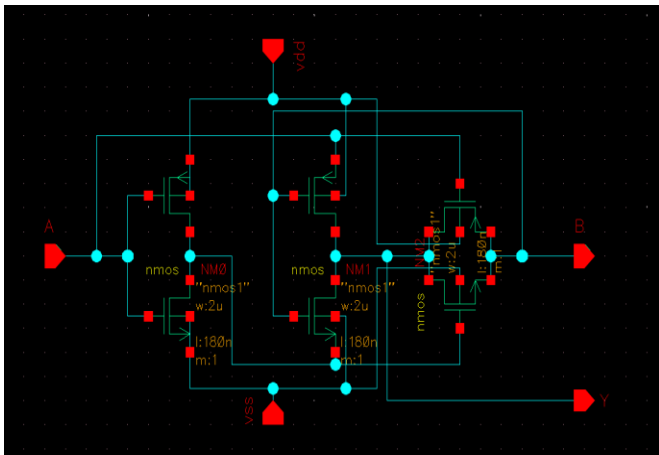
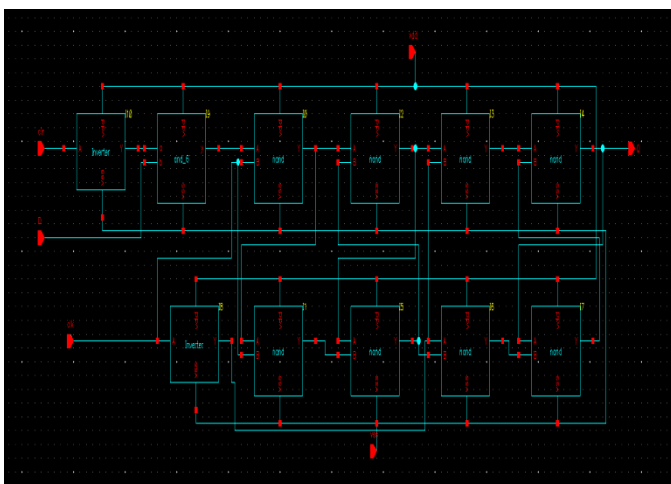


Fig-4(c): AND gate schematic diagram

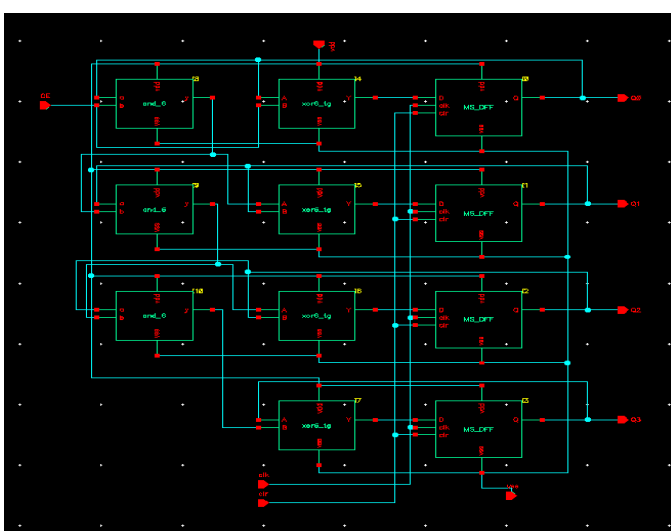


**Fig-4(d):** XOR gate schematic diagram

Using the instances of inverter, NAND gate and AND gate gates discussed above, master-slave D flip-flop is implemented as shown in fig.5. Subsequently using the instances of master-slave D flip-flop, AND gate and XOR gate the proposed synchronous 4-bit up counter is implemented as shown in fig.6.



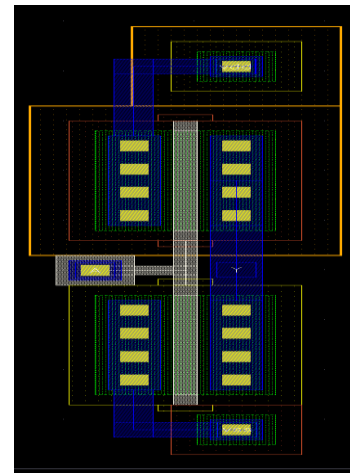
**Fig-5:** Master-slave D flip-flop schematic diagram



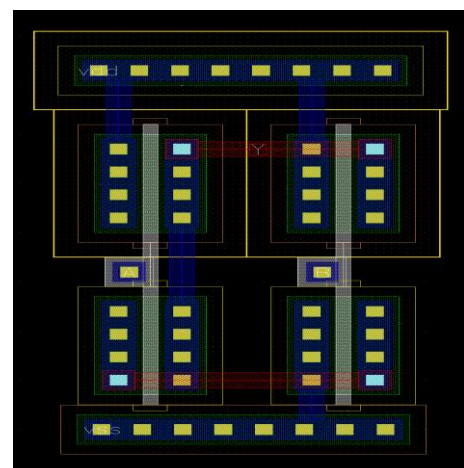
**Fig-6:** Synchronous 4-bit up counter schematic diagram

### 3.2. Layout

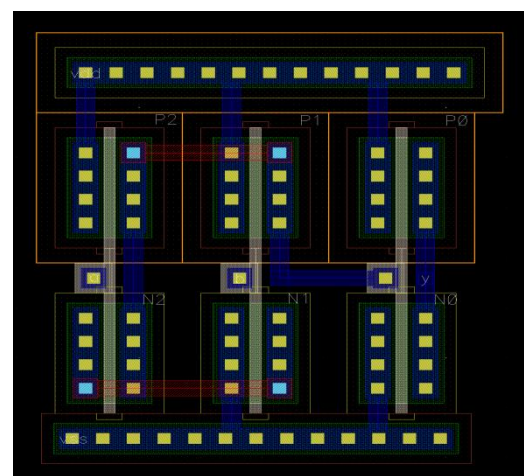
The optimized layout of all the gates, master-slave D flip-flop and synchronous 4-bit up counter are designed using sea of gate arrays concept in order to reduce the area. All the layouts are designed using 180nm CMOS process technology [1]. The cadence tool helps to verify layout versus schematic effectively.



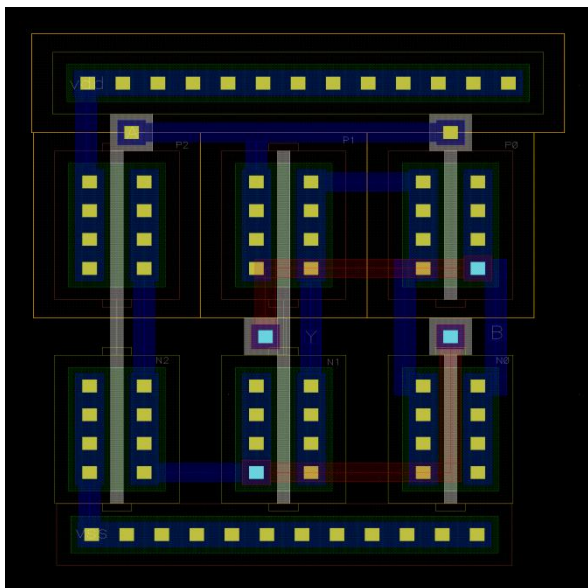
**Fig-7(a):** Inverter layout



**Fig-7(b):** NAND gate layout

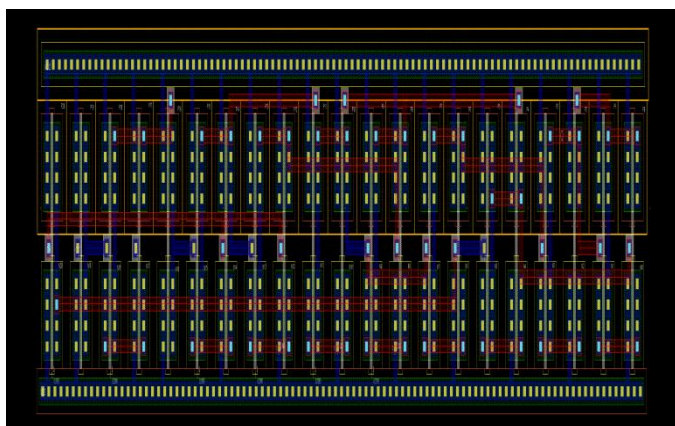


**Fig-7(c):** AND gate layout

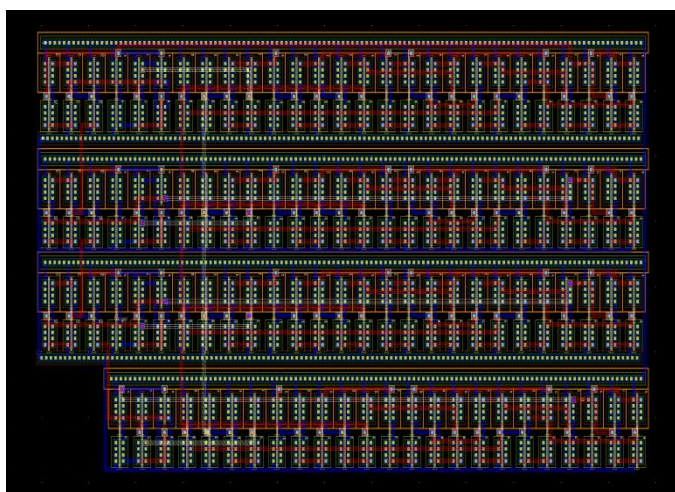


**Fig-7(d):** XOR gate layout

The final layout of the master-slave D flip-flop is designed by integrating the layout instances of the NAND gates and subsequently the layout of the synchronous 4-bit up counter is designed by integrating the layout instances of the basic AND, XOR gates and master-slave D flip-flop.



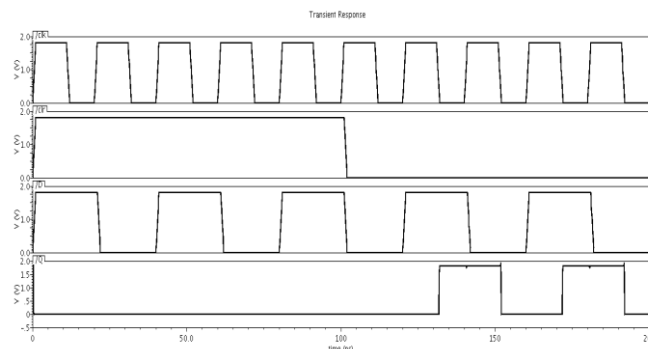
**Fig-8:** Master-slave D flip-flop layout



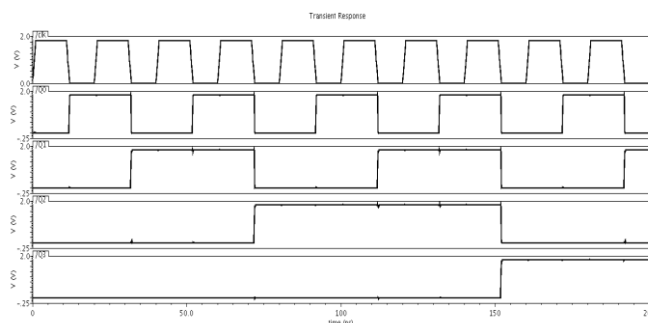
**Fig-9:** Synchronous 4-bit up counter layout

#### 4. SIMULATION RESULTS

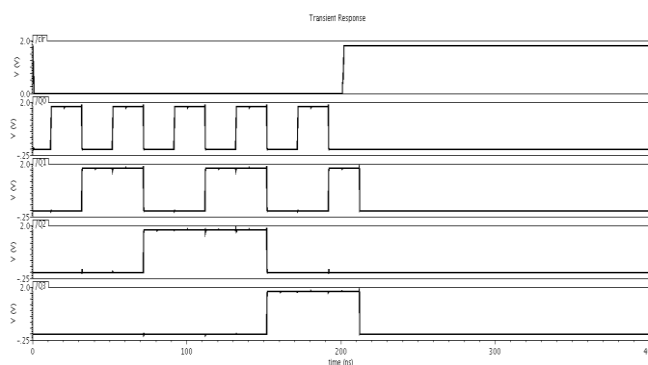
The layouts of master-slave D flip-flop and synchronous 4-bit up counter are simulated and the transient responses are analyzed using Cadence analog design environment.



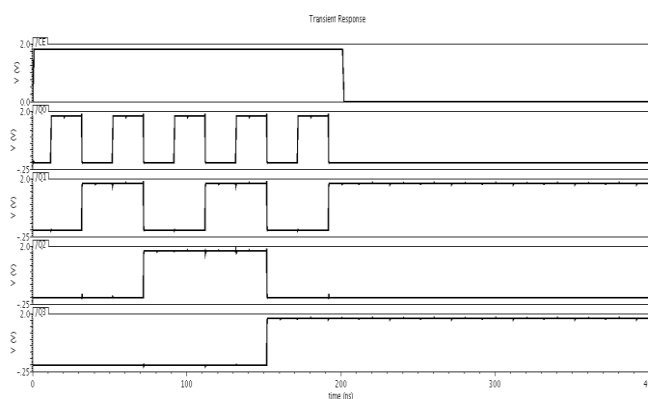
**Fig-10(a):** Transient response of master-slave D flip-flop



**Fig-10(b):** Transient response of counter with CE=1, clr=0



**Fig-10(c):** Transient response of counter with CE=1, clr=1



**Fig-10(d):** Transient response of counter with CE=0, clr=0

**Table-3:** Transistor count, delay and power estimation of the gates, flip-flop and counter

Circuits	Transistor count	Delay	Power
Inverter	2	11.04 ns	4.70 $\mu$ W
NAND gate	4	20.92 ns	5.22 $\mu$ W
AND gate	6	195.50 ps	7.87 $\mu$ W
XOR gate	6	5.985 ns	9.93 $\mu$ W
Master-slave D flip-flop	42	11.22 ns	26.23 $\mu$ W
Synchronous 4-bit up counter	210	20.39 ns	97.90 $\mu$ W

## 5. CONCLUSIONS

In this paper, synchronous 4-bit up counter has been implemented, simulated and analyzed. The performance of the counter is assessed in terms of area, delay and power consumption. The main goal to optimize the layout is met satisfactorily using Cadence tool with the sea of gate arrays concept. The logic and characteristics of the master-slave D flip-flop and synchronous 4-bit up counter are easily verified with the simulation results. Thus we present the design and implementation of synchronous 4-bit up counter which is optimized in terms of area.

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## BIOGRAPHIES



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