TD-AMS PROCESSING FOR VLSI IMPLEMENTATION OF LDPC DECODER

Maramreddy Harish[1], Neelima Koppala[2]

[1]*P.G.Student scholar M.Tech (VLSI), ECE Department, Sree vidyanikethan engineering college (Autonomous)*
[2]*Assistant professor, ECE Department, Sree vidyanikethan engineering college (Autonomous)*

Abstract

An Efficient analog to digital interface (TDC/DTC) is presented. In particular, we explore time-based techniques for data conversion, which can potentially achieve significant reductions in power consumption while keeping silicon chip area will be very small. On the basis of a generic mixed-signal system the scaling difficulties of analog and mixed-signal circuits based on a signal representation in the voltage domain are discussed for nanometer CMOS technologies. Easy to control and seamlessly embedded, were also low latency occur. Mainly applicant for LDPC implementation which is used for error correcting and image processing will be done. In gate level verilog hardware description language used for coding digital circuits using tool Xilinx ISE 10.1i and target family Spartan 3E,Device XC3S500, speed -5,package:FG320.The synthesized for the proposed digital circuits.

Keywords—*low density parity-check (LDPC), time-to-digital converter (TDC), Binary-search time-to digital converter (BS-TDC), low power*

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1. INTRODUCTION

The rationale behind digitally-assisted analog design is to move the accuracy burden from the realm of analog design to the digital domain. Relaxing the precision of the analog circuitry reduces power consumption significantly, while the correction of analog imperfections is implemented in the digital domain, allowing lower power and faster designs[1]. At this point the motivating question shall be discussed why TDCs suddenly become popular in mainstream micro-electronics: Modern VLSI technology is mainly driven by digital circuits. The reasons for this are the many advantages of digital compared to analog circuits: Atomic digital functions can be realized by very small and simple circuits. This results in a compact and cheap implementation of elementary logic functions and enables complex and flexible signal processing systems[2]. A comparable complexity was not feasible with an analog implementation due to area and power consumption but also due to variability and signal integrity.

Flexible means reconfigurable, adjustable or even programmable. Data can be stored easily in digital systems without any loss of information. The design of digital circuits is highly automated resulting in high design efficiency and productivity. However, the main advantage of digital signal processing is the inherent robustness of digital signals against any disturbances, i.e. noise and coupling, as well as the inherent robustness of digital circuits against process variations[4].

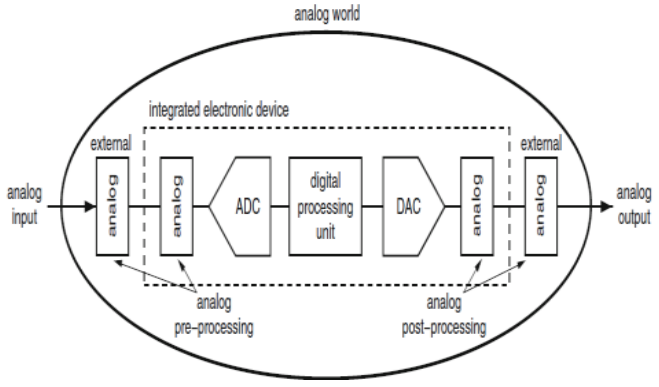

Fig. 1 Generic digital signal processing system

The reduction in supply voltage accompanying technology scaling, which is dramatically Improves the energy and area efficiencies of a digital circuits, makes the realization of voltage domain analog computation circuits, problematic. In order to maintain a dynamic range under such a low supply voltage ,it is necessary to reduce the mismatches and thermal noise ,and that results in large chip area and low power consumption[1] .

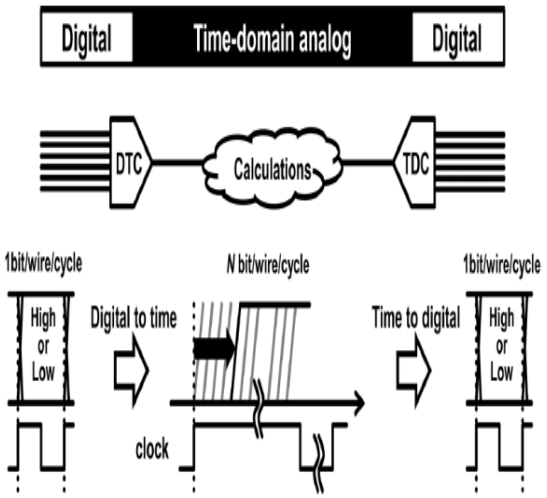

Fig. 2 Basic TD-AMS

2. DIGITAL TO TIME CONVERTER

The circuit diagram of a single-bit DTC and its operation principle are shown in Fig.3 Digital-to-time conversion is realized by selecting a signal from delayed or non-delayed time-domain Signals originated from clk according to a digital input signal. The DTC is composed of unit delay cells with Tdel delay (DELs), NORs, and inverters [1]. When Din is low, node B stays low and a rising edge of passes through two NORs. On the other hand, when is high, the rising edge passes through DEL as well as two NORs. As a result, according to whether is high or low, the timing of the rising edge of varies Dout by Tdel.

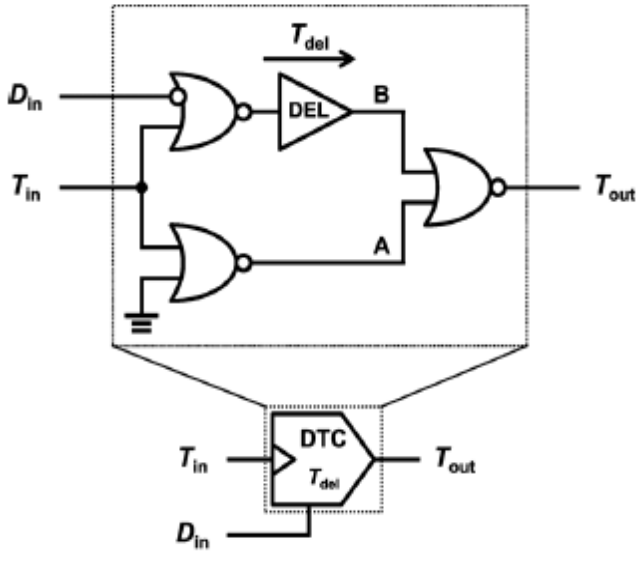

Fig 3 Digital to time converter circuit diagram

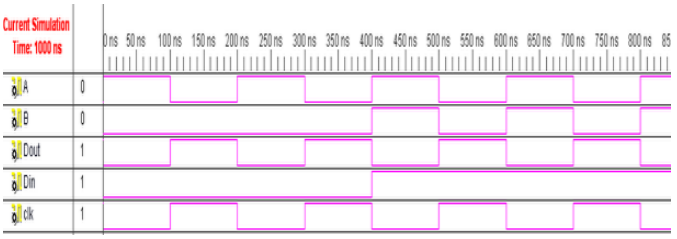

Fig 4 Timing waveform for 1bit DTC

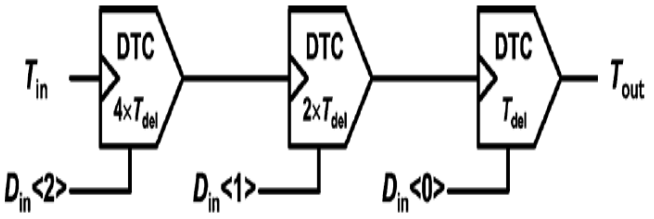

Fig 5 Proposed 3bit DTC circuit diagram

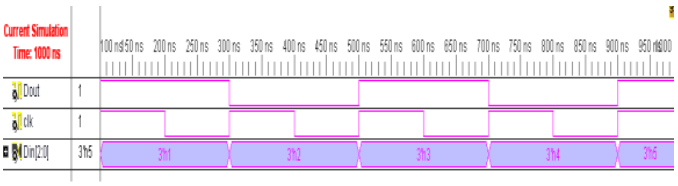

Fig 6 Timing waveform for 3bit DTC diagram

A multi-bit DTC is composed of cascaded single bit DTCs with binary weighted numbers of DELs. For example 3bit

3. CONVENTIONAL TDC AND ITS OPERATION

The operating principle of a TDC based on a digital delay line. The reference clock which is in a more general sense an arbitrary start signal is delayed along the delay-line. On the arrival of the stop signal the delayed versions of the input signal are sampled in parallel. Either latches or flip-flops can be used as sampling elements. The sampling process freezes the state of the delay-line at the instance where the clock signal occurs [7].These results in a thermometer code because all delay stages which have been already passed by the start signal give a HIGH value at the outputs of the sampling elements, all delay stages which have not been passed by the input signal yet give a LOW value. The position of the HIGH-LOW transition in this thermometer code indicates how far the input signal could propagate during the time interval spanned by the input and the clock signal. Hence this transition is a measure for the time interval .An excellent style manual for science writers is [7].

An implementation of the basic delay-line TDC is shown in Fig. 7. The input signal ripples along a buffer chain that produces the delayed signals input[7]. Flip-flops are connected to the outputs of the delay elements and sample the state of the delay line on the rising edge of the clk signal. The clk signal drives a high number of flip-flops so a buffer-tree (not shown) is required. Any skew in this buffer-tree directly contributes to the non-linearity of the TDC characteristics.

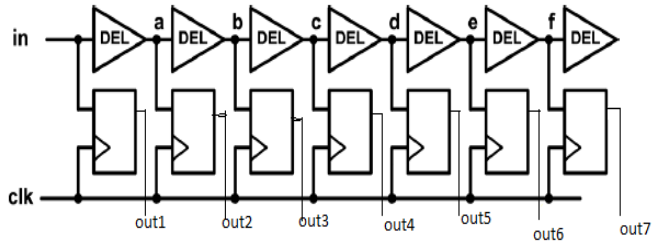

Fig 7 Delay based conventional TDC circuit diagram

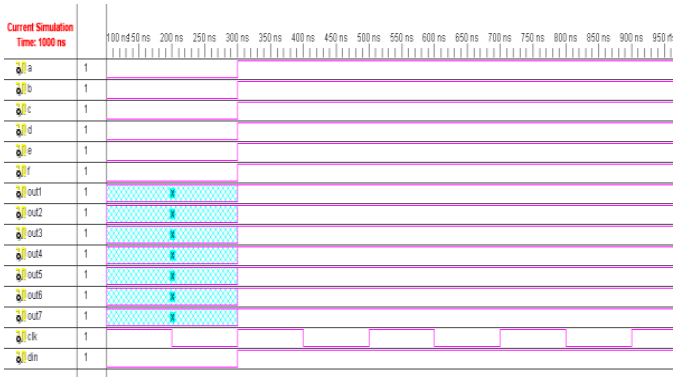

Fig. 8 Timing diagram for delay based conventional TDC

4. BINARY SEARCH TDC

TDCs are extensively researched now days for use in all digital PLLs in wireless Transceivers so on, because a TDC can gain the full benefits of deep submicron CMOS process. Before explanation of binary search TDC (BS-TDC) proposed circuit just briefly describe a conventional TDC, which is composed in the form delay chain and flip-flops. In other words, the required number of flip-flops increases extremely based n bits, which is a lead to more area and delay.

In order to reduce those parameters, we proposed BS-TDC based on binary search algorithm. As shown below fig.11.the n-bit BS-TDC is composed only of n FFs, where as there are 2^n-1 FFs in a conventional TDC. Because the area and power for FFs are dominant in TDCs, reducing FFs directly results in area and power reduction. Although a binary-search approach is commonly used in voltage-domain ADCs, some tricks are required in order to apply it to a TDC because time can neither be stored nor subtracted[1].

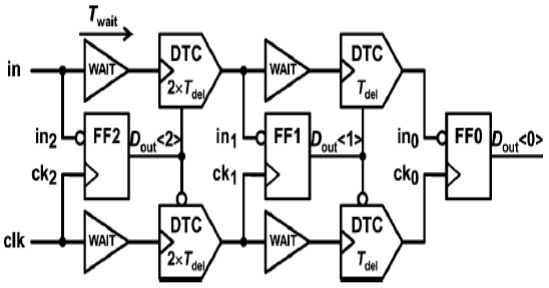

Fig. 9 Circuit diagram of the Binary search TDC

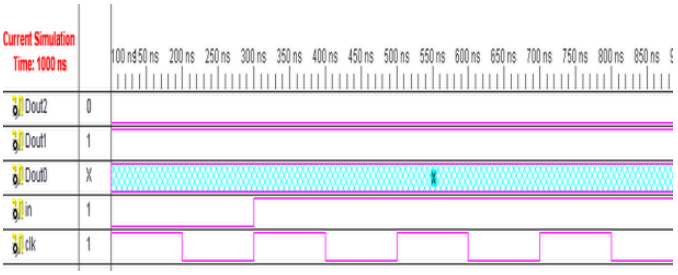

Fig. 10 Timing waveform for binary search TDC

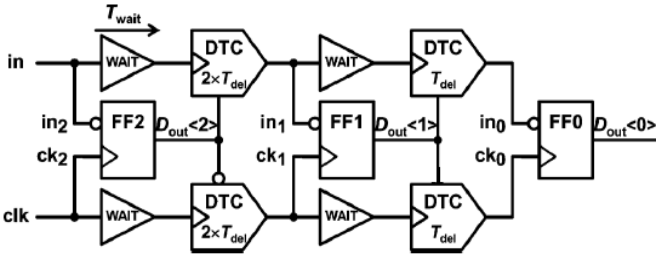

Fig. 11 Circuit diagram of the new proposed Binary search TDC

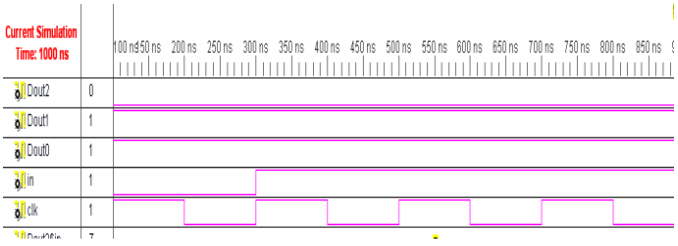

Fig 12 Timing waveform for new proposed binary search TDC

But in fig.9 binary search TDC has logic error is there .when an input is high then one output will become doesn't exist because the clk will become low[7] .so that the logical error applied in proposed binary search TDC .so, that a modification of changing the inverted input at DTC to normal input is done in the above fig.9

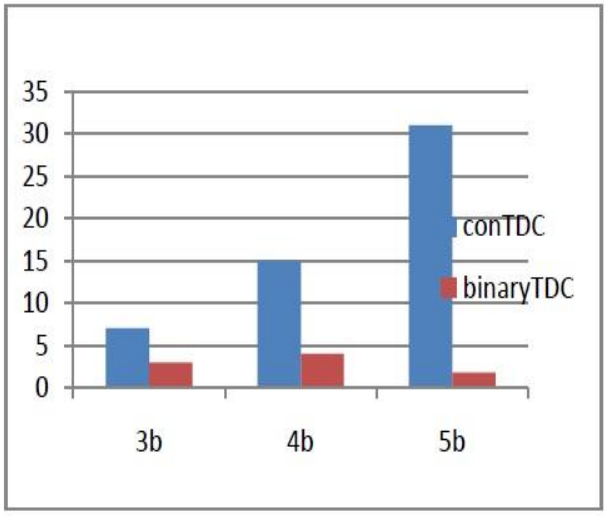

Fig. 13 Comparison area based on LUTs conventional TDC and binary search TDC

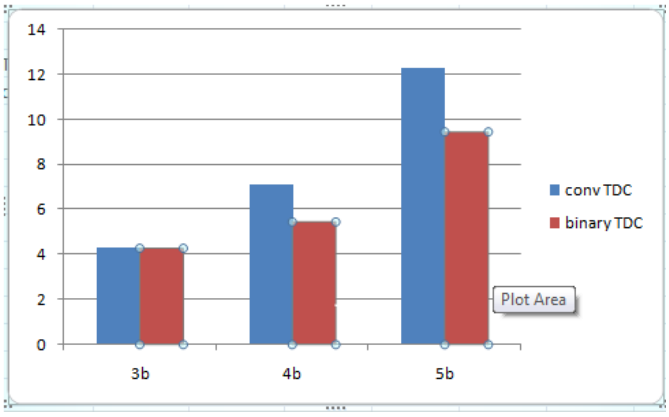

Fig. 14 Comparison combinational delay between conventional TDC and Binary TDC

Table 1: Performance summary comparison conventional TDC and BS-TDC

Types of TDC /parameter	Conventional TDC			Binary search TDC		
Number of bits (n)	3b	4b	5b	3b	4b	5b
Number of LUTs	7	15	31	3	4	5
Delay(ns)	4.32	7.11	12.23	4.2	5.9	9.7

5. ACCURACY OF DTC AND TDC

The accuracy of DTC and TDC with simulation of the circuit show in fig.15 A 1b digital input of DTC is converted into time domain signal and TDC converted digital output Dout .In order based on clock signal DTC and another input 011 taken input to full range of the DTC [4] .Then output of TDC Dout will be high .But the digital logic should not mismatches, if it so error occurrence will be appear. The simulation result in hardware implementation is given below fig16.

6. MINIMUM CALCULATION

A minimum calculation, which is most frequently, appears in min-sum algorithm for LDPC code decoding, is executable by a single 1bit Comparator gate as shown in Fig. 17. The output of OR becomes high when any one of the input signals becomes high. Then, among the input signals with various rising edge timings, the OR can find the fastest one, which corresponds to the minimal value[7]. A simulation result is shown in Fig. 18. These calculations are obviously more efficient than the digital counterparts.

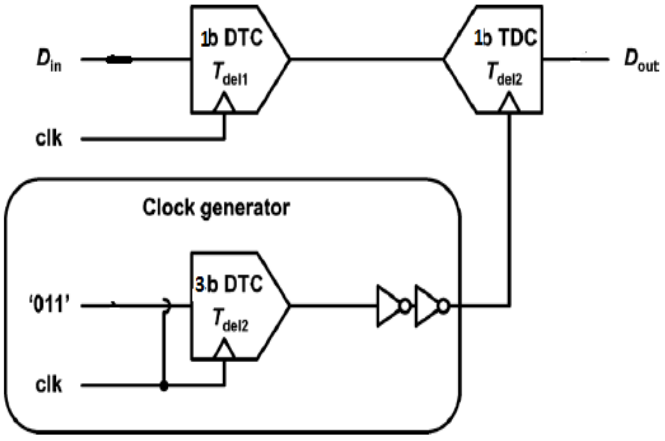

Fig. 15 Circuit diagram of accuracy of DTC and TDC

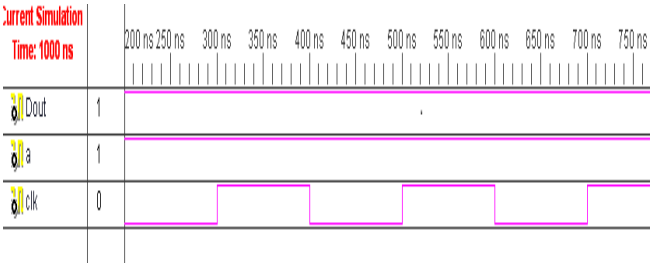

Fig. 16 Timing waveform for Accuracy

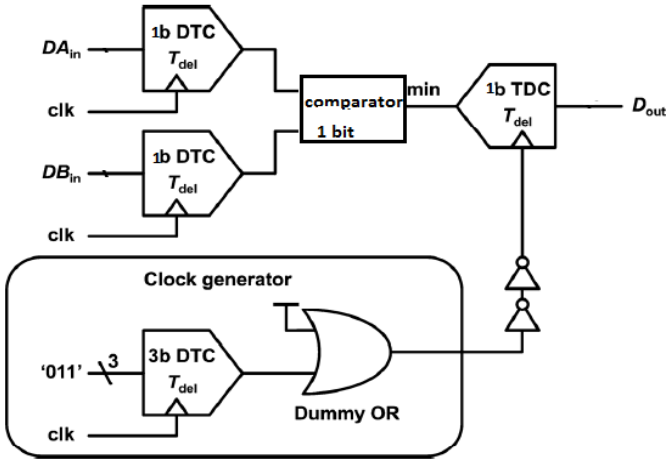

Fig. 16 Circuit diagram of Minimum calculation

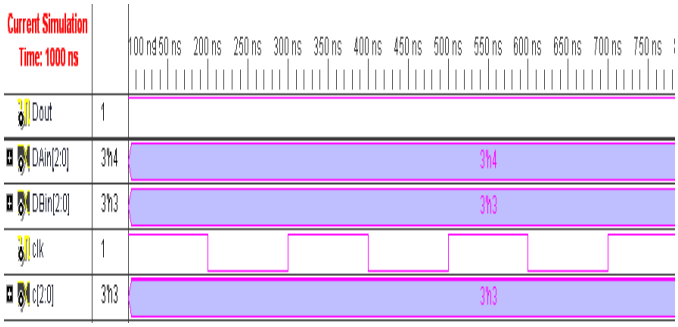

Fig. 17 Timing waveform for minimum calculation

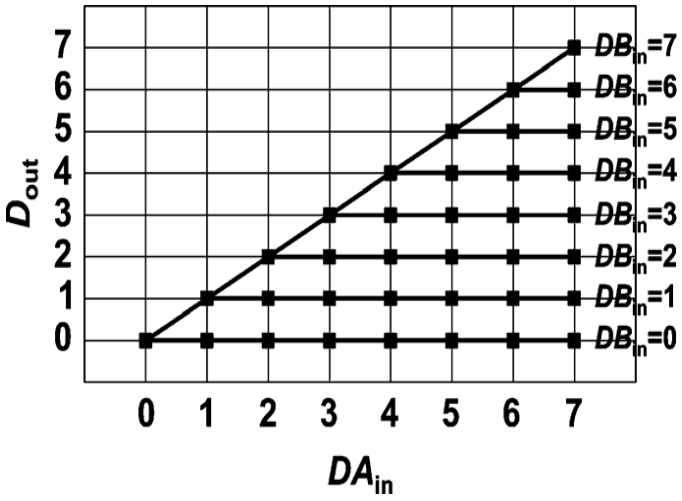

Fig. 18 simulation results for minimum calculation

7. LOW DENSITY PARITY CHECK CODES

Low-density parity-check codes are a class of linear block code defined by a sparse M x N parity-check matrix, H [5],where N > M and M = N − K. Although LDPC codes can be generalized to non-binary symbols, we consider only binary codes. The parity-check matrix has a small number of '1' entries compared to '0' entries, making it sparse. The number of '1's in a parity-check matrix row is called the row-weight, k, and the number of '1's in a column is the column-weight, j. A regular LDPC code is one in which both row and column weights are constant, otherwise, the parity check matrix is irregular. Although a LDPC code is defined by a sparse matrix, a bipartite graph, also known as a Tanner graph, can be used to represent the code. A bipartite graph is a graph whose nodes can be divided into two sets such that each node is connected to a node in the other set. The two sets of nodes in a Tanner graph are called check nodes and variable nodes representing rows and columns respectively[6].

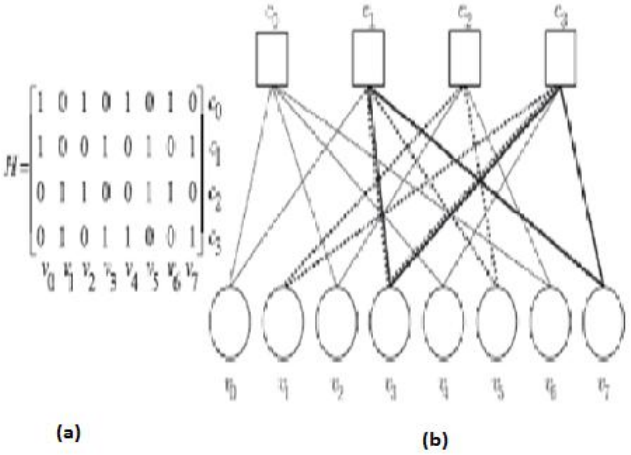

Fig.19 (a)parity check matrix (b) Tanner graph Representation

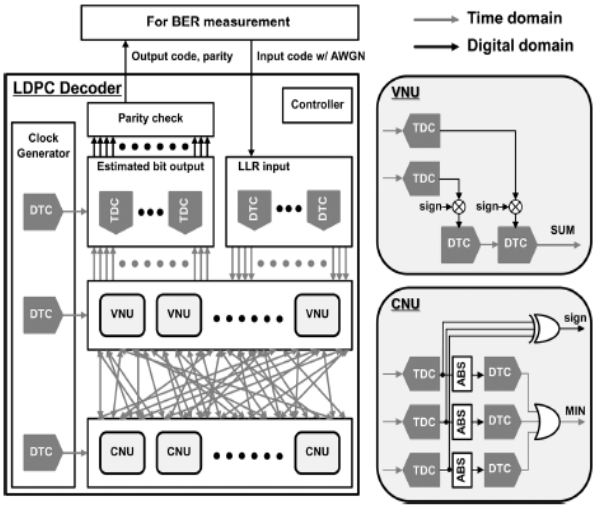

Fig. 20 Architecture of LDPC decoder

Tanner graph representation will be reduced to minimum routing congestion and also reduced power consumption[6].

Fig20.illustrates the overall architecture of the implementation (8,4) LDPC decoder leveraging TD-AMS .It is mainly of variable node function units(VNUs) corresponding to (1) and check node function units(CNUs) corresponding to (2). The calculations in the VNUs and CNUs are partitioned into the time domain and digital domain, considering efficiency. The minimum function in the CNU and the summation function in the VNU are executed in the time domain, whereas absolute value (ABS) and XOR function in the CNU are executed in the digital domain.

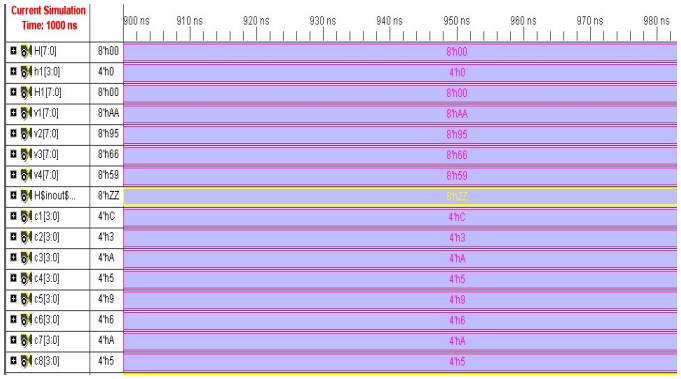

Fig. 21 Timing waveform for parity check matrix

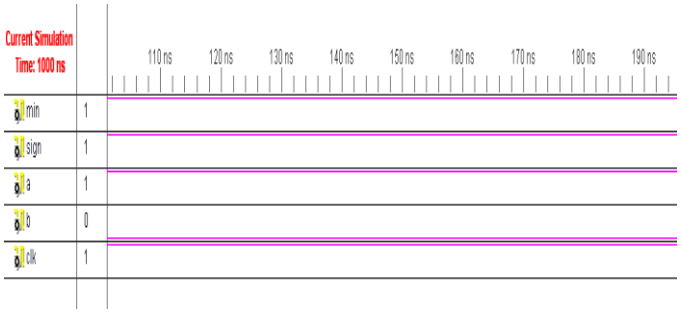

Fig. 22 Timing waveform for check node unit

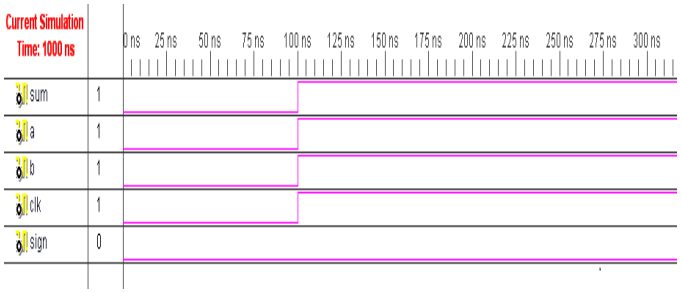

Fig. 23 Timing waveform for variable node unit

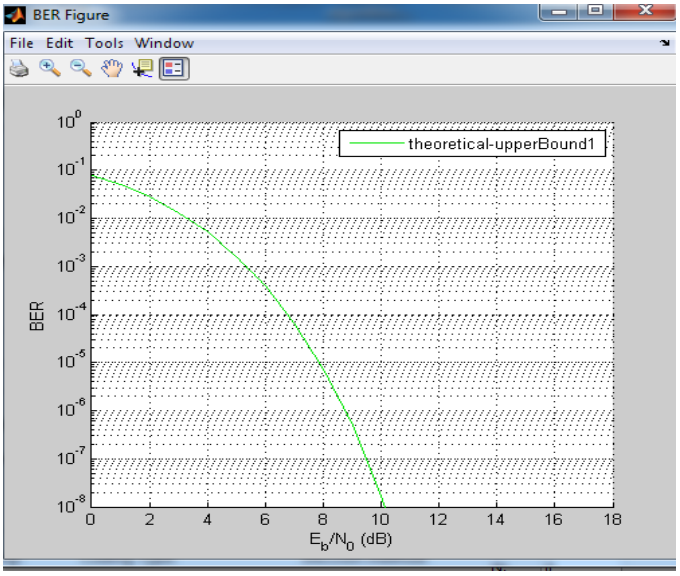

Fig. 24 BER measurement results

8. EXPERIMENTAL RESULTS

All the circuits in TD-AMS including TDC and DTC are developed verilog hardware description language in the same way digital .These modules can be incorporated in the verilog simulations of the system including general digital modules. LDPC decoder with proposed time –domain analog and digital mixed signal processing .LDPC is implemented in 90 nm technology and Bit error rate (BER) measurement results is calculated in MATLAB tool

9. CONCLUSIONS

The analog circuitry is reduced to two simple building blocks, leading to less design complexity and lower power consumption. But this trade-off is quite favorable given recent technological advancements in nanometer CMOS technologies. The proposed technique is binary search TDC can enhance the delay and area efficiencies of computing especially in applications where high calculation accuracy and complete answers are not required, such as error correction and Image processing. Bit error rate is reduced also power consumption will be reduced.

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