CARRIER RECOVERY AND CLOCK RECOVERY FOR QPSK DEMODULATION

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Abstract

This paper deals with the design and implementation aspects of high data rate digital demodulators. The Existing remote sensing satellites support data rates of several hundred mega bits per second. The future trend is towards giga bit rate transmission. This necessitates for demodulators of the ground receive system to process faster and handle the ever-rising data throughput more efficiently. Different Satellites use different modulation schemes with variable data rates. In order to cater to the Multi mission /Multi-satellite data reception requirements of a ground station, it is necessary to have greater flexibility and programmability features embedded in the design of demodulators. The demodulation techniques for Binary / Quadrature Phase shift Keying (BPSK/ QPSK) are well established and understood when implemented with analog circuits. The BPSK/ QPSK can be demodulated by different techniques such as squaring loop, Costas loop and others in analog domain. The Costas loop technique is adopted for developing the digital demodulator because unlike in Square Loop technique, in this the carrier recovery and data demodulation can be done simultaneously with simple blocks level design. The high data rate digital demodulator performs IF amplification, filtering and analog to digital conversion of the received IF signal followed by a Digital demodulator. The basic design strategy includes a configurable data rate BPSK/ QPSK demodulation with COSTAS loop circuitry utilizing the flexibility of FPGA implementation. The basic design considering a sampling clock from local clock oscillator operating at 125 MHz and 70 MHz carrier down converted to 30 MHz for 8 Mbps data rate (For BPSK). Later the sampling clock is increased to 250 MHz and the carrier is direct 70 MHz with data rate 42.4456 Mbps (For QPSK). The Performance of the Demodulator is evaluated using MATLAB simulation tools. The development has done with ISE implementation tools. The purpose of this paper is to evaluate the new technology by implementing a BPSK/QPSK demodulator on an ADC-FPGA board. A mathematical algorithm was developed and implemented with ISE tools for digital demodulator design. The input test signals from Modulation Simulators and signal generators have been interfaced to the FPGA board through Analog-To-Digital Converter (ADC). The recovered carrier output and I, Q demodulated data patterns have been verified through ISE tools and Wave Vision Software for FFT analysis.

Keywords—*Digital Demodulator (BPSK/QPSK); Earth Station data reception, digital Down conversion, Carrier recovery, Loop filter, Finite impulse Response (FIR), Phase word, Digital Synthesizer, COSTAS loop.*

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1. DESIGN OF COSTAS CARRIER RECOVERY LOOP

Carrier recovery is the process of extracting a coherent reference carrier from the received modulated carrier signal. To correctly demodulate the data, a phase & frequency coherent carrier is to be recovered and compared with the received signal in a product detector/ Multiplier. To determine the absolute phase of the received signal it is necessary to reproduce a carrier at the receiver that is in phase & frequency coherence with the transmit reference oscillator. In the case of High data rate BPSK/QPSK modulated signal the carrier cannot simply be tracked with a standard Phase-lock loops (PLL) at the receiver, but a more sophisticated method of carrier recovery is required. Phase-lock loops (PLLs) have been one of the basic building blocks in modern communication systems.

There are many kinds of Phase Lock Loops: the Costas Loop or Quadrature loop, which is named by J. P. Costas, a pioneer in synchronous communications, is a very good choice for the high data rate digital demodulator design. The implementation is very powerful and useful in many situations. Further we can precisely determine and correct the Doppler variations.

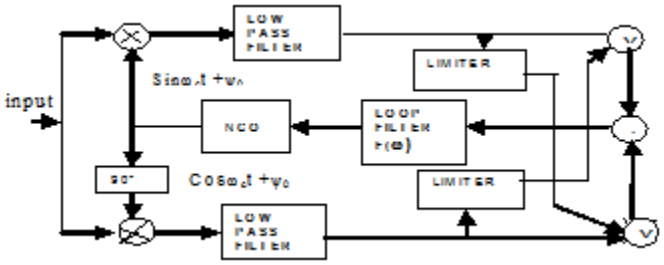

Fig 1: Block diagram of a basic Costas loop carrier recovery design

The Costas or the quadrature loop involves two parallel tracking loops operating simultaneously from the same NCO (Ref fig.5). One loop called the in-phase loop uses the NCO directly for tracking .The other loop uses 90 degrees shifted NCO .The mixer outputs are multiplied, filtered with FIR and used to control the NCO frequency and phase control word. The low pass filters (FIR) in each arm must be wide enough to pass the carrier modulation without distortion. The in-phase mixer generates the cosine terms. The quadrature mixer generates the sine terms.

The multiplier output

$I(t) . Q(t) = A2.m2 (t) . \sin\Psi e . \cos\Psi e$
$= A2/2 . 2.\sin\Psi e(t).$

Where Ψe is the phase error

The double frequency terms are eliminated by the Low pass filters following the common multiplication between two parallel tracking loops. An error signal is generated by this multiplication. The error signal is filtered by a Loop filter, whose output is the control word which controls the frequency and phase of NCO. The Costas loop thus tracks the phase variations with NCO without interference from the carrier modulation.

The limiter cross over arms in extended COSTAS loop design is used for controlling the amplitude variations and regulates the CNR within the loop. At high SNR the limiter out put will have sign that is identical to the present data bit polarity. The Low pass filters outputs can be passed through threshold detectors and can be used directly for next stage development Bit synchronization module. The output of the NCO contains a phase ambiguity of Π/4 rad, it can be overcome by differential encoding of the data at the transmitter and differential decoding after demodulation at the receiver.

The loop filter bandwidth and the arm filter (FIR) bandwidths are the critical tasks to be addressed for designing the demodulator to cater to multi-mission data reception application.

The fundamental expression that relates the mean squared phase jitter in the phase lock loop to the SNR in the loop is

$\sigma_\varphi^2 = 1/\rho \text{ rad}^2$,
$= (B_{L\,/}\, B_i) *[1/ (S/N)i]$

Where ρ = SNR in the loop,
(S/N)i = input Signal-to-Noise ratio
B_L = One sided loop Bandwidth
B_i = One sided IF bandwidth (Arm filter bandwidth)

If S_L is the squaring loss in the carrier regeneration process,

$\sigma_\varphi^2 = 1/\rho_L S_L$ Where $\rho_{L\,=}$ Loop SNR

The term squaring loss is used to describe the degradation in the loop SNR due to S*N and N*N distortions occurring in the arm filters. The squaring loss depends on the shape of the input pre-filter, the data waveform and the Eb/No.

$S_L = \underline{h_1} + \underline{h_2\, T_{b\,/}\alpha}\ \alpha\ 2\ Eb/No$

Where T_b = Bit duration
α = Bif / Rs
Bif = Double sided IF bandwidth
Rs = Data rate

$$h_1 = 1/2\pi \int_{-\infty}^{\infty} Sm(\omega)\, l\, Hc(\omega)l^4\, d\omega$$

$$h_2 = 1/2\pi \int_{-\infty}^{\infty} l\, Hc(\omega)l^4\, d\omega$$

Where Hc (ω) = Low pass equivalent of the input band pass filter transfer function.
Sm (ω) = Spectrum of the modulated signal.

It is seen from the above relation that if the input pre-filter band width is too wide relative to the bit duration $1/T_b$, h1 and h2 will increase, while if it is too narrow, α decreases and both of these increase the squaring loss. QPSK requires much higher S/N ratio in the XPLL than that required for BPSK for a given bit error rate performance.

The analysis substantiated with the practical results indicate that the double sided loop band width of 200 KHz for the Costas PLL is adequate for QPSK operation up to the Symbol rates of about 21.2257 MBPS. For lower data rates (< 10 MBPS) the loop bandwidth has to be narrowed for better SNR. The Pre-filter band width has to be designed as equivalent to 55% of the highest baud rate expected.

The Digital implementation of the basic Costas loop for High data rate BPSK/ QPSK demodulator is proposed to be carried

out on a Single Virtex-5 FPGA. Xilinx ISE is Programmable Logic Development software. The compilation of the design is dramatically faster than other PLD development tools, allowing us to quickly implement changes and list the results in order to meet the specifications. As the design cycle is accelerated one can quickly go through many design iterations. An average high-density design of up to 100,000 gates can be compiled in less than 30 minutes thus giving more time to make analysis for perfect design. Xilinx ISE design environment offers unmatched flexibility and performance. This software allows for seamless integration with industry standard design entry, synthesis and verification tools. MATLAB simulation checks are utilized for proper analysis of the design.

Apart from the general advantages with digital systems, a digital version of the phase-lock loop solves some of the problems associated with its analogue counterpart; namely sensitivity to DC drifts and component saturation, difficulties encountered in building higher order loops and need for initial calibration and periodic adjustments. In addition, with the ability to perform elaborate real-time processing on the signal samples, the Digital PLL (DPLL) can be made more flexible and versatile using FPGA. A carrier recovery system is a PLL circuit used to estimate and compensate for frequency and phase differences between a received signal and the receiver's local oscillator for the purpose of coherent demodulation. The loop should acquire and track the changes in carrier frequency (or phase) due to Doppler variation.

The Digital Costas loop (DCL) has four basic components: a phase detector, numerically controlled oscillator (NCO), digital low pass FIR and a loop filter, required interface between loop filter output and NCO input. A high order (FIR) Low pass filter and 2nd order loop filter are adequate to track the data and Doppler shift variations with good performance.

1.1 Mathematical Description for QPSK Costas Loop

The input to the Costas loop is the waveform written as

$$y(t) = I'(t)\cos\big(\omega_c t + \psi(t)\big) + Q'(t)\sin(\omega_c t + \psi(t)) + n(t)$$

Where n(t) is a white band pass noise.

The in-phase mixer generates

$$I(t) = \frac{I'(t)\cos(\psi(t))}{2} + n_{mc}(t) + terms\ at\ frequency\ 2\omega_c$$

While the quadrature mixer generates

$$Q(t) = \frac{Q'(t)\sin(\psi(t))}{2} + n_{ms}(t) + terms\ at\ frequency\ 2\omega_c$$

Where the mixer noise n_{mc} (t) and n_{ms} (t) are low pass demodulated noise processes in the carrier noise n (t). The higher frequency components are removed by FIR low pass filter. The output of the multiplier is then

$$I(t)Q(t) = \frac{I'(t)Q'(t)\sin\big(2\psi(t)\big)}{8} + n_{sq}(t)$$

Where n_{sq}(t) represents all the signal and noise cross-products. The multiplier of the Costas loop can be thought of as allowing the bit polarity of the in-phase loop to correct the phase error orientation of the tracking loop, thereby removing the modulation.

1.2 Design Considerations

The design has planned to simulate with the following parameters:
Sampling frequency: 100-250MHz
Carrier frequency: 30 MHz (for BPSK)
70 MHz (for QPSK)
Low pass filters used: Raised Cosine FIR
FIR sampling frequency (fs):
25MHz (8 MBPS BPSK)
50MHz (21.2257MBPS QPSK)
FIR Cutoff frequency : fs /4
Loop filter used: 2nd order Butterworth IIR
Loop filter cutoff frequency : 200 KHz

1.3 Design Strategy for FPGA Implementation

- Finalize the Basic level specifications and Functional Block diagram
- Arithmetic realization of the QPSK Demodulator and Bit Synchronizer Designs
- Simulation and Modeling with Matlab and Simulink for Mathematical analysis and verification
- Sub modules Implementation with VHDL and System Generator
- Logic Verification and Timing verification for each module
- Integration of all modules and final level logic verification with ModelSim
- Selection of FPGA (Virtex 5 series Xilinx FPGA chosen for this development)
- Translate, Place and Route the Design to required FPGA device
- Timing Analysis
- Hardware Co simulation and testing with Evaluation Boards and Chipscope pro tool / logic analyzer
- Verification with external analog data through ADC and Signal Generators

- Validation of results with respect to theoretical and MATlab results

2. DIGITAL IMPLEMENTATION OF COSTAS BLOCKS

2.1. Phase Detector

It compares the phase difference between synthesized output frequency and reference input. Commonly used XOR gate or fixed point Multipliers can be selected. The function of the phase detector is to generate an error signal, which is used to return the oscillator frequency whenever its output deviates from a reference input signal.

2.2 Digital Low Pass FIR Filter

Mixed signal has to be filtered to isolate the portion of the spectrum containing the signal of interest. The filter typically has to be a narrow-band filter with a fairly high rejection of unwanted spectrum. This is to done at a much lower sample rate using a less computationally intensive filter.

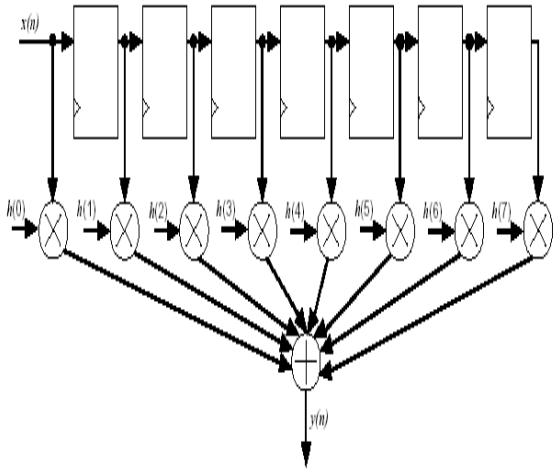

Fig 2: FIR Digital Filter Design

The design of FIR can be done with Filter Design and Analysis (FDA) Tool from MAT lab simulator. The following details has to provide for the FDA tool : Type of Filter (RRC) , Pass band and Stop band frequencies (as per the required data rates) , Sampling frequency (4 times the data rates), Pass band and stop band ripples.

The FIR design for a single MAC is as follows:

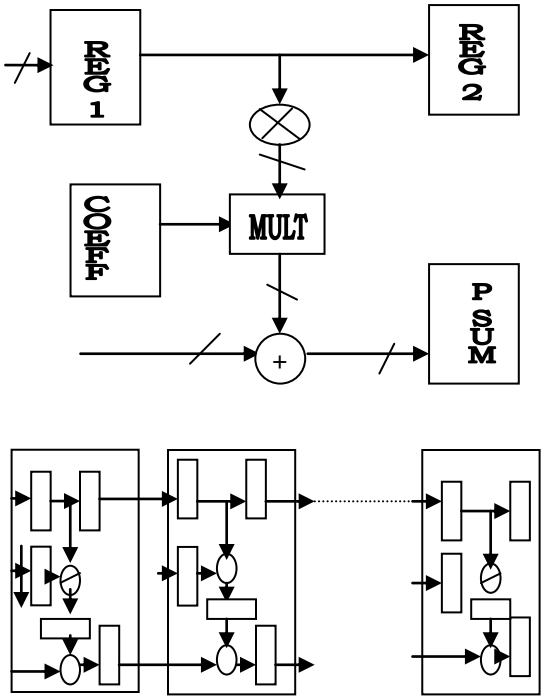

Fig 3: FIR Filter Organization

This FIR filter is implemented in FPGA using VHDL simulation on Xilinx development tools. The Basic design Parameters of FIR filter are

- Fully configurable fixed point FIR filter
- Two's complement arithmetic
- Pipeline architecture
- Parametric filter order (no. of taps), data and coefficient width
- Configurable output precision
- Coefficients stored in internal ROM

Hardware Test Plan: Simulate filter impulse response in VHDL simulation tool Synthesize filter using VHDL synthesis tool. Place-and-route using Xilinx place-and-route tools - circuit clock speed is output by this tool -circuit area is determined by the number of slices/CLBs used.

2.3 Loop Filter

- It converts the phase difference (error signal from previous multiplier section) to the frequency deviation.
- It is implemented as a second order low pass filter and generates signals to control the NCO.
- The Transfer function is obtained from the pole – zero plot which in turn is obtained from MATLAB Filter Design & Analysis (FDA) Tool.

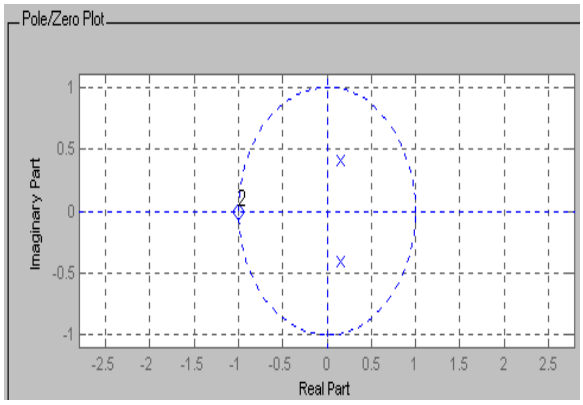

Fig 4: Pole-Zero Plot of Loop Filter

The transfer function is = $\frac{(Z+1)}{(Z-0.2-0.4j)\,(Z-0.2+0.4j)}$

2.4 Numerically Controlled Oscillator (NCO)

This component generates a sampled digital sinusoid, which when mixed with the incoming signal, shifts the signal's spectrum. If we multiply (mix) a signal with a sine wave, we get a frequency translation or "shift" of the spectral image. The amount of translation is equal to the frequency of the "carrier" sine wave.

The NCO generally consists of a digital waveform generator that increments a phase counter by a per-sample increment. This phase is then looked up in a waveform table to create a sine waveform .The output frequency of NCO is controlled by the loop filter output. If no frequency correction is needed, output frequency is equal to the Costas Loop central frequency. The NCO center frequency is programmable.

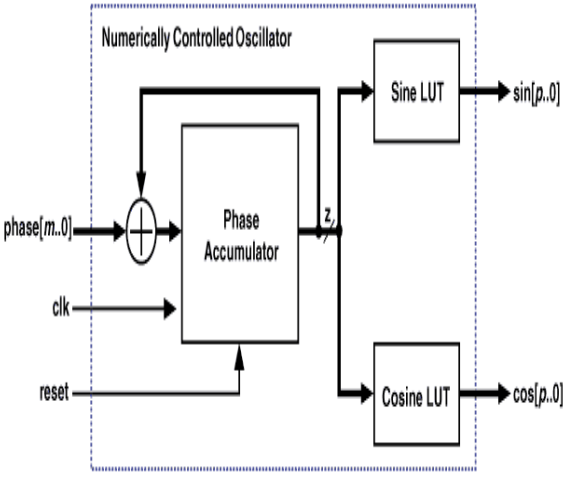

Fig 5: Numerically Controlled Oscillator

The digitally implemented NCO gives Simultaneous quadrature outputs. Parameterized phase accumulator width and output data width. The optimized design from Xilinx Core generators (DDS Synthesizer) has adopted for this purpose. It is Ideal for the Modulators/demodulators functions.

QPSK Costas Loop Implementation

A system-level design was developed that modeled a simple transmitter and channel that simulated a QPSK modulated Signal for a data rate of 42.4456 MB.

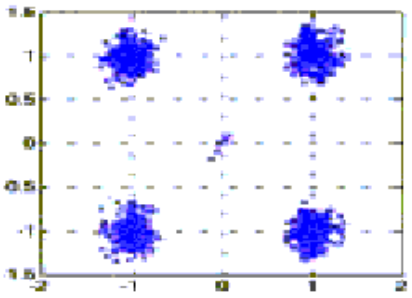

Fig 6: Modulation constellation diagram

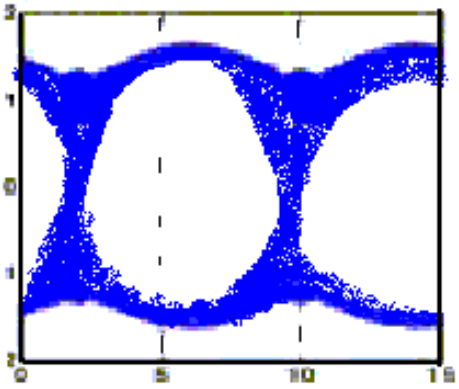

Fig 7: Eye diagram - transmitter.

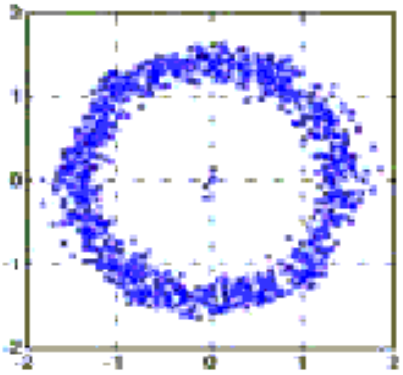

Fig 8: Rotating constellation

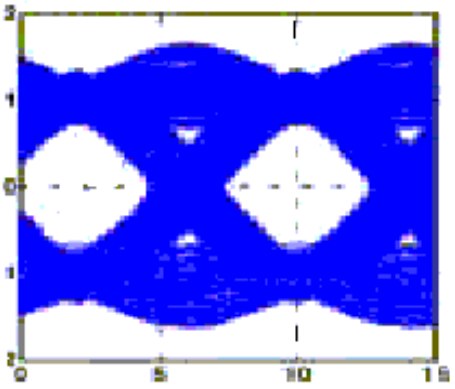

Fig 9: Eye diagram –receiver

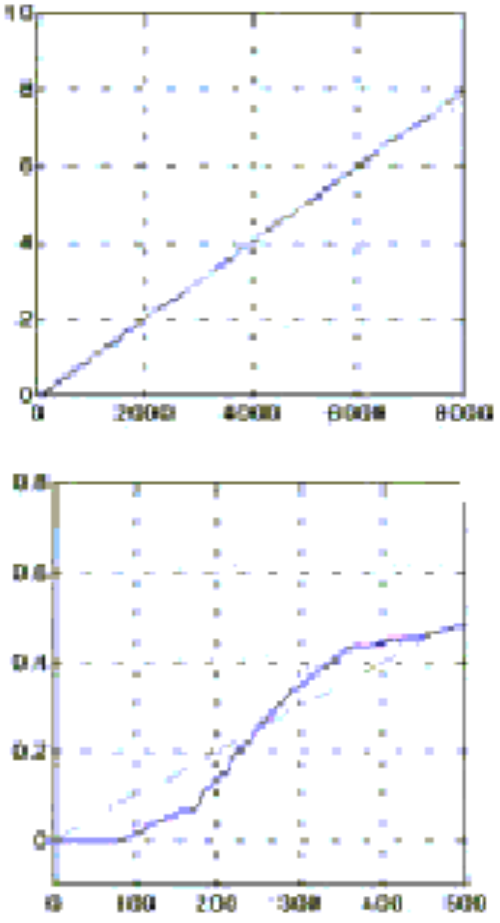

Fig 10: Input and output phase slopes

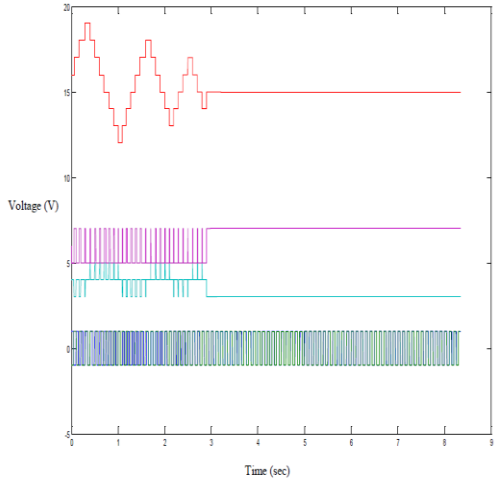

Fig11: Clock Recovery along with Error signal

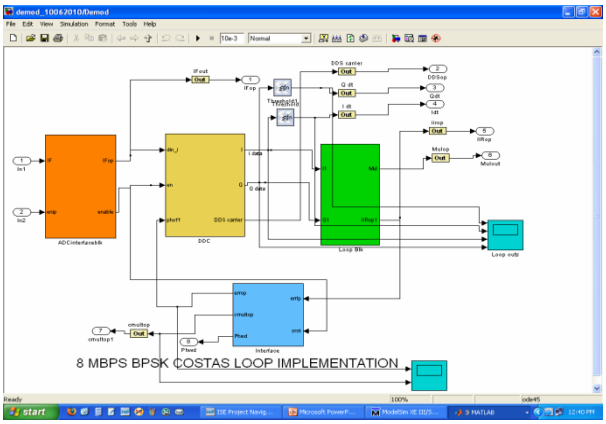

Fig 12: 8Mbps BPSK Costas Loop Implementation

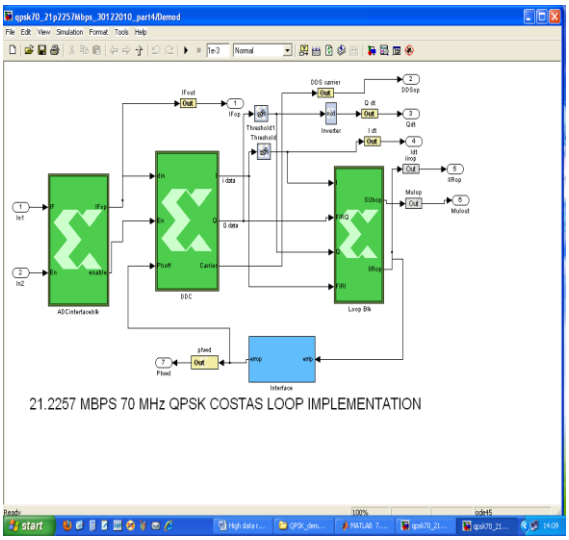

Fig13: 21.2257Mbps QPSK Costas Loop Implementation

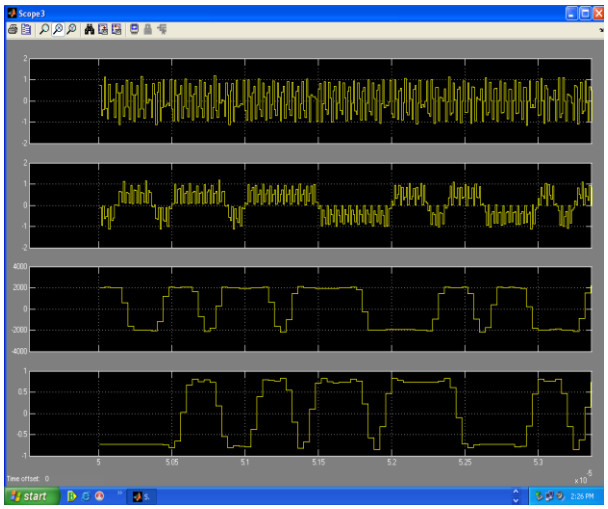

Fig 14: Mixer and FIR output responses

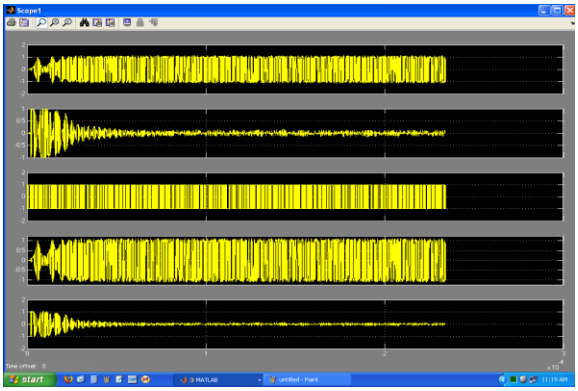

Fig 15: FIR and Loop filter output responses

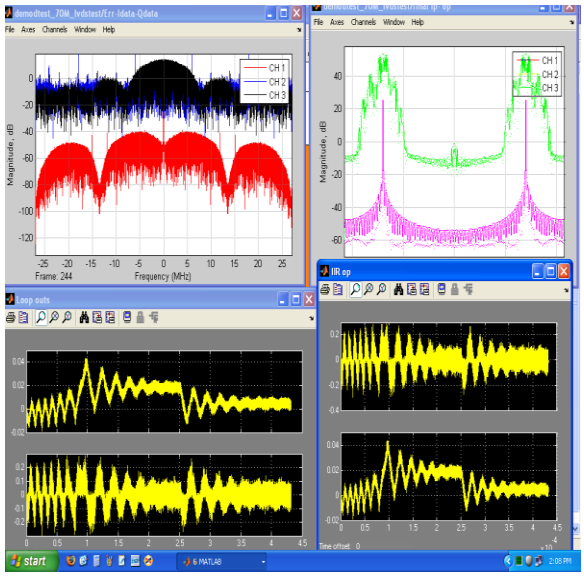

Fig 16: Carrier recovery from variation of input frequencies

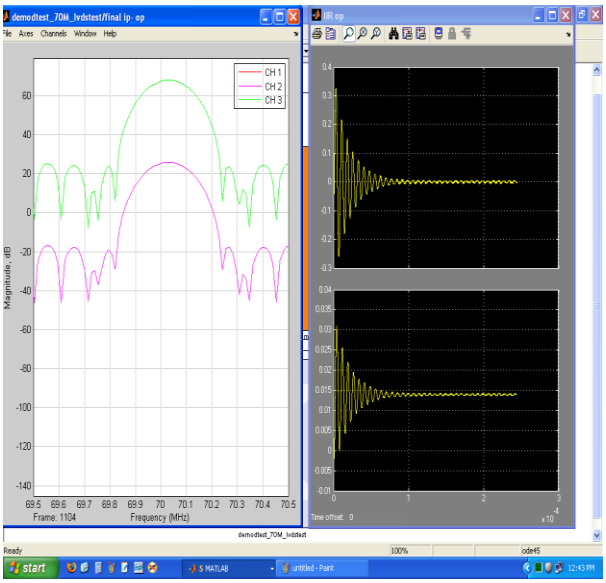

Fig 17: 70 MHz carrier recovery with Loop filter output response

Implementation Results from ADC-FPGA board with Practical BPSK inputs

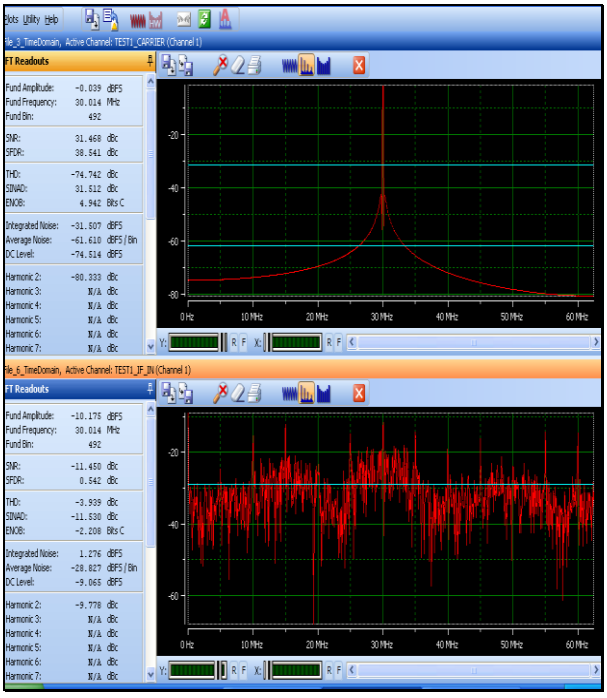

Fig 18: 30.01MHz Modulated input with recovered carrier

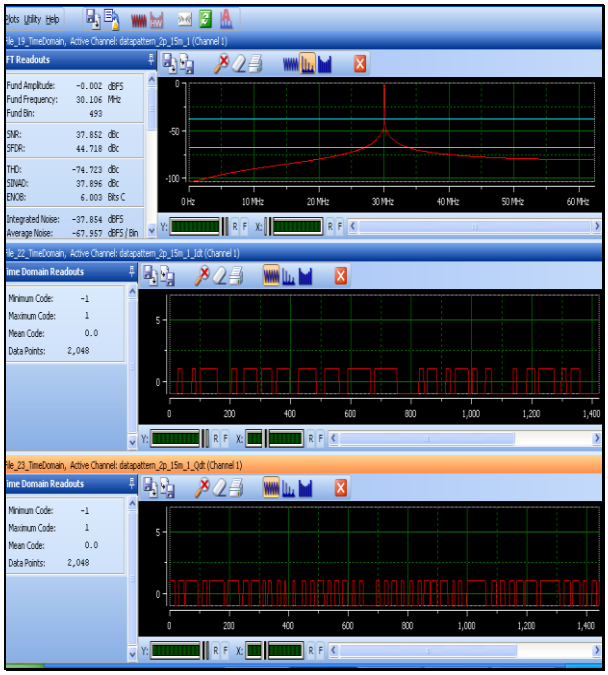

Fig 19: 30.1 MHz modulated input with recovered data pattern

3. CONCLUSIONS

The primary objective of the design is to develop a fully programmable high data rate digital demodulator using VLSI techniques and devices. The high data rate digital demodulator has the capability to demodulate any BPSK/ QPSK signal with a data rate ranging from 8 MBPS to higher MBPS. The design concepts and implementation aspects of a Costas Loop Carrier recovery have been given more emphasis, which have been elaborately discussed in this paper. The Simulations are carried out for a nominal BPSK and QPSK signal with a data rate of 8 MBPS and 42.4456 MBPS (21.2257 X 2) respectively. Further the process of implementing the Digital Costas Loop (DCL) on an FPGA has also been thoroughly discussed. The Costas Loop design is implemented on FPGA and tested extensively in MATLAB and Chip scope for design verification and validation for performance optimizations as required for high data rate applications. The simulation and implementation results show that this whole architecture results in robust and accurate carrier recovery. The Digital Low Pass FIR filter optimizations thereby make it feasible to implement an entire Costas Loop on FPGA.

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