IMPLEMENTATION OF A BIT ERROR RATE TESTER OF A WIRELESS COMMUNICATION SYSTEM ON AN FPGA

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Abstract

*This paper deals with the Field Programmable Gate Array (FPGA) implementation of an entire digital baseband wireless communication system. The proposed BER tester (BERT) integrates the modules of a typical communication system along with an AWGN channel into a single FPGA. The BER is calculated for a 2*2 MIMO system also. This FPGA based solution is a more cost effective, flexible and faster solution compared with the commercially available BER test equipments and software based simulators.*

Keywords— *BER; BERT; MC simulations; FPGA*

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1. INTRODUCTION

Undoubtedly the impact the technology has made on our day to day life in the last two decade or so is clearly overwhelming. With ever increasing demand from customers for better services and increased competition in the market it becomes absolutely vital for the service providers to ensure that their systems are subjected to very stringent performance testing measures. One such most widely used metric for determining the reliability of a digital communication system is the bit error rate (BER).[1][2]

This paper performs the bit error rate validation of a digital baseband wireless communication systems on an FPGA. The proposed BERT integrates the various modules of a communication system like the transmitter, receiver and AWGN channel onto an FPGA. The system performance will also be evaluated for a 2/2 antenna system. The transmitter side includes the rate 1/3 convolutional encoder, puncturer, interleaver and 16 QAM modulator .The receiver includes the ML detector, demodulator, deinterleaver, depuncturer, and Viterbi decoder. The output will be exported to MATLAB to plot the BER curve. The rest of the paper is organized as follows. Section II describes the literature survey, Section III contains the overall block diagram and the design details of all the implemented modules. Section IV shows some simulation results.

2. LITERATURE SURVEY

Any digital transmission system which transmits a series of bits over a communication channel is likely to get influenced by some errors due to various factors like noise, interference etc. We need to ensure that these errors are reduced to a minimum so as not to interfere with the working of the measurements of BER on the test system. BER is a measure of how effective the system is and indicates the number of bit errors introduced in the received message. BER Testers are used to measure this value. These measurements can be done using either the software based simulations like the MC (Monte Carlo) simulations and IS (importance sampling) or using the hardware based prototyping. The various problems encountered with the existing methods are as follows.[2][3][8]

- The MC simulations are not suitable for communication systems with low BER, the reason being the fact errors introduced are less, indicating simulations need to be run for a longer duration to be able to attain these BER.[4]
- The fading channel simulators which are used in the laboratories to replicate the channel are highly costly and not very accurate. They can also not be scaled to emerging new standards in the communication field.[1][5]
- The MC based simulations when done on a simple AWGN channel takes lesser time when compared to that for a fading channel. In reality most of wireless communication systems have fading characteristics which takes longer run times for the simulations to estimate the BER.[3]
- For a MIMO channels, the simulation time also is high as the receiver is highly complex and a lot of possible configurations in terms of the available coding schemes, channel, modulation techniques need to be explored before arriving at the optimum one.[3]
- The BER of a reliable communication link should be very low .For example IEEE 802.3 10 GB/sec Ethernet should have a BER of the order of $10^{(-12)}$).It means a single error occurs in approx. $10^{(12)}$) samples. This indicates that a very large number of symbols need to be processed for software based simulators, over different SNR ratios to obtain a reliable performance

measurement .Thus the simulation time can get extended to months.[3]

- We go for a hardware based prototyping, as it is much faster than software based simulations. Some of the BERT available in the market are from various companies like Data Communications Business Inc. (DCB), Tektronix, Picosecond Pulse Labs etc. The drawback of such equipment is the fact that they are not scalable. Also it can be used for testing the system designed only at a later stage, after which a lot of reworks needs to be done if the expectations are not met. Also there is an additional burden of designing the custom interfaces for each of the equipment and communication systems under test.[6]
- Most of the published BERT uses FPGA and Simulink to integrate the Forward Error Correction (FEC) blocks onto FPGA. Although use of Simulink reduces the need for having an extensive knowledge of the hardware, it has limited resources in its simulation library which may not be able to keep pace with emerging standards [6].
- The alternate proposed is where the entire communication system can be integrated into an FPGA along with the channel. The speedy calculations are made possible by the parallel circuitry of FPGA .Also the memory bandwidth of FPGA is high. These two features along with flexibility make it a highly likely candidate for implementing a BERT.[8]

3. PROPOSED SYSTEM

The block diagram of the proposed communication system is as given in figure1.The implementation has been done using Verilog HDL in Xilinx ISE 12.2 and simulated using the iSim simulator M.(63C).

- Convolutional Encoder: The source bit data is given at the input of the encoder. The encoder used is a rate 1/3 convolutional encoder, which is capable of performing forward error correction. It differs from the block coding in its encoding principle. In convolutional codes, the information bits are spread along the sequence. Hence it maps the information to code bits not block wise, but sequentially convolve the sequence of information bits according to some rule .The encoder has been implemented using 6 bit shift registers. For every data input, 3 coded bits will be generated. The simulation result is given in figure 3.

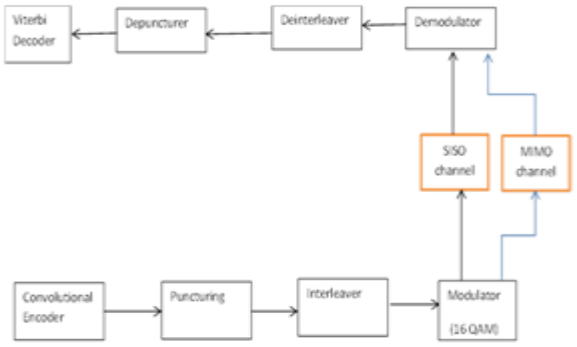

Fig 1: Block diagram of implemented communication system

- Puncturer: The 3 bit output of encoder is fed to a puncturer, where some of the output parity bits of the encoder are deleted as per the puncturing matrix. This has the same effect as encoding with an error-correction code with a higher rate, or less redundancy. Since the same decoder can be employed for decoding, it considerably increases the flexibility of the system without significantly increasing its complexity .Using different puncturing schemes we can adapt to the channel, ie using the channel state information, send more redundancy, if the channel quality is bad and send less redundancy (more information) if the channel quality is better. We have used a 13 bit puncturing matrix. The simulation result is given in figure 4.
- Interleaver: The three bit output of puncturer is given to an interleaver to reduce the burst errors. If the number of errors within a code word exceeds the error-correcting code's capability, it fails to recover the original code word. Interleaving ameliorates this problem by shuffling source symbols across several code words, thereby creating a more uniform distribution of errors. The interleaver concept is implemented using two temporary 50 bit registers and counters. The data is written sequentially into these locations specified by the incrementing counter. At the other end, the data at locations specified by a specific logic is taken out. Simulation details are given in figure 5.
- Modulator: The three bit output from the inter leaver is appended with a zero to make it 4 bits, which is then mapped to signal constellation as specified by figure 2 using the 16 QAM modulation techniques. The 4 bit data is mapped into an in phase and quadrature component, each 16 bits. Simulated results are given by figure 6.The entire transmitter has been simulated using figure 7.
- Demodulator: The received signal through the channel is demodulated using the reverse process, where the 4 bit data is recovered. Simulated results are given in figure 8.

- Deinterleaver: Here the reverse operation of the interleaver takes place. The simulation results are given in figure9.

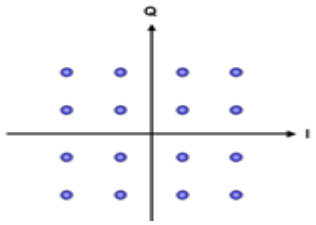

Fig 2: 16 QAM signal constellation

- De puncturing: The same puncturing matrix is used at the receiver side. De puncturing just introduces dummy bits. The simulated result is given in figure 10.
- Viterbi decoder: The three bit output of the depuncturer is fed to Viterbi decoder. There are three different parts to a Viterbi decoder. They are the path metric unit (PMU) which contains the Add Compare Select (ACS), the branch metric unit (BMU) and the survivor memory management unit. The block diagram of the basic Viterbi decoder is shown in figure 3.The first branch metric unit compares the received data symbols with the ideal output of the encoder at transmitter side. A hard decision decoding is performed using hamming distance as the metric. The path metric unit calculates the path metric by adding the branch metric associated with the received symbols with the path metrics from the previous stage. The last stage is the register exchange or the trace back unit, where the survivor path and the output data are identified. The simulated result of the Viterbi decoder is shown in figure 12 and the integrated receiver in figure 13.[7]

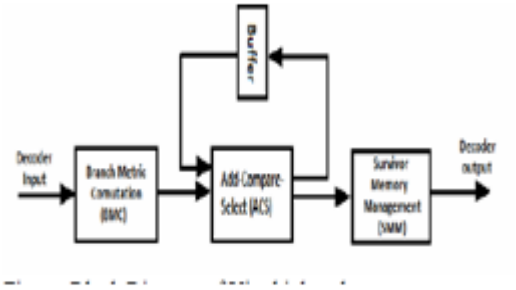

Fig 3: Block Diagram of Viterbi Decoder

4. SIMULATION RESULTS

The coding has been done using Verilog language in Xilinx ISE 12.2 and simulated using ISim Simulator.

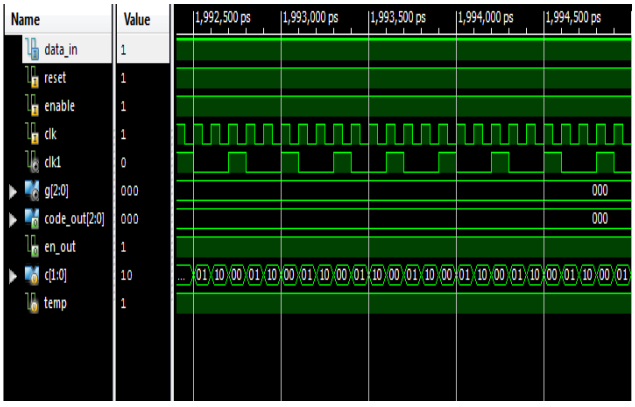

Fig 4: Simulation result of a rate 1/3 convolutional encoder

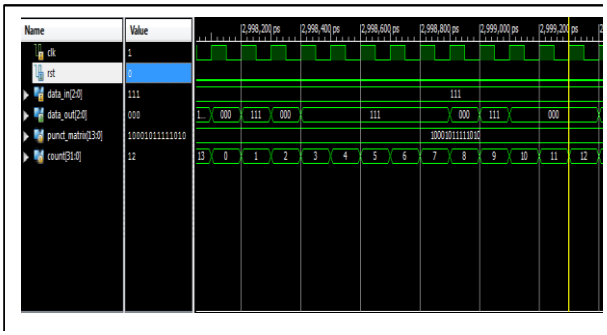

Fig 5: Simulation result of puncturer

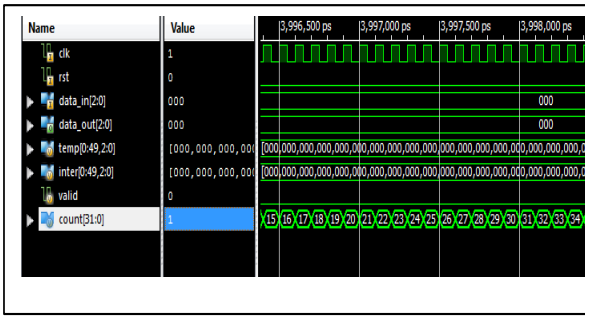

Fig 6: Simulation result of interleaver

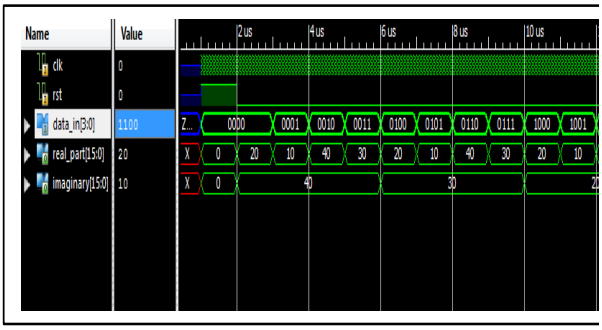

Fig 7: Simulation result of 16 QAM modulator

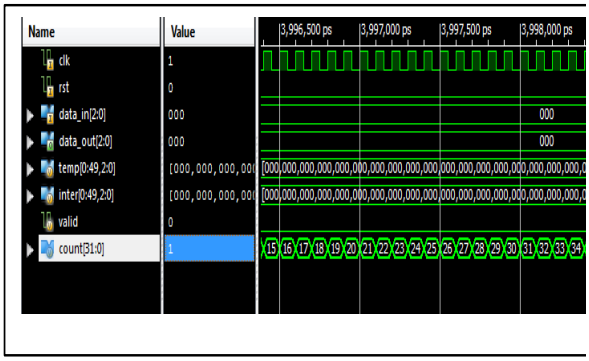

Fig 8: Simulation result of the integrated transmitter

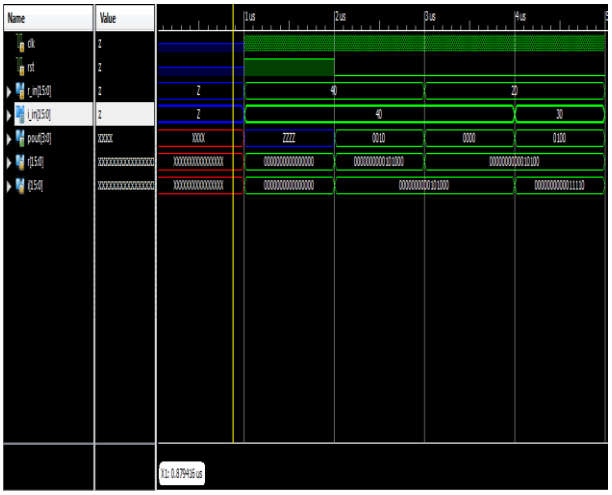

Fig 9: Simulation result of demodulator

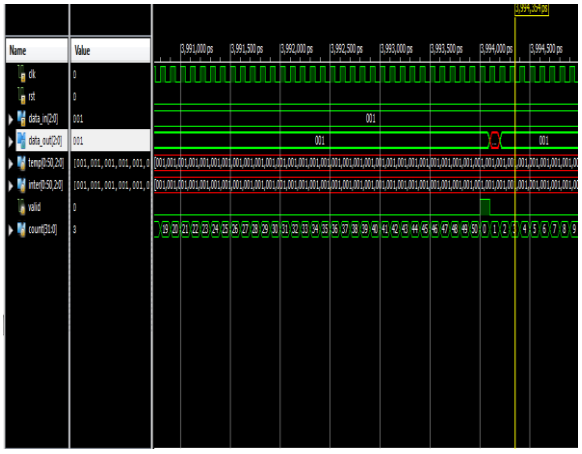

Fig 10: Simulation result of deinterleaver

Fig 11: Simulation result of de puncturer

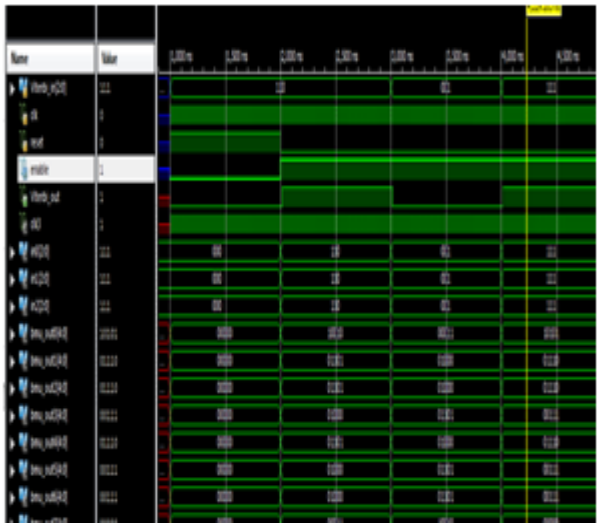

Fig 12: Simulation result of Viterbi decoder

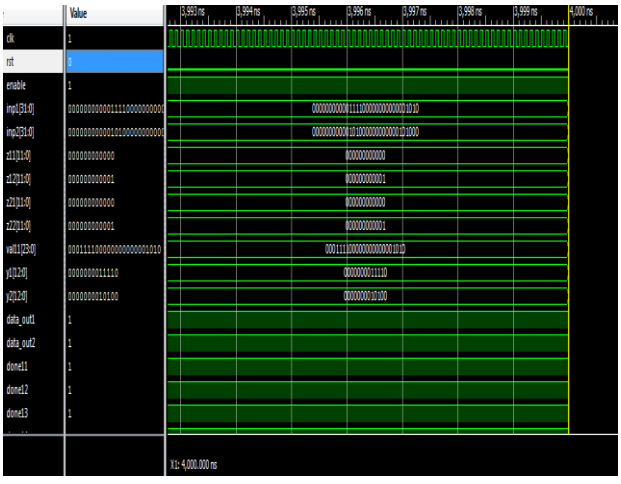

Fig 13: Simulation result of integrated receiver

5. CONCLUSIONS AND FUTURE SCOPE

The FPGA based BERT is a flexible and cost effective solution compared to the conventional bit error rate measurement techniques. The transmitter and receiver have been completely simulated successfully.

As an extension to the project, Verilog coding for different coding schemes and different modulations may be put on FPGA.A user friendly GUI may be developed through which the parameters of the BERT can be altered, as per choice. The main advantage of this BERT is the flexibility that it offers in terms of scalability to the new emerging technology standards and thus poses a very cost friendly and effective method.

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