CMOS ACTIVE PIXEL DESIGN USING 0.6 μm IMAGE SENSOR TECHNOLOGY

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Abstract

This paper describes the Complementary Metal Oxide Semiconductor (CMOS) Active Pixel Sensor (APS) that has become a huge demand for imaging systems because of a better picture quality, low cost, low power consumption and lesser noise as compared with the features of charged coupled devices (CCDs). In this paper, we have designed a CMOS Photodiode APS in 0.6 µm technology that has a lower voltage and noise reduction capability for the pixel. Simulation results with PSPICE and schematic design are presented and discussed. The measured voltage swing at the output for the APS design is 0.47 V to 3.04 V for the supply voltage of 3.3 V and the calculated conversion gain is 5.24590 µV/e. The total capacitance has calculated by simulation result is 30.50 fF. Lastly, we concluded with a description of some applications and opportunities for the CMOS APS.

Keywords: *CMOS APS, Photodiode APS.*

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1. INTRODUCTION

In modern days, Image sensors are an important factor in many image sensing and capture applications. The trend for new markets are based on digital cameras, webcams, computer based videos, smart toys, mobile phones cameras, and in many scientific applications. In past, before 1960, image sensor was fully based on film photography and vacuum tube. But during 1960, solid state image sensor was introduced with varying degrees of success using nMOS, pMOS and Bipolar Process [1]. With the growth of technology, CCD was invented during the period of 1960 to 1975 and CCD was commercialized in 1975 to 1990. In present generation, the widely used CCD sensors are being replaced by the existing CMOS APS which are characterized by reduced pixel size, give fast readouts and reduced noise. Due to these developments and applications, CMOS APS designs are challenging the saturated and matured technology of CCD sensors.

There are different types of CMOS APS designs presented such as: 1) Photodiode APS, 2) Photo gate APS, 3) Log-Photodiode APS, and 4) P-I-N Photodiode APS. In this article, after examining various types of APS, we present an approach for Photodiode APS using CMIOS technology. Based on the technology scaling, the current state-of-the-art of CMOS APS has a very low-power and low-voltage operations and is suitable for integrating low-cost camera-on-a-chip [2-5]. The design of the photodiode APS is implemented using PSPICE tool and its simulation results is also included in this paper.

2. IMPLEMENTATION OF PHOTODIODE APS

The schematic view of a basic photodiode APS is shown in Figure 1. It contains a photodiode, which is used for sensing light, three NMOS transistors i.e. the reset transistors (M1), a source follower transistor (M2) acting as a buffer transistor and a row select transistor (M3) [6-8]. When light falls on the photodiode [9] it gets converted into charge and the charge gets converted into voltage at the sensing capacitor of the photodiode only when the reset transistor is OFF. So, the photodiode can only be reset by $V_{DD} - V_{TR}$ voltage (where V_{TR} is the threshold voltage of M1 and V_{DD} is the supply voltage).

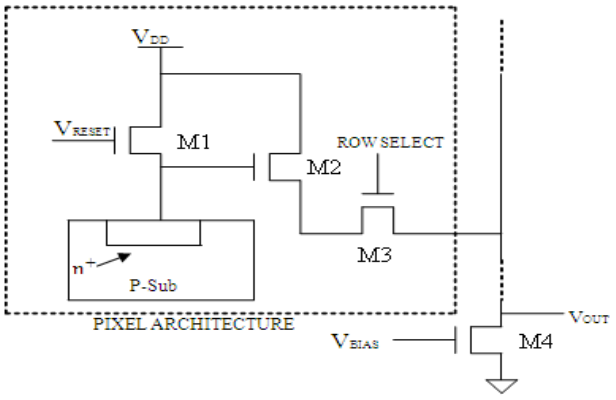

Fig-1: Structure of single CMOS photodiode APS

The voltage is passed to the source follower transistor which acts like a buffer amplifier. The source follower transistor is used at each and every pixel so that the fill factor is kept high and the pixel to pixel variation is reduced. The output is taken only when the row select transistor is enabled. The total photodiode capacitance includes the diode itself, the source of M1 and the gate of M2. The voltage swing is,

$$V_{BIAS} - V_{TL} \langle V_{OUT} \langle V_{DIODE} - V_{TS} - V_{TR} \quad (1)$$

Where, V_{TS} is threshold voltage of M2, V_{TL} is the threshold voltage of M4 (Bias transistor) and $V_{DIODE(\max.)} = V_{DD} - V_{TR}$

$$\text{If,} \quad V_{TS} = V_{TR} = V_T \quad (2)$$

Then the maximum output voltage can written as,

$$V_{OUT(\max)} = V_{DD} - 2V_T \quad (3)$$

For the design of the APS we have taken the same value of length (L) as 0.6 µm, width (W) as 4 µm for the all transistor, $V_{TR} = V_{TS} = V_{TL} = 0.13$ V and $V_{TRS} = 0.5$ V, where V_{TRS} is the threshold voltage of M3.

3. CIRCUIT DESIGN AND RESULTS

3.1 Photodiode Design

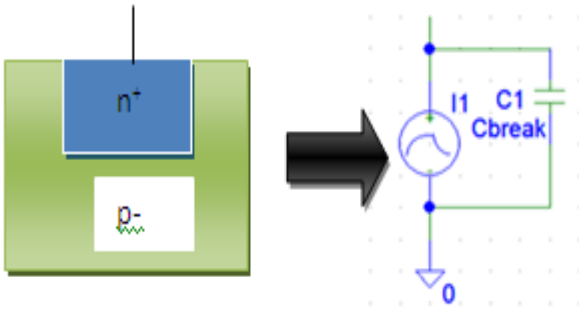

Fig-2: Schematic view of photodiode

For designing the photodiode, an exponential variation of current source I1 (shown in Fig. 2) is used which follows the similar behavior as photodiode and capacitor C1 is used for storing the charge. The current is generated due to the quantum efficiency and properties of photodiode [10]. We have considered the number of collected electrons as 4×10^5 with the area of the photodiode as 9 µm^2 and the integration time as 6 ms. The given equation will help in calculating the value for applied equivalent current source (i_p).

$$Q = nq = i_p t \Rightarrow i_p = \frac{nq}{t}$$

This is 10.66 pA. The total capacitance (photodiode capacitance + reset capacitance + buffer capacitance) has calculated by simulation result is 30.50 fF.

3.2 Reset Transistor Design

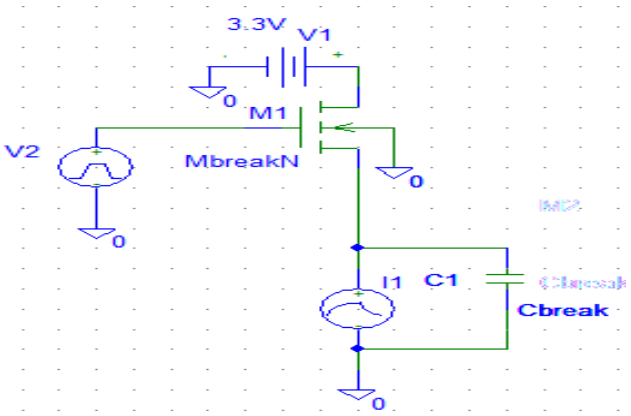

Fig-3: Schematic view of Reset Transistor

The reset transistor M1 is used to reset the charge on the photodiode. When the reset transistor is on, the charge of the photodiode is stored and when it is off, the transmission of charge i.e. voltage takes place. For the design (shown in Fig. 3) of the transistor we have calculated the oxide capacitance (C_{ox}) as 9.37×10^{-8} F, gate capacitance C_G as 2.25×10^{-19} F, the gate to source capacitance (C_{GS}) as 0.00015 fF and the drain current (I_D) as 2.03×10^{-11} A .

3.3 Source Follower Transistor Design

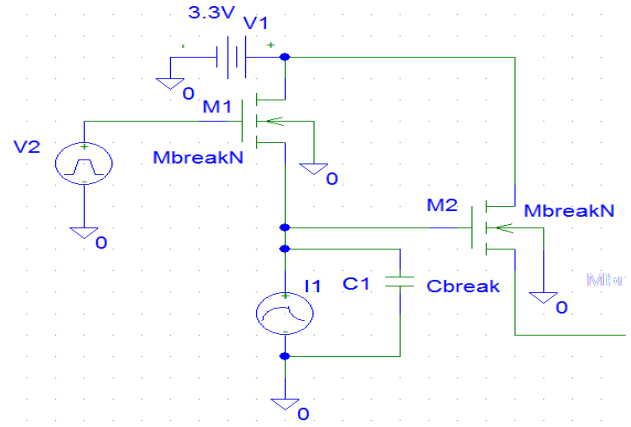

Fig-4: Schematic view of Source Follower Transistor

The Fig. 4 shows the source follower transistor M2 which behaves like a buffer amplifier. Once the charge to voltage conversion is done, the sensed voltage is transmitted to the

source follower transistor. For the implementation and design of the transistor we got the value of C_{ox} is 3.07×10^{-8} F, C_G as 2.25×10^{-19}, I_D as 5.38×10^{-5} A and the value of $V_{DIODE} - V_{TS} - V_{TR} = 3.3 - 0.13 - 0.13 = 3.04V.$

3.4 Row Select Transistor Design

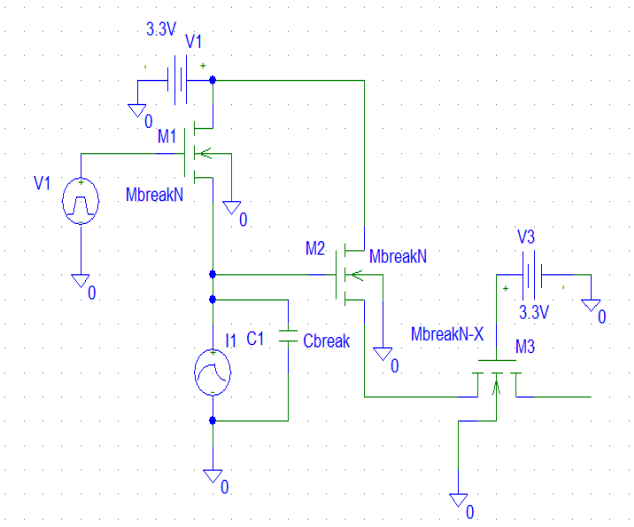

Fig-5: Schematic view of Row Select Transistor

Fig. 5 shows the schematic view of the row select transistor. It acts like a pass transistor. When the row select transistor is enabled, the data will be read out. It is shared by all pixels in the array on the same row and it selects the data of one pixel at a time from a single row.

3.5 Bias Transistor Design

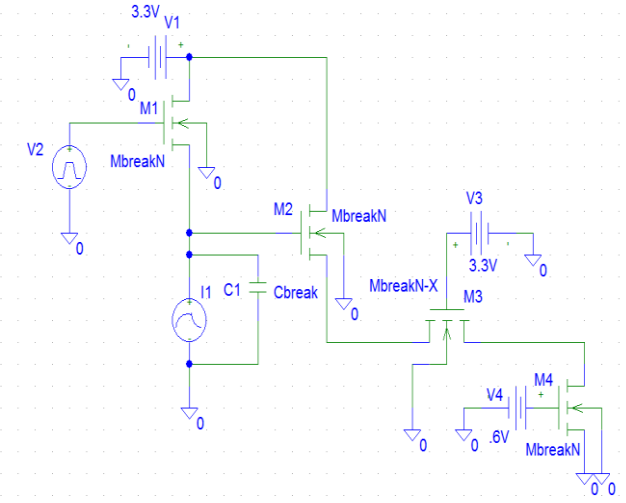

Fig-6: Schematic view of Bias Transistor

The bias transistor M4 is not part of the pixel itself but is shared by all pixels in the array on the same column which is shown in Fig. 6. This figure is also showing the overall schematic diagram for the CMOS APS design. Transistor M4 selects the data of one pixel at a time from a single column. A constant voltage source is applied to the transistor by applying a bias voltage V_{BIAS} to the gate. The output is taken from the drain of M4. So, $V_{BIAS} - V_{TL} = 0.6V - 0.13V = 0.47V.$

3.6 Results & Discussion

The measured voltage swing at the output for the APS design is,

$$V_{BIAS} - V_{TL} \langle V_{OUT} \langle V_{DIODE} - V_{TS} - V_{TR}$$

$$0.47V \langle V_{OUT} \langle 3.04V$$

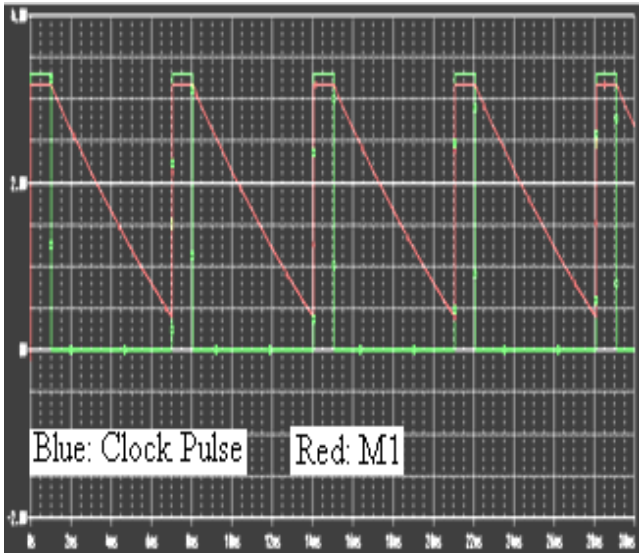

Fig-7: Output waveform for Clock Pulse and Reset Transistor

Fig. 7 shows the simulation result at the gate and source of the reset transistor. The green color shows clock pulse applied at the gate of reset transistor which is at a maximum voltage of 3.3 V having a pulse width of 1 ms and period of 7.02 ms. The red color shows the pulse obtained from the source of the reset transistor. The pulse is being decremented by 0.13 V and is at a maximum voltage of 3.17 V. The pulse width remains the same but instead of the fall time the pulse gets decreased exponentially due to the discharging of capacitor with time. It gets discharged until the charge is over and gets ready for the next clock pulse where the charge gets again accumulated in the capacitor and the process is repeated.

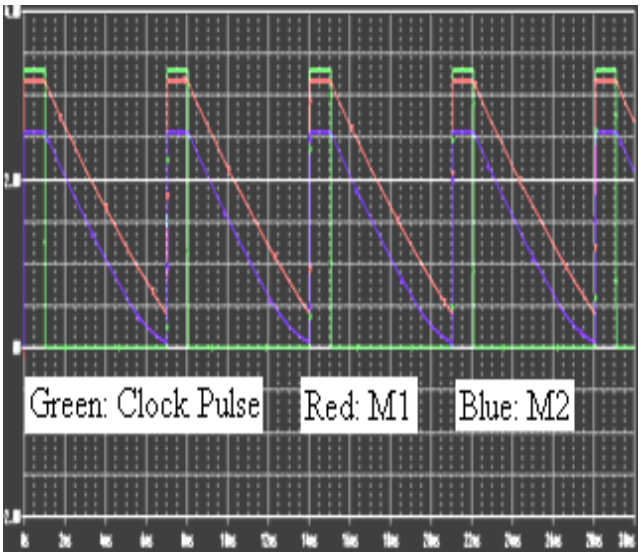

Fig-8: Output waveform for Clock Pulse, Reset Transistor and Source Follower Transistor

The blue graph form Fig. 8 shows the output voltage of source follower transistor i.e.M2 obtained from the source of M2. The pulse is again decremented by 0.6 V and has a maximum voltage of 2.57 V. Here once again the simulated output waveform is decreasing with time due to same reason of earlier transistor condition.

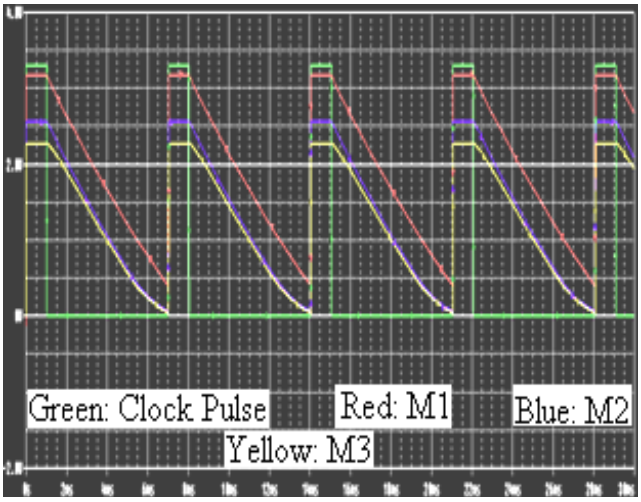

Fig-9: Output waveform for Clock Pulse, Reset Transistor, Source Follower Transistor and Row Select Transistor

The yellow graph shows (shown in Fig. 9) the output voltage of row select transistor i.e. M3 obtained from the drain of M3. The same pulse passes through it as it acts like a pass transistor. The pulse is also decremented by 0.3 V and has a maximum voltage of 2.28 V. The calculated conversion gain is 5.24590µV/e for the APS design.

4. CONCLUSIONS

CMOS sensor technology has an excellent performance for the new generation of sensors. CMOS sensor also has a better utilization as compared to CCD. Due to its less cost effective imager with small pixel sizes, it has a variety of application such as in mobile cameras, digital cameras, webcams and many commercial and scientific applications. Here, we have designed the photodiode active pixel sensor using 0.6 µm CMOS process and discussed the simulated/calculated design values of it.

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BIOGRAPHIES

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Reshmi Maity: Assistant Professor of the Department of Electronics & Communication Engineering, Mizoram University (A Central University, Govt. of India), India since 2008. She is the author of more than 25 international journal / conference papers in repute. She has good teaching and research experience in the field of MEMS, Microelectronics and Analog & Digital Communication She is currently working with VLSI Design and MEMS