# GAIN IMPROVEMENT OF TWO STAGE OPAMP THROUGH BODY BIAS IN 45nm CMOS TECHNOLOGY

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## Abstract

*Gain is an important parameter of an operational amplifier which decide accuracy and speed of it. Number of design techniques (gain boosting, cascoding, cascading etc.) available, which may improve gain of an OPAMP. This paper includes body bias technique to improve gain, thereby speeds up operation of an OPAMP. Technology scaling doesn't have much impact on threshold voltage of transistor which leads to reduced DC gain of an OPAMP, thereby slowdown their operation. Body bias technique cross the barrier of threshold voltage limitation of technology scaling, hence OPAMP exhibits improved DC gain. The proposed OP AMP having DC gain of 57.83 dB which is 5dB more than classical OP AMP design using transistor pair Unity gain bandwidth is 74 MHz. The op amp is designed in 45nm CMOS technology; simulation and result were carried out in Cadence with 1.3V power supply.*

***Keywords:*** *Body bias, Pseudo Cascode compensation, and Transistor pair*.

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## 1. INTRODUCTION

High speed analog and mixed signal design require high DC gain. There is an intrinsic performance trade-off between bandwidth and gain while designing an OPAMP. Maximum gain of an OPAMP is obtained by stacking (cascoding) or cascading of stages, operating at minimum bias current. Gain improvement by cascoding approach degrades the output voltage swing. Modern design technique with low supply voltage results in reduction of output voltage swing. However, cascading of amplifier stage, enhance the output signal swing at the cost of phase margin (stability) [1]. Gain of an amplifier, is related to two parameters output impedance ($r_d$) and transconductance ($g_m$).

$$\text{Gain } (A_v) = -g_m r_d \qquad (1)$$

Therefore IC designer have only two choices to improve DC gain, either increase transconductance ($g_m$) or output impedance ($r_d$) [2]. This paper presents body bias technique to improve DC gain of two stage op amp by increasing output impedance as well as transconductance. Design technique uses self bias circuitry to provide biasing. Compensation technique pseudo cascode is being implemented to resolve the stability issue of OPAMP.

## 2. APPROACH TO GAIN IMPROVEMENT

This section introduces body bias technique and their effect on transistor pair:

### 2.1 Body Bias

The bulk or body is common to many MOS transistors and is connected to the most negative (positive) supply for NMOS (PMOS) transistors. Such connection reverses biases source bulk and drain bulk junction which is essential for the proper operation of MOS [2].

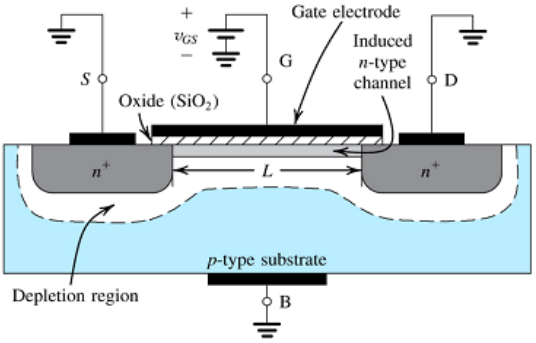


**Fig - 1:** Structure of NMOS transistor without body bias

Body effect exists, if potential at the body (B) is somewhat different from the source(S), MOS continues to work properly but some of its characteristics may change. To understand the effect properly, a negative potential is applied to the body which attract more holes to the substrate connection is given in the Figure 2. As a result depletion region becomes wider. Since threshold voltage is function of total charge in the depletion region.

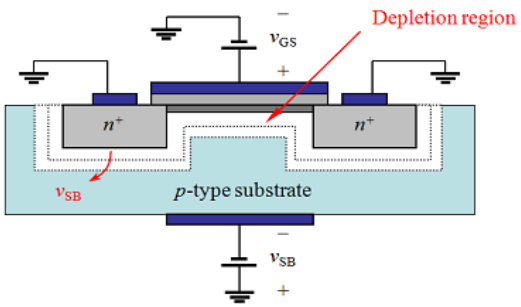


**Fig – 2**: Structure of NMOS transistor with body bias

Thus threshold voltage ($V_t$) is increased by applying negative potential to the body in accordance with the relation:

$$V_t = V_{t0} + \gamma \left[\sqrt{2\phi_f + V_{SB}} + \sqrt{2\phi_f}\right] \quad (2)$$

Where $V_{t0}$ is the threshold voltage when $V_{SB}$ = 0, $\Phi_f$ is a physical parameter, $\gamma$ is a fabrication process parameter.

$$\gamma = \frac{\sqrt{2qN_A\epsilon_{si}}}{C_{ox}} \quad (3)$$

The supply voltages are reducing while threshold voltages are remaining relatively constant due to continuous evolution of CMOS technology. As a result reduced gain is achieved from CMOS technology. IC Designer applies body bias to MOS in order to reduce the threshold voltage of MOSFET and achieve high gain [5].

## 2.2 Transistor Pair

Transistor pair is combination of two transistors $M_a$ and $M_b$, whose gate are tied together. Channel length of each transistor $M_a$ and $M_b$ in transistor pair is 45nm, where as width may vary to each other.

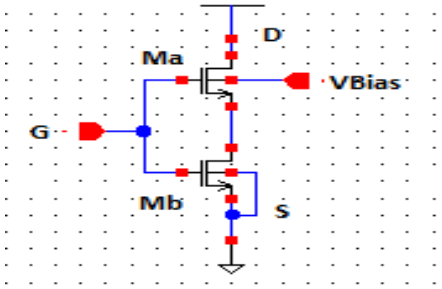


**Fig – 3**: Schematic of Transistor pair with body bias

In case of NMOS transistor pair, transistor $M_a$ operates in saturation region while $M_b$ in triode. As bias voltage ($V_{Bias}$) is applied to the body of $M_a$ its threshold voltage ($V_{THa}$) dropped, resulting gate to source voltage ($V_{GSa}$) of $M_a$ increased. Drain to source voltage ($V_{DSb}$) of $M_b$ is increased due to increment in $V_{GSa}$, which drive transistor $M_a$ from triode to edge of saturation region, hence output impedance of transistor pair is increased. Similarly, output impedance of PMOS is increased by applying suitable bias voltage to body of transistor $M_a$ of transistor pair.

## 3. COMPANSATION TECHNIQUE

Transistor mismatch and temperature variation affects the stability of an OPAMP, therefore to make it stable a compensation network (pseudo cascode) is added in between input stage and output gain stage of an op amp. In pseudo cascode compensation, a single capacitor $C_c$ is splited in two halves, one half $C_{c/2}$ is attached to the node N1 of cascoded input transistor M2, while second half $C_{c/2}$ is attached to node N2 of cascoded load transistor M3.Since transconductance($g_m$) of all transistor of an op amp is deduced from single bias current $I_{BIAS}$ ,hence pole/zero frequency will be proportional to bias current $I_{BIAS}$. Transistor mismatching or temperature variation alters the bias current $I_{BIAS}$, does not affect the ratio of pole/zero frequency, hence stability in OPAMP is achieved. Compensation technique mostly used to resolve stability issue of an OPAMP whose dominate pole /zero frequency depends on short circuit transconductance [4,7]. A pole placed at an appropriate low frequency in the open-loop response reduces the gain of the amplifier to one (0 dB) for a frequency at or just below the location of the next highest frequency pole. The pole exists at lower frequency is known as dominant pole because it affects the pole existing at higher frequency.

## 4. TWO STAGE OPAMP WITHOUT BODY BIAS

The p channel differential amplifier with NMOS current mirror load serve as input stage where as current source inverter acts as output stage in two stage OPAMP.

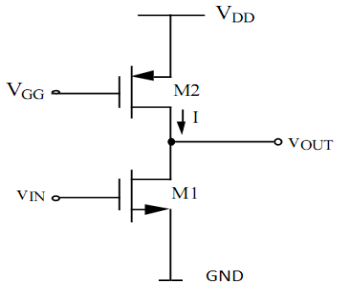


**Fig – 4**: Schematic of Current Source Inverter [3]

From small signal analysis, voltage gain of current source inverter is given by:

$$V_{OUT} / V_{IN} = - g_m / (g_{ds1}+g_{ds2}) \quad (4)$$

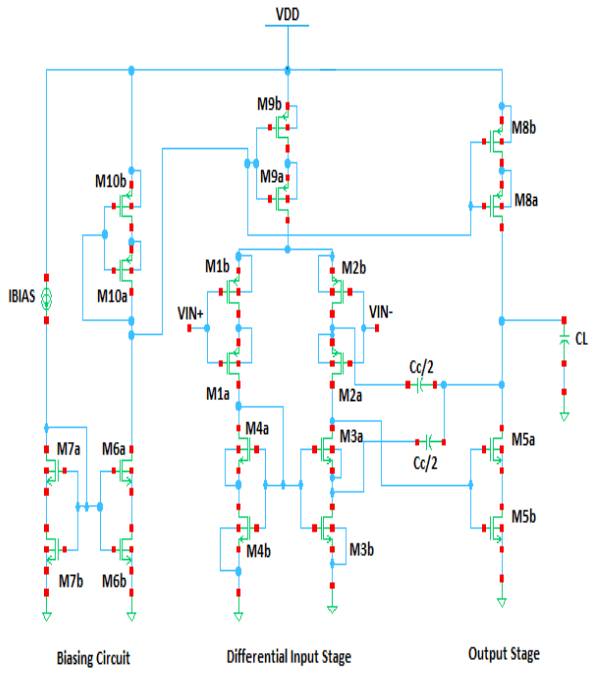


**Fig – 5:** Schematic of Two stage OPAMP without body bias

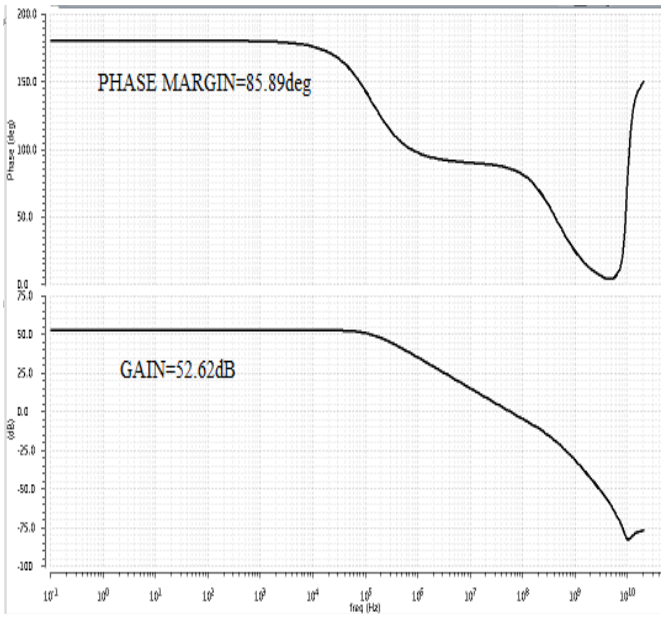


**Fig – 6:** Gain and Phase plot OPAMP without body bias

## 5. SUGGESTED TWO STAGE OPAMP WITH BODY BIAS

Body bias technique discussed in above section 2.1 is applied in suggested two stage OPAMP. Biasing network generates biasing voltage $V_{BAISn}$ and $V_{BAISp}$ which provide biasing voltage to transistor $M_{Xa}$(X=1 to 7) and $M_{Ya}$(Y=8 to 10) respectively. Bulk biasing moves $M_{Xb}$(X=3 to 7) and $M_{Yb}$(Y=1,2,8,9,10) from linear to point of saturation region, Hence transistor pair exhibit high output impedance and transconductance ,thereby overall gain of an OPAMP is improved.

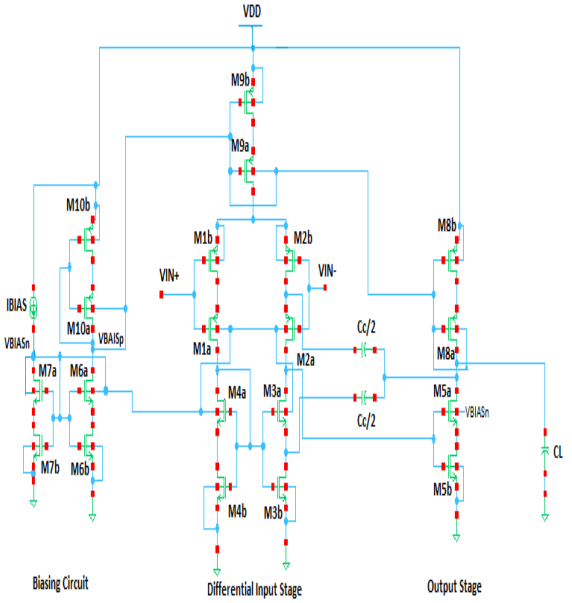


**Fig- 7:** Schematic of Two stage OPAMP with body bias

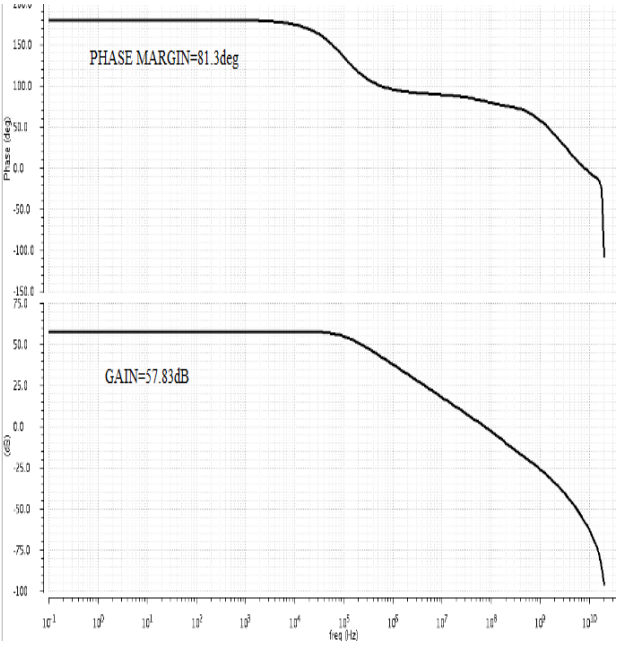


**Fig – 8:** Gain and phase plot of two stages OPAMP with body bias

## 6. SIMULATION RESULTS

In this paper two stage op amp has been simulated using 45nm CMOS technology in CADENCE VIRTUOSO platform with an power supply of 1.3v. The parameters such as width of MOSFET in both OPAMP is different from other OPAMPs, but compensation capacitors having same value in both of the design. Taking all these parameters into consideration a desirable results were obtained which is shown in below Table1.

**Table – 1:** Simulation Result of Two Stages OPAMP With and Without Body Bias

| **Parameters** | **OPAMP without Body Bias** | **Suggested OPAMP with Body Bias** |
|---|---|---|
| Supply Voltage (V) | 1.3 | 1.3 |
| DC Gain (dB) | 52.62 | 57.83 |
| Phase Margin | 85.89 | 81.3 |
| UGB(MHz) | 58 | 74 |
| Power Consumption (μw) | 42.82 | 42 |
| Output Voltage Swing (V) | 1.2 | 1.2 |
| Compensation Capacitor $C_c$ (pF) | 0.1 | 0.1 |

## 7. CONCLUSIONS

Settling behavior of analog and mixed signal devices determines the speed and accuracy of the circuit. Fast settling and High accuracy needs maximum DC gain and maximum unity-gain frequency. DC gain achieved by suggested bulk biasing two stages OPAMP is 57.83db, which is 5dB more than op amp without bulk biasing. The unity gain bandwidth achieved is 74MHz.The trade off is slight decrease in phase margin. The OPAMP is designed in 45nm CMOS technology; simulation and result were carried out in Cadence with 1.3V power supply. Improved DC gain of proposed two stages OPAMP improves its settling behavior and accuracy.

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