PERFORMANCE ANALYSIS OF SWCNTs BUNDLES AND MWCNT INTERCONNECTS FOR SUBTHRESHOLD CIRCUITS

Anil Kumar[1], Prashant Gupta[2], Chandresh Kumar Sharma[3]

[1]*Electronics & Communication Engineering Department, National Institute of Technology, Hamirpur (HP), India*
[2]*Electronics & Communication Engineering Department, National Institute of Technology, Hamirpur (HP), India*
[3]*Electronics & Communication Engineering Department, National Institute of Technology, Hamirpur (HP), India*

Abstract

In this paper present the performance analysis of two possible realizations of a CNT-based nano-interconnect, namely one obtained by using a bundle of SWCNT and another one employing an MWCNT and their applicability as interconnects in nanoscale integrated circuits in subthreshold regime. The time delay, power dissipation and power delay product of SWCNT bundle and MWCNT interconnect configurations are derived and compared to those of the copper (Cu) wire counterparts for the intermediate and global interconnects for three different technologies (32-, 22- and 16nm). It is observed that, compared with the Cu, and SWCNT bundle the MWCNT interconnect can lead to a reduction of all above three parameters and it becomes more significant with increasing interconnect length. Because of considerable improvement in Power Delay Product MWCNT interconnect will be more suitable for the next generation of interconnect technology as compared with the SWCNT bundle and Cu counterpart in subthreshold regime also.

Keywords—*carbon nanotube (CNT), power-delay-product(PDP), equivalent-circuit models, multiwall CNT (MWCNT), single-wall CNT (SWCNT)*

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1. INTRODUCTION

In integrated circuits technology scaling is done to incorporate more number of transistors in the same area to increase the functionality and performance of the circuits. However, with technology scaling leakage power dissipation increases significantly [1]. For ultra-low power applications like mobiles, wireless sensors, body based sensors, and implanted medical electronics less power should be used to increase the battery life. So ultra-low power devices uses sub threshold design to achieve low power. In sub threshold the supply voltage is reduced below the threshold voltage so that they use less power to operate. Due to low supply voltages the performance of the devices is reduced. This reduction of performance is caused by increased delay of the circuits at low voltages. The delay is increased because of the scaling down of the device parameters. The region in which they are operating defines Complementary Metal Oxide Semiconductor (CMOS) circuits' operation. Generally they are operated in super threshold region where the supply voltage V_{dd} is more than threshold voltage V_t. As we reduced the supply voltage near to threshold voltage the circuits operation starts shifting from strong inversion, where we have strong currents, to moderate inversion, as we reduce the supply voltage below threshold voltage V_t the circuit operation shifts to weak inversion where the circuits are driven by small currents. This region where the supply voltage V_{dd} is lower than the threshold voltage V_t and having small current drives is called sub threshold region.

Power saving from sub threshold operation of device is obtained but cost speed significantly .The speed of sub threshold circuits can be enhanced by optimization of the device and/or interconnects. Performance is mainly limited by interconnect in deep submicron [2]. Hence, it is important to investigate and optimize the performance of interconnects in sub threshold application domain.

Carbon nanotubes, which exhibit good electrical and thermal properties, are expected as future nanoscale IC interconnects and have received intensive attention in recent years. Carbon nanotubes can be classified into single-wall carbon nanotubes (SWCNTs) and multiwall carbon nanotubes (MWCNTs). MWCNTs are always metallic and can have lower resistivity than SWCNT bundles for higher interconnect length. Hence, attractive for interconnect applications. There are many studies in considering MWCNTs and $SWCNT_S$ as interconnects in super threshold region [3]–[9]. However, very little progress has been made to investigate carbon nano tubes (CNT_S) as interconnect in sub threshold conditions [10]–[12]. In this paper, we investigate these interconnect in sub threshold region.

In this paper, the various performance parameters (delay time, power dissipation and PDP) are observed for MWCNT and SWCNT bundle interconnects for intermediate and global interconnects. Global interconnects more critical as all the above parameters increases with longer length.

This paper is organized as follows. Section II describes the sub threshold operating region. In Section III, describes the equivalent circuit models of MWCNT and SWCNT bundle, In Section IV, Simulation results and comparison of MWCNT and bundle SWCNT interconnects with conventional Cu interconnect has been discussed. Finally, Conclusions are drawn in Section V.

2. MODEL FOR SUBTHRESHOLD APPLICATIONS REGIME

The sub-threshold operation of a device is defined as the device operating with supply voltage lower than its threshold voltage. The device current is the sub-threshold leakage current which increases exponentially with V_{DS} and V_{GS} given by [15]

$$I_{sub} = I_0 e^{\left\{\frac{V_{GS}-V_t+\eta V_{DS}}{nV_T}\right\}}\left(1-e^{-V_{DS}/V_T}\right) \quad (1)$$

Where, V_t is the threshold voltage, n is the sub threshold slope factor (n = 1+C_D /Cox) [15], C_D and Cox are depletion and oxide capacitances, respectively, "V_T" is the thermal voltage defined as kT/q, where k, T and q are Boltzmann constant, temperature and electron charge respectively. η is drain-induced barrier lowering coefficient that causes an increase in sub threshold current with drain voltage in short channel MOSFET and I_0 is defined as [15] :

$$I_0 = \mu_0 C_{OX} W/L (n-1) V_T^2 \quad (2)$$

Where W and L are channel width and length of MOSFET respectively. μ_0 is the mobility of charge carriers. Due to the exponential variation of the sub threshold current with supply voltage delay increases in sub threshold region.

3. CIRCUIT MODELS OF SWCNT BUNDLE AND MWCNT

3.1 Circuit Model of an MWCNT

For an individual MWCNT with N shells, the resistance of the MWCNT in the equivalent single conductor model can be divided into the lumped part [17]

$$R_l = \left(\sum_{i=1}^{N} R_{l,i}^{-1}\right)^{-1} = \left[\sum_{i=1}^{N}\left(\frac{R_Q}{4n_i} + R_{c,i}\right)^{-1}\right]^{-1} \quad (3)$$

and the per-unit-length (p.u.l.) distributed part [16]

$$R_S = \left(\sum_{i=1}^{N} R_{S,i}^{-1}\right)^{-1} = \left(\sum_{i=1}^{N} \frac{2n_i\lambda_i}{R_Q}\right)^{-1} = \frac{R_Q}{2\sum_{i=1}^{N} n_i\lambda_i} \quad (4)$$

Where R_Q is the quantum resistance for each conduction mode, $R_{c,i}$ is the contact resistance between electrode and tube for the i^{th} shell of MWCNT, n_i is the number of conducting channels of the i_{th} shell, and λ_i is the effective electron mean free path of the

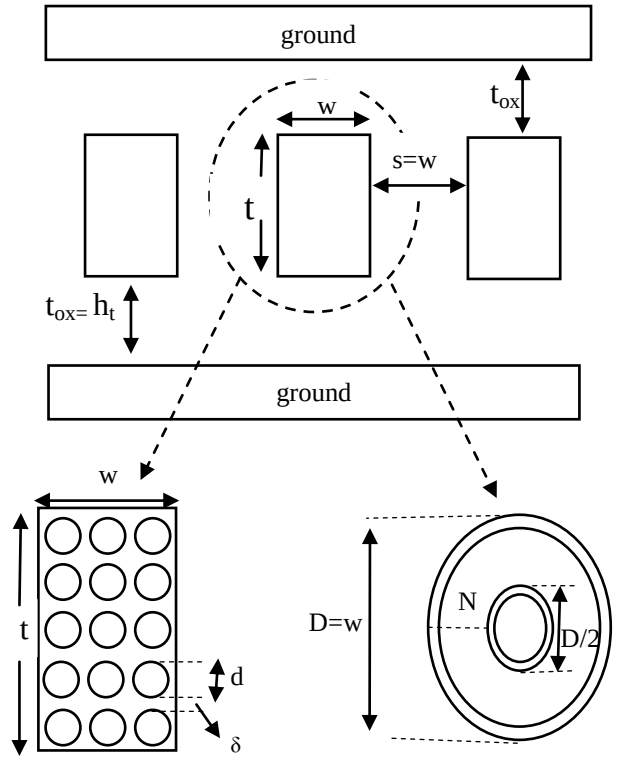

Fig 1 Cross section of a typical interconnect configuration in advanced IC designs. In this figure, the aspect ratio is two. The "interconnect" can be replaced by an equivalent circuit model for MWCNTs, Cu wires, or SWCNT bundles

Table 1: Relevant geometric parameter of the considered structures

Parameter	Description
w	Width of interconnect
t	Height of interconnect
s	Spacing between two parallel wires
d	Diameter of a SWCNT in the bundle
D	Outer diameter of MWCNT
t_{ox}	Dielectric thickness
h_t	Height from the ground
N	Total number of $SWCNT_S$ in the bundle and total number of shells in the MWCNT

i^{th} shell. The number of conducting channels of the i^{th} shell can be expressed as [17]

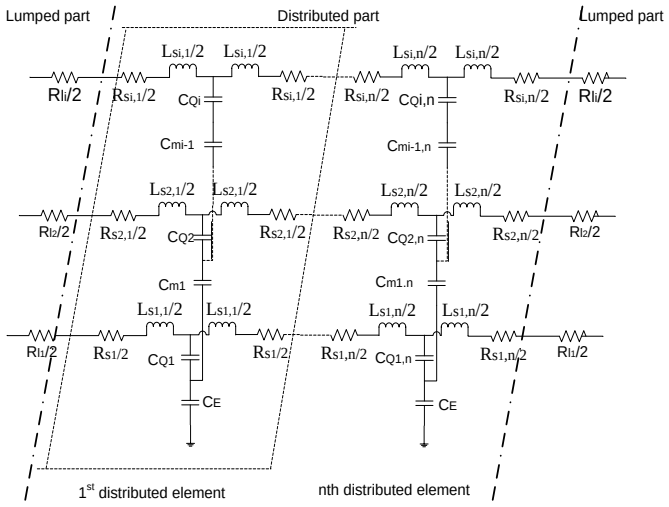

Fig 2 Equivalent-circuit model of a MWCNT

$$n = \begin{cases} aD_i + b, & D_i > 3nm \\ 2/3 & D_i \le 3nm \end{cases} \quad (5)$$

Where, D_i is the diameter of i^{th} shell and a = 0.0612 nm^{-1}, b = 0.425. The effective electron mean free path (mfp) of the i^{th} shell can be obtained as follows [16]

$$\lambda_{mfp,i} = \frac{2\times 10^3 D_i}{\left(T/T_0\right) - 2} \quad (6)$$

The quantum resistance for each conduction mode is given as

$$R_Q = \frac{h}{4e^2} \quad (7)$$

Where h is the Planck constant and e is the electronic charge.

The per-unit-length capacitance in the equivalent single conductor model can be expressed as [16].

$$C = \left(C_E^{-1} + C_Q^{-1}\right)^{-1} \quad (8)$$

Where,

$$C_E^{-1} = \left(\frac{\cosh^{-1}\left[\left(D + 2h_t\right)/D\right]}{2\pi\varepsilon_0\varepsilon_r}\right) \quad (9)$$

$$C_Q = 2\times\frac{2e^2}{h v_F} \cong 193aF/\mu m \quad (10)$$

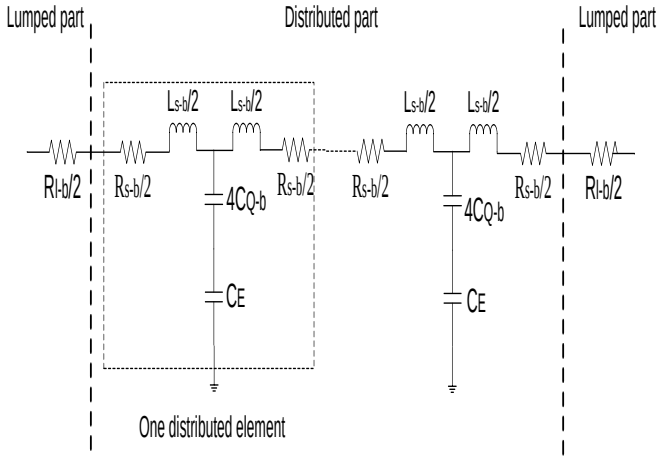

Fig 3 Equivalent-circuit model of an SWCNT bundle

And inter shell capacitance is given by,

$$C_m^{i,i+1} = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{D_{i+1}}{D_i}\right)} \quad (11)$$

The equivalent-circuit model of an MWCNT interconnects for predicting its performance is shown in Fig. 2, where mutual capacitances between shells and quantum capacitances in serial connection. Electrostatic capacitance is connected to outermost shell only.

3.2 Circuit Model of an SWCNT Bundle

The line is realized by means of a bundle of N equally spaced SWCNTs, fixed at the Van der Waals distance δ(.34nm), having the same radius d and in the hypothesis of a perfect hexagonal packed structure with a lattice constant Δ=2d + δ

[17]. If w and t are the interconnect width and height, respectively, the number of SWCNTs along the w and t (see Fig. 1) direction can be expressed as

$$N_w = \frac{(w-d)}{\Delta} \quad (12)$$

$$N_t = \frac{2(t-d)}{\sqrt{3}\Delta} + 1 \quad (13)$$

The number of SWCNTs in the bundle is calculated as follows:

$$N = \begin{cases} N_w N_t - \dfrac{N_t}{2} & if\ N_t\ is\ even \\ N_w N_t - \dfrac{(N_t - 1)}{2} & if\ N_t\ is\ odd \end{cases} \quad (14)$$

Since it is assumed that probability of tubes being metallic is 1 and the N SWCNTs are supposed to have the same number of spineless conducting channels n [17]:

$$n = \begin{cases} ad + b & d > 3nm \\ 2 & d \le 3nm \end{cases} \quad (15)$$

Where a = 0.0612 nm^{-1}, b = 0.425. The total number of conducting channels n_{tot} is given by the sum of the conducting channels of each SWCNT in the bundle; therefore, $n_{tot} = n \cdot N$. The lumped parameter R_l is given by the parallel of the resistances of the N SWCNTs and takes into account the contact resistance of the i^{th} SWCNT, R_{ci}, and the quantum resistance of each conducting channel in every SWCNT, $R_Q = h/2e^2$, where $h = 6.6262 \times 10^{-34}$ J·s is the Planck constant and $e = 1.602 \times 10^{-19}$ C is the electron charge. By assuming Rci =Rc ∀ i = 1. . . N,

$$R_{l-bundle} = \left[\sum_{i=1}^{N} \left(\frac{R_Q}{2n} + R_{ci} \right)^{-1} \right]^{-1} = \frac{1}{N} \left(\frac{R_Q}{2n} + R_c \right) \quad (16)$$

The factor 2 multiplying n takes into account the presence of the two spin orientations per channel. The conduction mechanism taking place in the CNTs is assumed to be ballistic if its length is much shorter than the effective mean free path λ_{mfp} of the SWCNT given by [17]

$$\lambda_{mfp} = \frac{2 \times 10^3 d}{\left(T / T_0 \right) - 2} \quad (17)$$

Unless the interconnect is very short (>λ_{mfp}), its TL model includes the p.u.l. resistances R_S associated with the scattering mechanisms which, under the hypothesis of low bias excitation, can be approximated with less than 10% error by [17]

$$R_{S-bundle} = \frac{R_Q}{2nN\lambda_{mfp}} \quad (18)$$

For a densely packed metallic SWCNT bundle, its capacitance is equal to the capacitance of a metallic wire with the same overall cross section [6]. When the metallic ratio (P_m) in the SWCNT bundle is larger than 0.3 [18], the relative difference in the calculated mutual capacitances (C_m) between the SWCNT bundle and the Cu wire with the same cross section is smaller than 10%, and it continues to decrease with the increasing metallic ratio.

The quantum capacitance C_Q of an individual SWCNT has a typical value of 100 aF/μm, and for an SWCNT bundle, we have

$$C_{Q-bundle} = C_Q \times N \quad (19)$$

The equivalent-circuit model of an SWCNT bundle interconnects for predicting its performance is shown in Fig. 3, where all SWCNTs in the bundle are connected in parallel, with the electrostatic and quantum capacitances in serial connection.

Table 2: structure parameters of interconnects from itrs 2009 [20]

	Parameters	Technology Node		
		32	**22**	**16**
Intermed-iate*and Global interconnect	Wire Width w (nm)	32* 48	22* 32	16* 24
	Height Width Ratio t/w	2* 3	2* 3	2* 3
	Dielectric Thickness $t_{ox} = h_t$ (nm)	54.4* 110.4	39.6* 76.8	25.2* 60
	Effective Resistivity of Cu (μΩ-cm)	4.83* 3.52	6.01* 4.2	7.34* 4.92
Relative Permittivity of Dielectric ϵ_r		2.3	2.0	1.7

4. RESULTS AND DISCUSSIONS

In this section, Performance parameters like Power Dissipation, Delay and PDP of MWCNT and SWCNT bundle interconnects at the 32-, 22- and 16-nm technology nodes are studied for applications in the intermediate and global levels, in comparison with their copper counterparts.

Geometrical parameters are listed in Table 1. The outermost diameter of MWCNT is equal to the wire width, and the innermost diameter and the outermost diameter ratio is assumed to be 0.5[14]. Modelling of resistances and electrostatic capacitances of MWCNT interconnect is done using (3)–(11). The equivalent resistance and capacitance of SWCNT bundle interconnect is extracted using equations (12)-(19), with interconnect geometry parameters as listed in Table-II. The space between wires is assumed to be equal to the wire width, i.e., s=w. Interconnects parameters of Cu are extracted from online tool available at [20].The inductances of all three types of interconnects are assumed negligible in sub threshold region of operation. The contact resistance between electrode and tube for each shell is assumed to be 2 kΩ. Drivers are assumed to be inverters with a n-MOSFET size of W/L = 5. The p-MOSFET size is assumed to be 2.5 of the n-MOSFET size throughout the analysis. Simulation is done using the SPICE tool. The source voltage is assumed to be a step signal with switching voltage less than threshold voltage of corresponding technology.

Fig. 5 and 6 depicts the delay time and power dissipation respectively of the MWCNT, SWCNT bundle interconnects to their Cu counterparts at the intermediate level for 400µm length at different technologies considered.

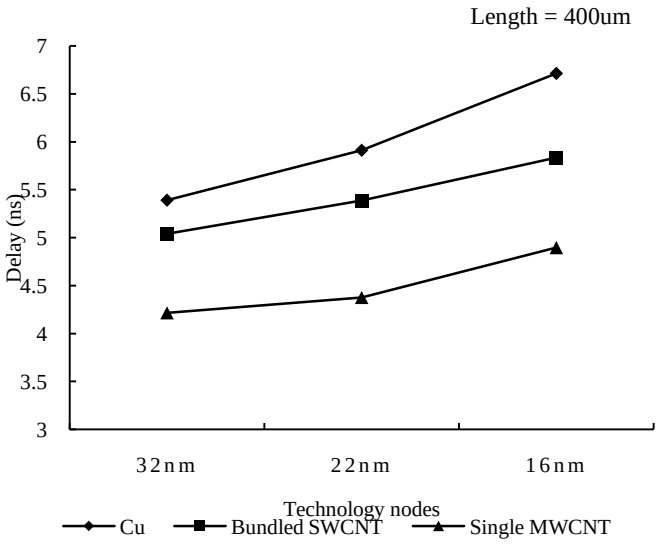

Fig 5 Delay of Cu, SWCNT Bundle, and single MWCNT in intermediate interconnect at different technology nodes.

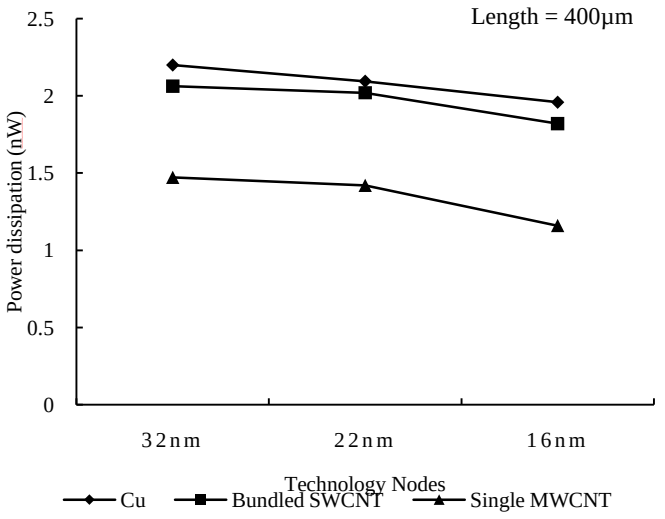

Fig 6 Power Dissipation of Cu, SWCNT Bundles, and single MWCNT in intermediate interconnect at different technology nodes.

Fig. 7 and 8 shows delays time and power dissipation variation respectively of the single MWCNT and bundle SWCNT interconnects at the global level at technology node considered. Fig. 9 and 10 depicts delay variation with length for the intermediate and global-level interconnects respectively at 16nm technology nodes for all three types of interconnect considered configurations.

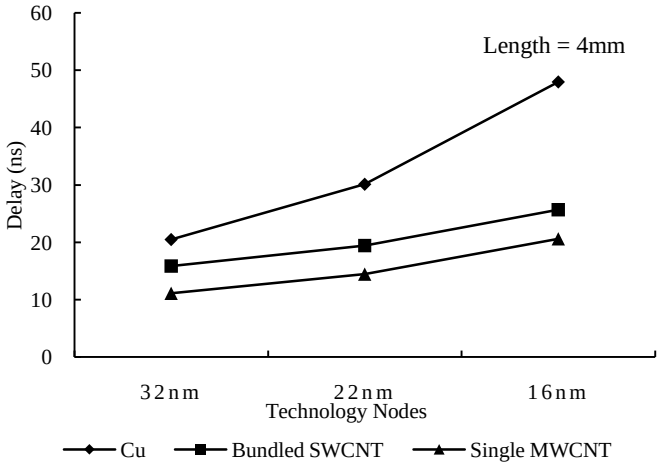

Fig 7 Delay variation of Cu, SWCNT bundle and single MWCNT in global interconnect at different technology node.

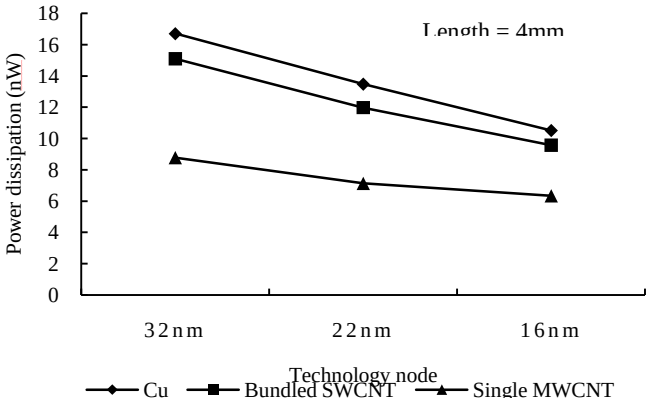

Fig 8 Power Dissipation of Cu, SWCNT Bundle and single MWCNT in global interconnect at different technology nodes.

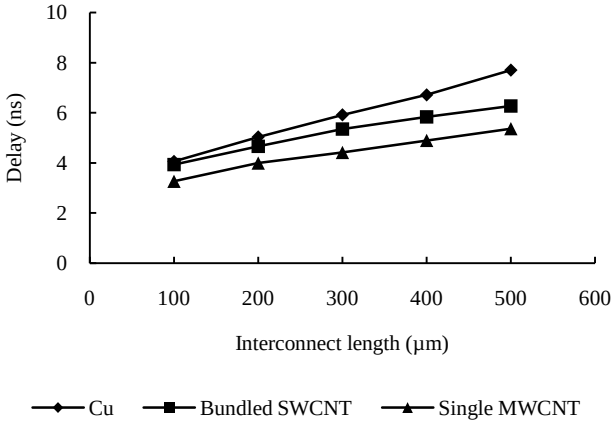

Fig 9 Delay of Cu, SWCNT bundle and single MWCNT in intermediate interconnects at 16nm technology.

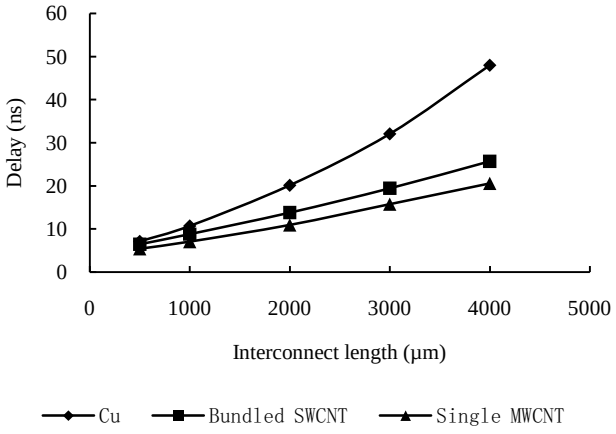

Fig 10 Delay of Cu, SWCNT bundle and single MWCNT in global interconnect at 16nm technology.

Fig. 11 and 12 shows PDP variation with length for the intermediate and global-level interconnects respectively at 16nm technology nodes for all three types of interconnect considered configurations.

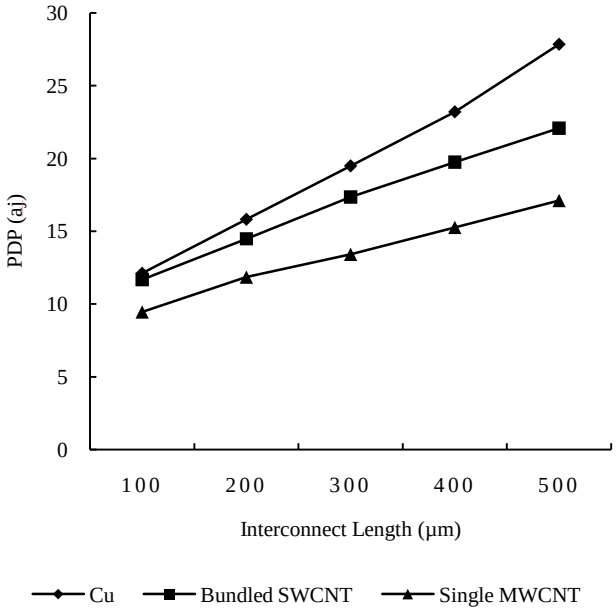

Fig 11 PDP of Cu, SWCNT bundle and single MWCNT in intermediate interconnects at 16nm technology.

The overall analysis for delay and power dissipation for intermediate and global interconnect, represented above in graphs is summarised through Table III and Table IV. The two tables concludes that MWCNT interconnects gives many folds better performance in delay and overall PDP as compare to Cu counterpart and also better than bundle SWCNT interconnects in subthreshold regime also.

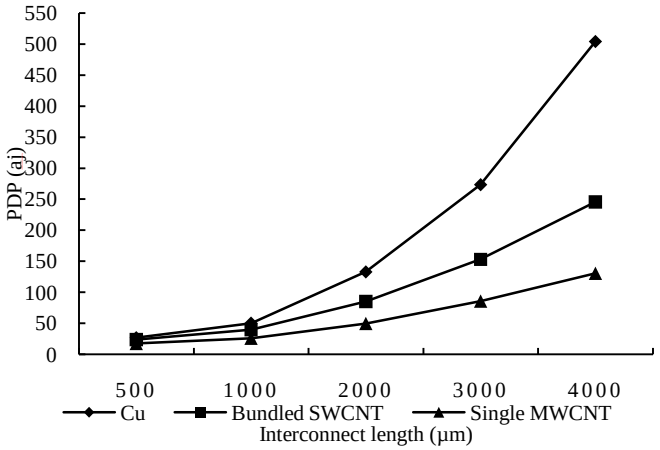

Fig 12 PDP of Cu, SWCNT bundle and single MWCNT in global interconnects at 16nm technology.

Table 3: comparative analysis of pdp at different technology nodes for 400µm interconnect length

Technology	Interconnect PDP(aj) for 400µm			Reduction in MWCNT PDP than cu/SWCNT bundle (no. of folds)	
	Cu	Bundled SWCNT	Single MWCNT	Cu	Bundled SWCNT
32nm	11.863	10.404	6.210	**1.91**	**1.675**
22nm	15.914	12.128	7.804	**2.03**	**1.554**
16nm	27.200	19.742	13.257	**2.05**	**1.489**

Table 4: comparative analysis of pdp at different technology nodes for 4mm interconnect length

Technology	Interconnect PDP for 4mm (aj)			Reduction in MWCNT PDP than cu/SWCNT bundle (no. of folds)	
	Cu	Bundled SWCNT	Single MWCNT	Cu	Bundled SWCNT
32nm	342.116	219.553	96.657	**3.539**	**2.271**
22nm	406.001	235.128	106.152	**3.824**	**2.215**
16nm	504.290	245.949	130.575	**3.862**	**1.88**

5. CONCLUSIONS

This work analyzed the delay and power dissipation for Cu, bundled SWCNT and single MWCNT interconnects for the 32-, 22- and 16nm technologies nodes using SPICE simulation. The MWCNT, SWCNT bundle and Cu interconnects have been represented as an equivalent circuit model and the CMOS driver is used to drive the interconnect lines It has been observed that MWCNT exhibits 2 to 4 folds PDP reduction as compared to bundled SWCNT/Cu and provide better result for submicron technologies. This reduction in PDP is more significant for longer interconnect length. Therefore, MWCNTs can be predicted as one of the most promising materials for the future global VLSI interconnects in subthreshold region also.

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