LOW COMPLEXITY DIGIT SERIAL FIR FILTER BY MULTIPLE CONSTANT MULTIPLICATION ALGORITHMS

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Abstract

Serial input data is multiplied with constant pair to produce constant multiplication called Multiple Constant Multiplications (MCM). In order to reduce number of shifting, an addition/subtraction operation, Graph Based (GB) algorithm is taken as a proposed algorithm to construct multiplier for transposed form of digit serial FIR (Finite Impulse Response) filter design 4-tap digit serial FIR filter with digit size d=2,4,8. To analyze low complexity Digit based recoding algorithm and CSE (Common Subexpression Elimination) algorithm simulation compared with GB algorithm based on the performance of area utilization and delay report in Xilinx ise design suite12.1software. Finally this FIR filter is implemented in FPGA spartan3 hardware for real time implementation.

Keywords: *Multiple Constant Multiplication, Digit size, Low complexity, GB algorithm*

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1. INTRODUCTION

MCM is involved to produce constant multiplication in Digital Signal Processing (DSP) systems, MIMO (Multiple Input Multiple Output) systems, Error correcting codes, Frequency multiplication, Graphics and Control applications.

In such applications full fledge of multipliers are not needed. Since coefficients are constant to produce constant multiplication. Once the MCM architecture is constructed, it can be called as many times it required.

Constant multiplication either can be done by digit parallel design or digit serial design. Digit parallel design of constant multiplier needs external wire for shifting. It requires more area while implementation takes place in FPGA or any other ASIC. Hence digit serial design overcomes area constrain with acceptable delay timing.

Multiplication with constant is called constant multiplication. This process is used in filter operation. There are two types of constant multiplication.

One is Single Constant Multiplication (SCM) and other is Multiple Constant Multiplication. Input is multiplied with single specific coefficient to produce output is called SCM. Canonical Signed Digit (CSD) number representation is used to implement SCM multipliers.

Input is multiplied with multiple numbers of specific coefficients to produce multiple outputs is called MCM. Multiplication is a process of shifting and addition operation. Constant multiplier consists of number of adder, subtractor and shifter according to the coefficient pair.

FIR filter output can be obtained by multiplication of input and impulse response. Direct and transposed form implementations are two forms of FIR filter implementations. Rather than direct form, transposed form is most effective and realizable structure. Multiplication operation takes place in multiplier block. These transposed form multiplier blocks in FIR filter will replace by MCM architecture also known as shift and add architecture.

FIR filter gives guaranteed feed forward, stable and linear phase response. For FIR filter impulse response is equal to the number of coefficients. But it is not the case in Infinite Impulse Response (IIR) filters. Hence this FIR filter implementation is sometimes called as multiplierless digit based recoding method.

1.1 Objective

Main objective is to eliminate multiplier block and introducing MCM architecture in digit serial FIR filter for the reduction of multiplication in the form of shift and add operations.

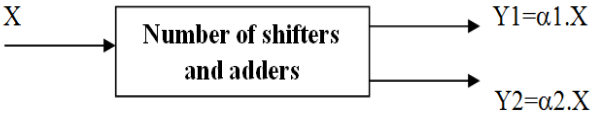

Fig 1 MCM operation

In Fig.1 X denotes input, α1 and α2 are filter coefficients, Y1 and Y2 are the outputs.

An operation with the same input is to be multiplied by a set of coefficients is said to be MCM. Serial input data is multiplied with two pair of coefficients and produces Y1, Y2 outputs.

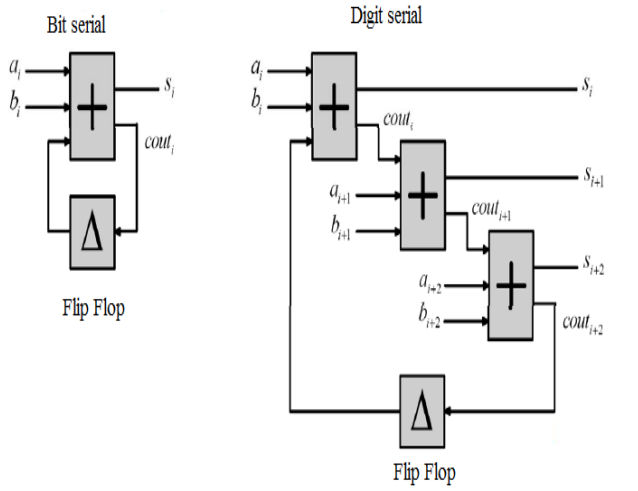

Fig 2 Digit Serial operation

Bit serial and Digit serial are the two cases for serial addition. Compared to bit serial operation, Fig.2 explains that Digit Serial operation needs less number of delay elements such as flip flop for addition or subtraction.

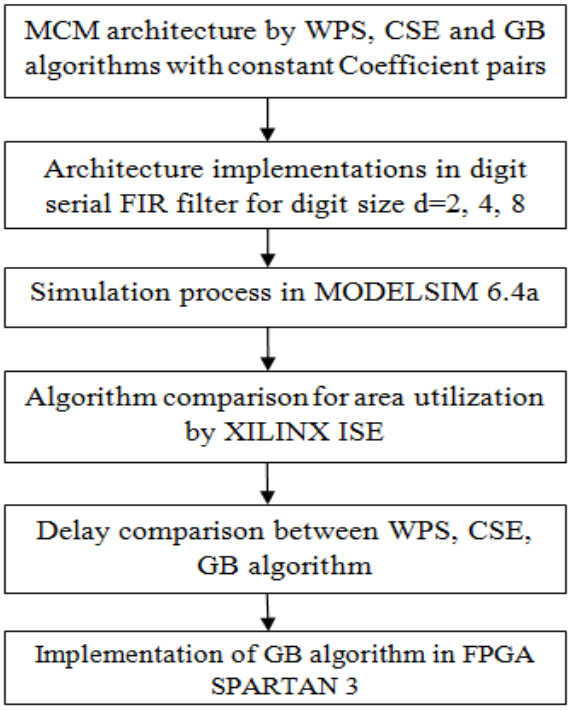

Fig 3 flow map for proposed system design

Fig.3 gives the flow map for proposed system design.

2. PROPOSED WORK

To design MCM architecture without partial product sharing algorithm (Digit based recoding), Common Sub-expression Elimination (CSE) algorithm [5]-[6] is used in existing methods. In proposed method, Graph Based (GB) [10]-[11] algorithm is used for this purpose.

Four constants are taken as taken as coefficient pair. According to MCM principle constant multiplication is performed by number of shifting and addition operation. For this purpose compare with other algorithms, GB algorithm is used to find number of shifting and addition operation.

Consider the first coefficient pair as 29x and 43x.For this pair, without partial product sharing algorithm requires six addition and six shifting operations and CSE algorithm requires four additions and four shifting operations. But GB algorithm requires only one subtractor, two adders and three shifting operation.

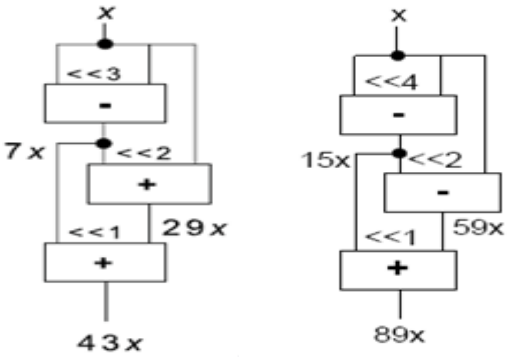

Fig 4 GB algorithm for 29,43,59,89 coefficients

Consider the second coefficient pair as59x and 89x.For this pair, without partial product sharing algorithm requires four addition, one subtraction and five shifting operations and CSE algorithm requires four subtractions and four shifting operations. But GB algorithm requires only two subtraction, one addition and three shifting operation.

2.1 FIR Filter [4 TAP] with MCM

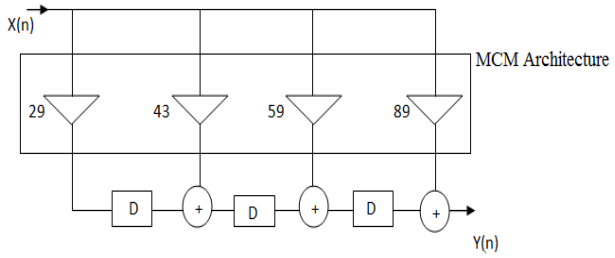

Fig 5 Four tap FIR filter with MCM architecture

Steps of GB algorithm can be applied for any coefficient pair combinations. Hence GB algorithm is used and number of operation is reduced drastically than other algorithms.

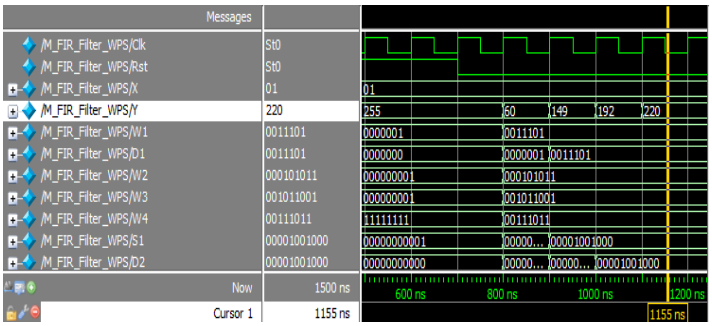

Fig 6 Output for FIR filter with digit based recoding algorithm

Four filter coefficient 29,43,59,89 values are taken for digit serial FIR filter design. X(n) is taken as a input sequence and Y(n) is taken as output sequence.

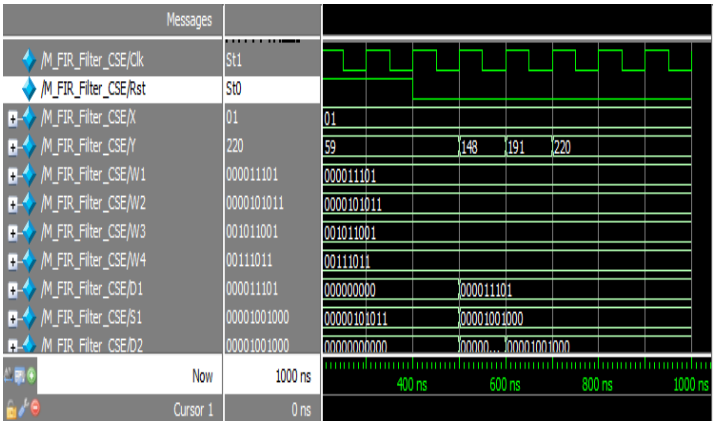

Fig 7 Output for FIR filter with CSE algorithm

Fig.6 shows 4 tap FIR filter with without partial product sharing (Digit based recoding) algorithm and Fig.7 displays 4 tap filter with CSE algorithm.

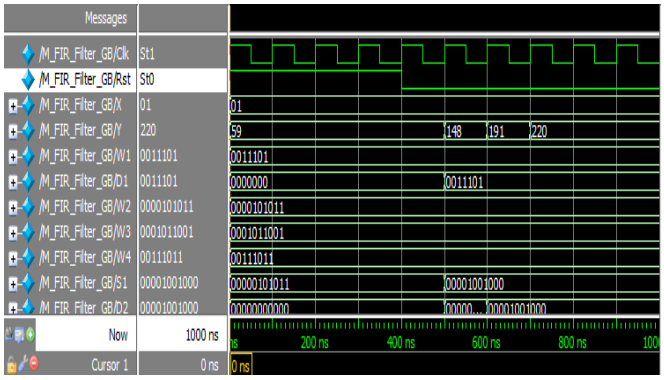

Fig 8 Output for FIR filter with GB algorithm

Fig.8 displays 4 tap filter with GB algorithm. This simulation result was displayed by modelsim software. These are the simulation results displayed by modelsim software.

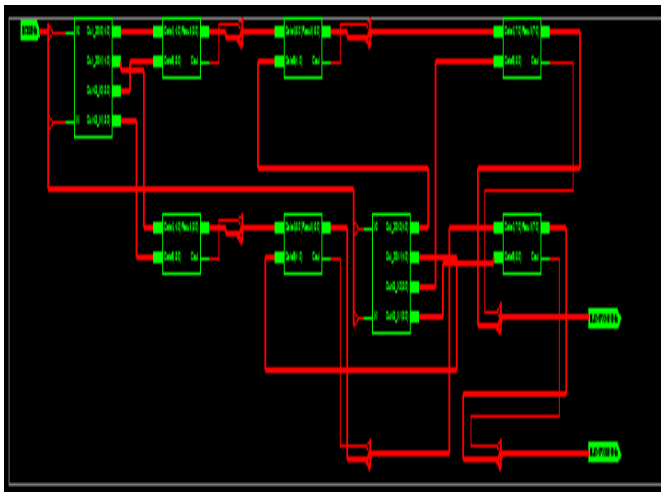

Fig 9 RTL schematic view of FIR filter

After completion of simulation process in Modelsim tool, synthesis process is takes place to calculate gate count and delay report. Fig.9 shows the RTL schematic view of FIR filter with MCM architecture.

3. FIR FILTER DEVICE UTILIZATION REPORT

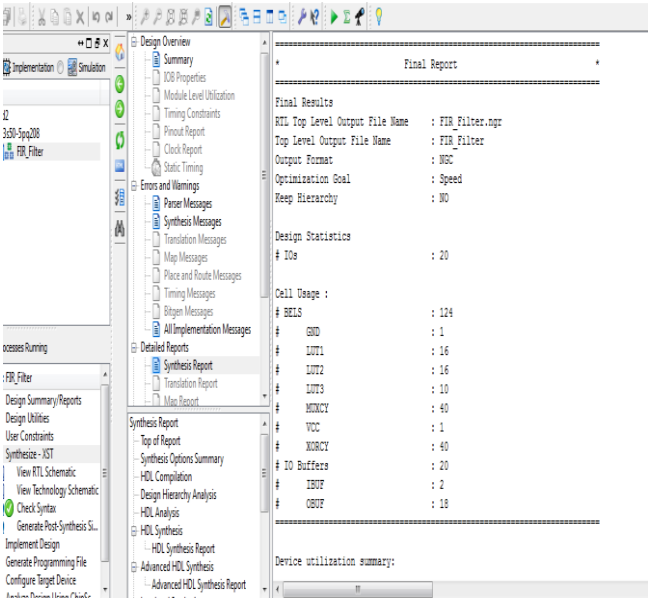

Fig 10 Device utilization report

FIR filter with digit size d=2, 4, 8 was synthesized separately for device utilization in terms of gate count with each different algorithms. Fig 10 shows the device utilization report of FIR filter with GB algorithm. Table-1 explains that the FIR filter

with GB algorithm utilized less number of gate count than other two algorithms.

Table -1: Gate Count Comparison

FIR filter digit size	WPS	CSE	GB
d=2	790	635	578
d=4	1157	1132	707
d=8	2048	1994	1902

4. FIR FILTER DELAY SYNTHESIS REPORT

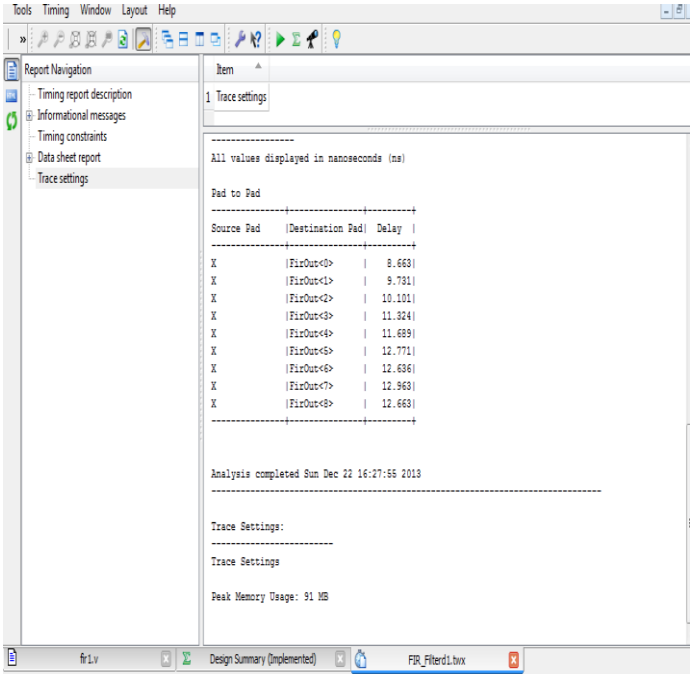

Fig 11 Delay synthesis report

FIR filter with digit size d=2, 4, 8 was synthesized separately for delay comparison. Fig.9 shows the delay synthesis report of FIR filter with GB algorithm. Table-2 explains that the FIR filter with GB algorithm has less delay time than other two algorithms.

Table-2: Delay comparison

FIR filter digit size	WPS	CSE	GB
d=2	18.884ns	11.91ns	11.885ns
d=4	16.078ns	15.384ns	17.165ns
d=8	28.759ns	19.988ns	19.476ns

5. CONCLUSIONS

Thus the implementation of digit serial FIR filter was implemented with low complexity MCM architectures for digit sizes d=2, 4, 8. Device utilization and delay values are compared for hardware implementation. Hence this MCM approach drastically reduces the system complexity, area and delay and FPGA hardware real time implementation has performed with spartan3 version. Future enhancement of this paper is to design MCM architecture with more coefficient pairs for FIR filter implementation.

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BIOGRAPHIES

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