

DESIGN OF SUBTHRESHOLD DML LOGIC GATES WITH POWER GATING TECHNIQUES

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Abstract

Sub-threshold circuit design is one of the promising methods for low power to ultra-low power applications. Circuits which operate in the sub-threshold region use a supply voltage that is close to or less than the threshold voltages of the transistors, so that there is a significant reduction in both dynamic and static power consumption. The low-power dual mode logic (DML) family is a logic family designed to operate in the sub-threshold region. The proposed logic family can be switched between static and dynamic modes of operation according to system requirements. The ability of DML circuits to operate in both the static and dynamic modes gives the opportunity to create efficient logic circuits which balance power consumption and operating frequency (speed of the circuit) requirements. In the static mode of operation, the dual mode logic gates has very low-power dissipation with moderate performance, and in the dynamic mode of operation they have higher performance, at the price of increased power dissipation

Keywords: Dual mode logic (DML), Subthreshold

1. INTRODUCTION

With technological advancements and the mobile applications expansion, power consumption has become a primary focus of attention in VLSI digital design. Hence Digital sub-threshold circuit design is one of the main focus areas for low power to ultra-low power applications. The supply voltage that is applied to the circuits operating in the sub-threshold region is very close to or less than the threshold voltages of the transistors, so it allows a significant reduction of both dynamic and static power.

One of the most common logic family used for sub-threshold operation currently is the Complementary Metal Oxide Semiconductor (CMOS) logic family. Ultra low Voltage (ULV) operation originally introduced in 1972 was originally used for low throughput applications like wrist watches, sensors and biomedical devices. It gives low to moderate performance and maintains low- power dissipation.

The dual mode logic NAND, NOR and INVERTER is designed to operate in the sub threshold region. The proposed logic gates can be operated in two modes: static CMOS-like mode and dynamic CMOS-like mode as shown in Fig. 1. In the static mode of operation, the DML gates have very low power dissipation with moderate performance. When the DML gate is in the dynamic functional mode, they have much higher performance, at the cost of increased power dissipation. This particular feature of the Dual Mode Logic provides the option to control system performance on-the-fly and hence support applications in which a flexible workload is required.

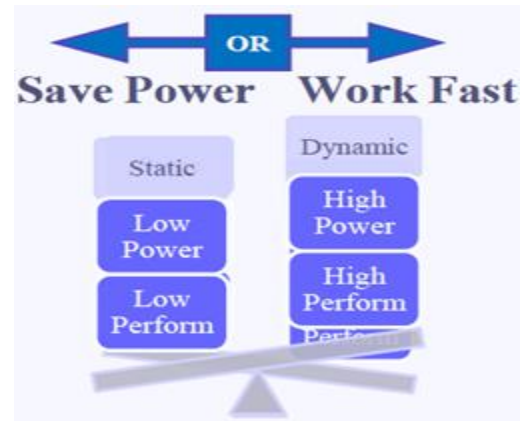


Fig-1: Static and Dynamic Modes of Operation

The rest of this paper is constructed as follows. Section II provides an overview of the basic DML logic gate architecture and its method of operation. Section III describes the designing of the Nand, Nor, Not DML gates. Section IV describes the Dual Mode Logic with Power Gating techniques. Section V concludes this paper.

2. BASIC DUAL MODE LOGIC ARCHITECTURE

The basic DML logic gate designed to operate in either static mode of operation or dynamic mode of operation consists:

A static gate having one or more logic inputs, a single logic output and a switching element that is associated with the static gate as shown in Fig. 2. The switching element comprises of an

input that is connected to a constant voltage, and another input for providing a signal used for mode selection, an output that is connected to a logic output of the static gate. The switching element can be configured to operate in either of the two modes by:

- i) disconnecting the static gate output from both the input that is connected to a constant voltage, and the other input for providing a signal used for mode selection, when the mode selection signal applies a constant voltage to the input used for providing mode selection signal, thereby selecting static mode of operation
- ii) Connecting the static gate output to both the input that is connected to a constant voltage, and the other input for providing a signal used for mode selection, when the mode selection signal applies a dynamic clock signal to the input used for providing mode selection signal, thereby to select dynamic mode operation.

Switching the Dual mode logic gates between the two functional modes, static and dynamic, is performed by applying either a constant voltage or a dynamic clock signal at the mode selection input of the switching element.

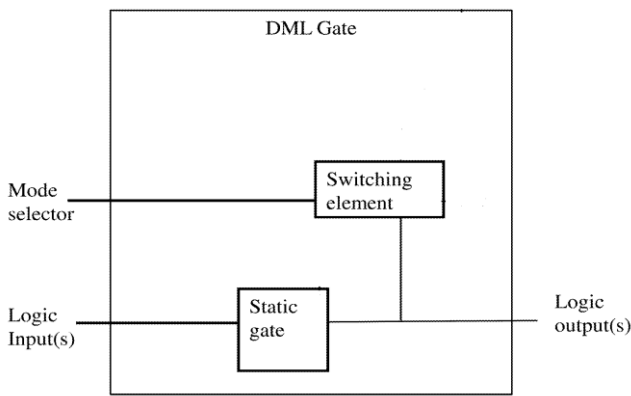


Fig-2: Basic DML Logic

When static functional mode is selected an appropriate constant voltage (high or low as required by static gate topology) is applied to the mode selection input of the switching element. The applied constant voltage causes the switching element to disconnect the static gate output from the constant voltage applied, thus enabling static mode of operation. During dynamic mode of operation, the switching element input a dynamic clock signal which has pre-charge and evaluate phases, which will periodically connect the static gate output to the constant voltage level, thus enabling dynamic mode of operation.

In the DML circuit designed, the static gate is a CMOS gate and switching element is implemented by either a PMOS or an NMOS transistor. In order to operate the Dual mode logic gate in the dynamic functional mode, the clock (Clk) signal applied

to the switching element has two distinct phases: the precharge and evaluation phases. During the precharge phase, the output of the DML gate is charged to high/low, based on the topology of the DML gate. During the following evaluation phase, the DML gate's output is evaluated according to the values at the DML gate inputs. The DML topologies, marked Type A and Type B, are illustrated in Fig. 3. Type A topology has an added p-MOS transistor that precharges the output to a logical "1" during the precharge phase. Type B DML topology has an added n-MOS that precharges the gate output to a logical "0" during the precharge phase.

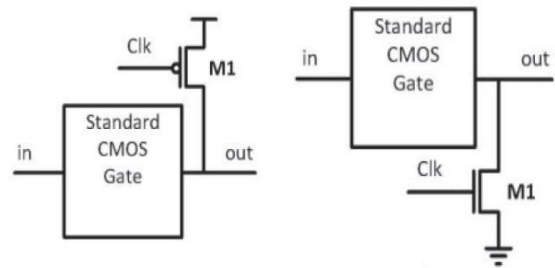


Fig-3: Basic DML Type A topology and Type B topology.

Switching the DML gates to operate in CMOS-like static mode of operation is done by either by fixing the global Clock (Clk) signal to logic high for Type A topology or by fixing the global Clk signal to logic low for Type B topology.

3. DML NAND, NOR, INVERTER GATES DESIGN

Conventional Nand logic gate design is done using Tanner S-Edit EDA tool and its power and performance are found. Also Dual Mode Logic Nand gate Type A and Type B topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations. The truth table of the 2-input NAND gate is given in Table 1.

Table-1: Truth Table of 2-input NAND

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

To design a DML gate, the methodology that is to be followed is to place the precharge transistor in parallel to the stacked transistors of the basic CMOS gate. Then, the evaluation of the logic will be performed with the parallel transistors which will make the evaluation process faster.

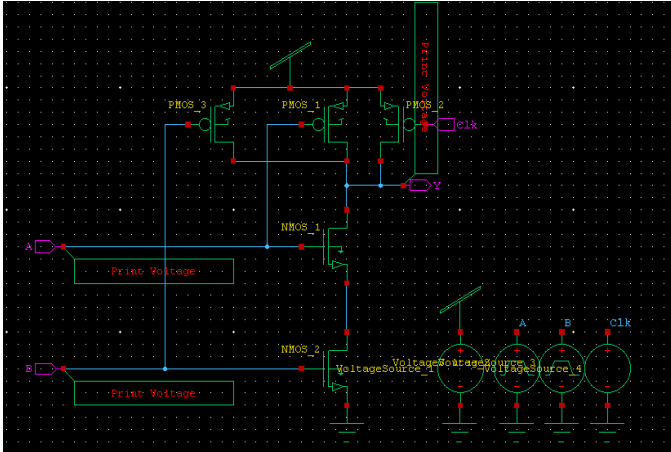


Fig-4: Schematic of type A Static nand

In the DML Type-A Static NAND topology, the switching element is a pMOS transistor connected parallel to the Pull-up network as shown in Fig. 4. The input to the switching element is a constant high voltage to make it OFF. The only difference when designing DML Type-A Dynamic NAND topology, is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation.

In the DML Type-B Static NAND topology, the switching element is an NMOS transistor connected parallel to the Pull-down network. The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NAND topology shown in Fig. 5 is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation.

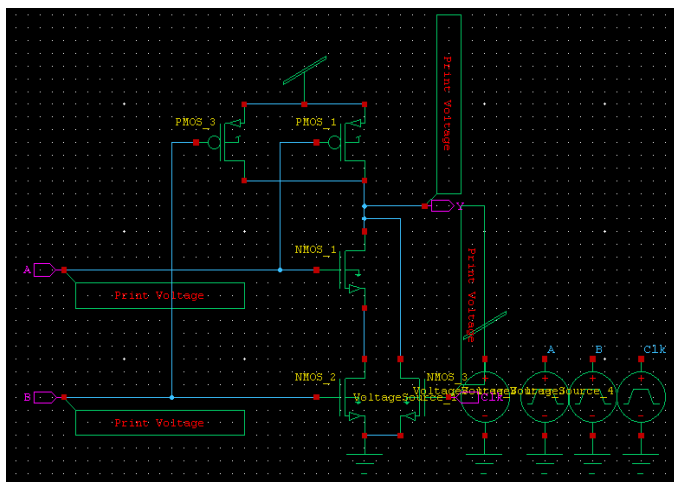


Fig-5: Schematic of type B Dynamic nand

Conventional NOR logic gate design is done using Tanner S-Edit EDA tool and its power and performance are found. Also Dual Mode Logic Nand gate Type A and Type B topologies

designed and their power consumption and performance were analyzed for static and dynamic mode of operations. The truth table of the 2-input NOR gate is given in Table 2.

Table-2: Truth Table of 2-input NOR

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

In the DML Type-A Static NOR topology, the switching element is a PMOS transistor connected parallel to the Pull-up network which is a series connection of 2 PMOS transistors as shown in Fig. 6. The input to the switching element is a constant high voltage to make it OFF. The only difference when designing DML Type-A Dynamic NOR topology, is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation.

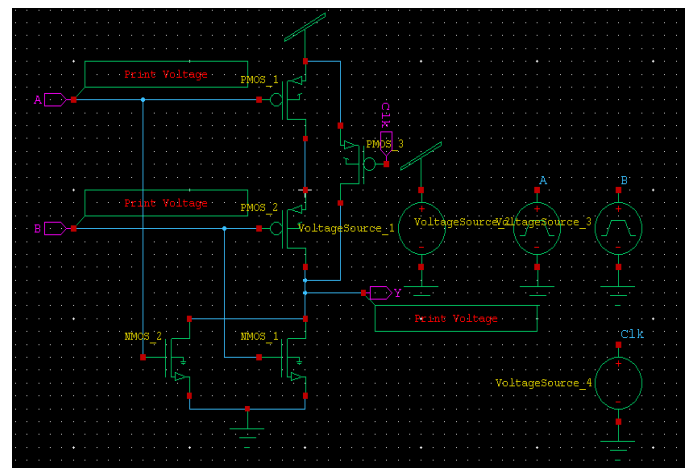


Fig-6: Schematic of type A Static nor

In the DML Type-B Static NOR topology, the switching element is an NMOS transistor connected parallel to the Pull-down network which is a parallel connection of 2 NMOS transistors. The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NOR topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation as shown in Fig. 7.

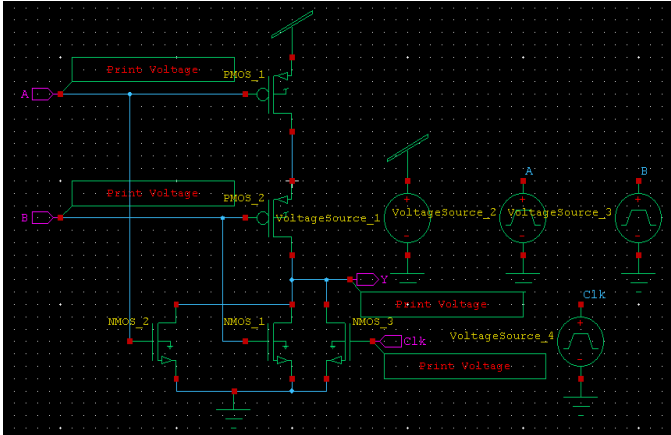


Fig-7: Schematic of type B Dynamic nor

Conventional inverter gate design is done using Tanner S-Edit EDA tool and its power and performance are found. Also Dual Mode Logic Nand gate Type A and Type B topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations. The truth table of the NOT gate is given in Table 3.

Table-3: Truth Table of NOT

A	Q
0	1
1	0

In the DML Type-A Static NOT topology, the switching element is a PMOS transistor connected parallel to the Pull-up network as shown in Fig. 8. The input to the switching element is a constant high voltage to make it OFF. The only difference when designing DML Type-A Dynamic NOT topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation.

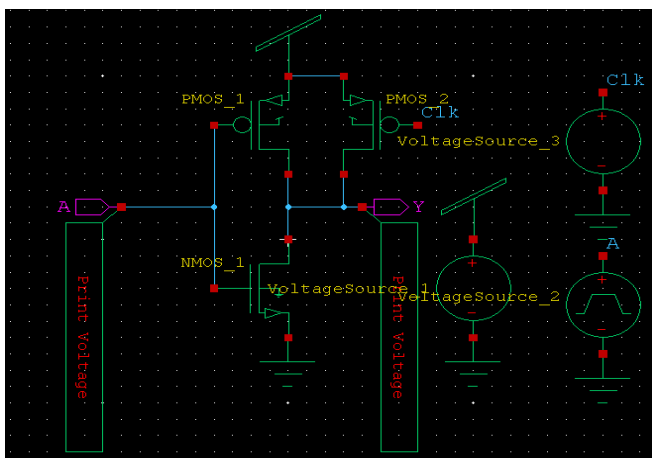


Fig-8: Schematic of type A Static not

In the DML Type-B Static NOT topology, the switching element is an NMOS transistor connected parallel to the Pull-down network. The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NOT topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation as shown in Fig. 9.

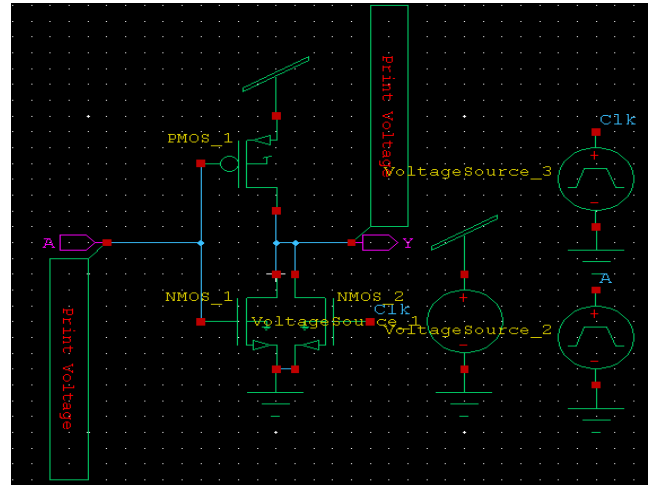


Fig-9: Schematic of type B Dynamic not

4. DML WITH POWER GATING TECHNIQUES

Power Gating is an effective implementation that is used in Low Power Designs. While Clock Gating saves the dynamic power of a circuit, Power Gating saves the leakage power. As the technology moves from micron technology to sub-micron technology, the leakage power dissipation dominates the dynamic power dissipation.

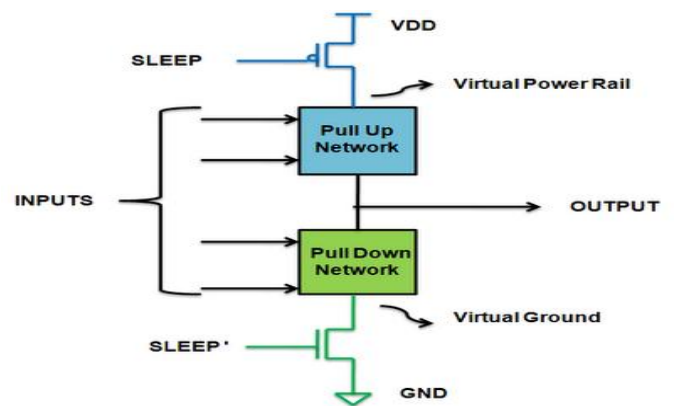


Fig-10: Power Gating structure

The power gated sleep circuit has two modes of operations:

1. Active mode
2. Sleep mode

In active mode, the sleep Signal SLEEP of the transistor is held at logic '0' and SLEEP at logic '1' hence both the sleep transistors remain ON. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage.

In sleep mode, the sleep Signal SLEEP of the transistor is held at logic '1' and SLEEP at logic '0' hence both the sleep transistors are turned OFF and the logic part is dis-connected from the supply and ground leading to very less power consumption during sleep mode. Power gating is incorporated in to the DML architecture as shown in Fig. 11.

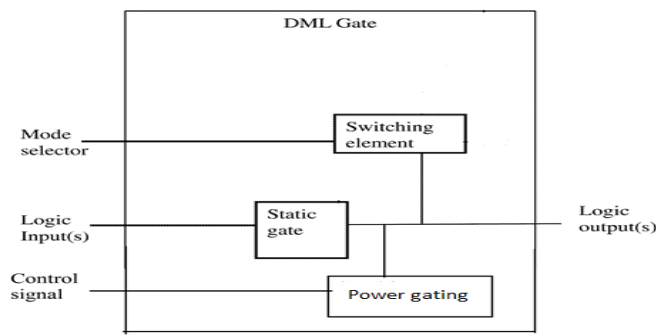


Fig-11: DML gate with Power Gating

Different methods of power gating like the sleep method, sleepy stack and dual sleep approaches added to the existing Dual mode logic NAND, NOR, NOT gates.

The Sleep method is the basic power gating method. The sleep transistors isolate the logic networks and the sleep transistor technique or the sleep method dramatically reduces leakage power during sleep mode. Fig.12 shows Type A Dynamic Dual Mode Logic Nand with sleep power gating technique.

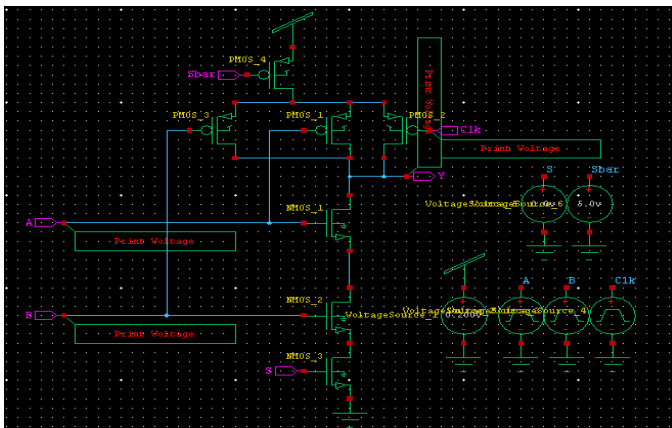


Fig-12: Type A dynamic NAND with Sleep Power Gating Technique

The sleepy stack approach merges the sleep and stack approaches. The sleepy stack technique splits the existing transistors into two half Size transistors like the stack approach. The activity of the sleep transistors in the sleepy stack method is same as the activity of the sleep transistors in the sleep method. The sleep transistors are turned on during the active mode and they are turned off during the sleep mode. Fig. 13 shows Conventional NOT gate with Sleepy Stack Power Gating Technique.

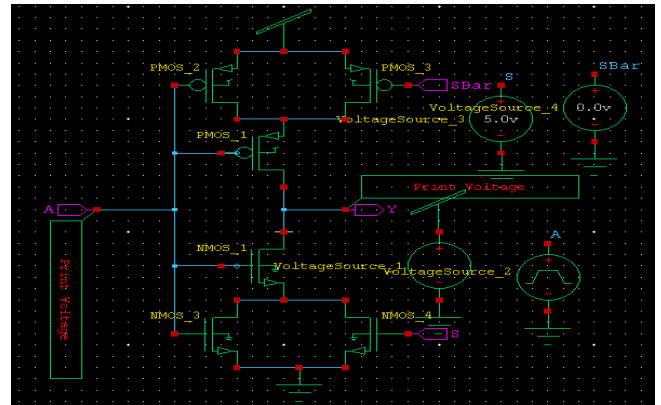


Fig-13: Conventional NOT gate with Sleepy Stack Power Gating Technique

The Dual sleep approach has the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. In normal mode when S=1 the pull down NMOS transistor is in ON state and in the pull-up network the PMOS sleep transistor is in ON state since S'=0. During sleep mode state S is forced to 0 and hence the pull-down NMOS transistor is in OFF state and PMOS transistor is in ON state and in the pull-up network, PMOS sleep transistor is OFF while NMOS sleep transistor is ON. So in sleep mode state a PMOS is in series with an NMOS both in pull-up network and pull-down network which reduces the power dissipation. Fig.14 shows Type B Static NOR with Dual Sleep Power Gating Technique

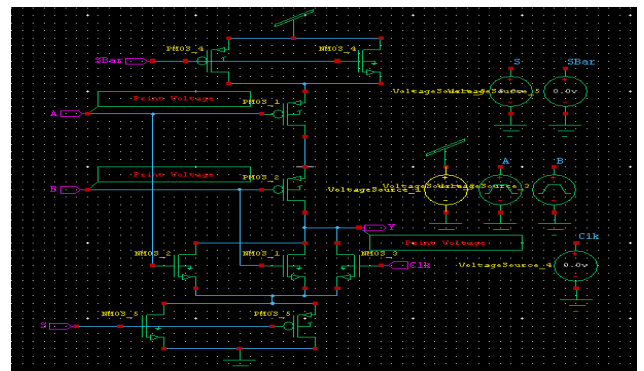


Fig-14: Type B Static NOR with Dual Sleep Power Gating Technique

The comparison of the NAND, NOR, NOT Dual mode logic gates in terms of power consumption is shown in Table 4.

Table- 4: Comparison between NAND, NOR, NOT DML gates

	NAND	NOR	NOT
CONVENTIONAL	6.24E-09W	5.11E-09W	3.35E-09W
TYPE A STATIC	5.32E-09W	4.91E-09W	2.37E-09W
TYPE A DYNAMIC	9.44E-09W	5.54E-09W	1.15E-08W
TYPE B STATIC	6.07E-09W	5.08E-09W	3.27E-09W
TYPE B DYNAMIC	7.02E-09W	5.15E-09W	3.26E-09W

The NAND Dual mode logic gate is compared in terms of power consumption for different power gating techniques like sleep method, sleepy stack method and dual sleep method in Table 5.

Table-5: Comparison between NAND DML gates with different power gating techniques

	NAND SLEEP POWER GATING	NAND SLEEPY STACK POWER GATING	NAND DUAL SLEEP POWER GATING
CONVENTIONAL	1.71E-09W	2.06E-09W	1.01E-08W
TYPE A STATIC	1.36E-09W	7.42E-10W	7.39E-09W
TYPE A DYNAMIC	2.73E-09W	3.29E-09W	1.34E-08W
TYPE B STATIC	1.55E-09W	8.32E-10W	9.87E-09W
TYPE B DYNAMIC	2.13E-09W	8.09E-09W	1.14E-08W

The NOR Dual mode logic gate is compared in terms of power consumption for different power gating techniques in Table 6. Also The NOT Dual mode logic gate is compared in terms of power consumption for different power gating techniques in Table 7.

Table-6: Comparison between NOR DML gates with different power gating techniques

	NOR SLEEP POWER GATING	NOR SLEEPY STACK POWER GATING	NOR DUAL SLEEP POWER GATING
CONVENTIONAL	2.98E-09W	2.24E-09W	2.82E-09W
TYPE A STATIC	2.27E-09W	2.18E-09W	1.81E-09W

TYPE A DYNAMIC	7.72E-09W	2.45E-08W	5.47E-09W
TYPE B STATIC	2.95E-09W	1.78E-09W	1.73E-09W
TYPE B DYNAMIC	3.04E-09W	3.17E-09W	2.91E-09W

Table- 7: Comparison between NOT DML gates with different power gating techniques

	NOT SLEEP POWER GATING	NOT SLEEPY STACK POWER GATING	NOT DUAL SLEEP POWER GATING
CONVENTIONAL	1.58E-09W	2.57E-10W	1.65E-09W
TYPE A STATIC	5.07E-10W	3.45E-12W	2.00E-10W
TYPE A DYNAMIC	5.57E-09W	1.93E-09W	1.75E-09W
TYPE B STATIC	1.50E-09W	2.06E-10W	1.56E-09W
TYPE B DYNAMIC	1.63E-09W	2.86E-10W	1.96E-09W

5. CONCLUSIONS

The result obtained leads to the conclusion that while operating in the dynamic mode, sub threshold DML gates achieve an improvement in speed compared to a standard CMOS, while dissipating more power and in the static mode, a reduction of power dissipation is achieved, at the expense of a decrement in performance. The different methods of power gating applied to the DML logic have reduced the power dissipation further.

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BIOGRAPHIES



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