

FPGA IMPLEMENTATION OF VARIOUS LINES CODING TECHNIQUE FOR EFFICIENT TRANSMISSION OF DIGITAL DATA IN COMMUNICATION

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Abstract

This paper describes the implementation of various line coding schemes using VHDL on Xilinx Spartans-6 XC6SLX45 FPGA platform for the purpose of security, area optimization and can support efficient digital communication in varying channel environment. The choice of line code depends upon presence or absence of DC level, power spectral density, Bandwidth requirement, Bit error rate (BER) performance, ease of clock signal recovery and presence or absence of inherent error detection property. The line encoding schemes used are Unipolar RZ and NRZ, Polar RZ and NRZ, AMI and Manchester coding and Pseudo ternary encoding, Coded Mark Inversion format. Select pin impinged on the chip enables the users to select any one of the line encoding technique according to their requirement. The modeling and simulation of various line codes are implemented on Xilinx design tools and Hardware abstraction completed on Spartan-6 FPGA.

Keywords: Line Encoding, Xilinx Spartans-6 XC6SLX45 FPGA, NRZ (Non Return to Zero), RZ (Return to Zero), AMI (Alternate Mark Inversion), Manchester format, CMI (Coded Mark Inversion), pseudo ternary encoded format.

1. INTRODUCTION

Line coding consists of representing the digital signal to be transported by an amplitude and time-discrete signal that is optimally tuned for specific properties of the physical channel and of receiving equipment. After the emergence of VLSI technology researcher are continuously trying to reduce the power requirement, area optimization and to achieve less propagation delay by using various algorithms. Line coding is a key building block for communication system in which 1's and 0's are translated into the sequence of voltage and current pulse that can be propagated through physical media like coaxial cable, optical fiber etc. Digital baseband signal often used to provide particular spectral characteristics of a pulse train. Most popular line codes are return to zero and not return to Zero. All of them are in either unipolar or polar encoded format. The choice of line codes depend upon the presence or absence of DC level, PSD (power spectral density), bandwidth requirements, bit error rate performance, ease of clock signal recovery or absence of inherent detection property.

2. METHODOLOGY

Line coding techniques can be broadly divided into following different categories:-

1. *Unipolar NRZ (Not Return To Zero)* Unipolar mean bits can be represented by either positive voltage or by negative voltage. In this encoded format binary 1 is represented by high voltage level while binary 0 is represented by zero voltage level for whole bit interval (T_b).

2. *Unipolar RZ (Return To Zero)* In this encoded format binary 1 is represented by high voltage (positive) level for first half bit interval ($0 < t < T_b/2$) and it return to zero for second half bit interval ($T_b/2 < t < T_b$). Binary 0 is represented by zero voltage level for whole bit interval (T_b).

3. *Polar NRZ (Not Return To Zero)* Polar means bits can be represented in both positive as well as negative voltage level. In this encoded format binary 1 is represented by high voltage (positive) level while bit 0 is represented by low voltage (negative) level for whole bit duration (T_b).

4. *Polar RZ (Return To Zero)* In this encoded format binary 1 is represented by high voltage (positive) level for first half bit interval ($0 < t < T_b/2$) and it return to zero for second half bit interval ($T_b/2 < t < T_b$) while bit 0 is represented by low voltage (negative) level for first half bit interval ($0 < t < T_b/2$) and it return to zero for second half bit interval ($T_b/2 < t < T_b$).

5. *Manchester Encoded Format* In this encoded format binary 1 is represented by high voltage (positive) level for first half bit interval ($0 < t < T_b/2$) and low voltage (negative) level for second half bit interval ($T_b/2 < t < T_b$) while bit 0 is represented by low voltage (negative) level for first half bit interval ($0 < t < T_b/2$) and high voltage (positive) level for second half bit interval ($T_b/2 < t < T_b$).

6. *AMI (Alternate Mark Inversion)* In this encoded format bit 0 is represented by zero voltage level for whole bit interval (T_b) while bit 1 are represented by high voltage level and low voltage level alternatively for bit duration (T_b).

7. *Pseudo ternary Encoded Format* In this encoded format binary 1 is represented by zero voltage level while binary 0 is represented by alternating high voltage level and low voltage level for whole bit duration (T_b).

8. *CMI (Coded Mark Inversion)* In this encoded format binary 0 is represented by zero voltage level for first half bit interval ($0 < t < T_b/2$) and high voltage (positive) level for second half bit interval ($T_b/2 < t < T_b$) while bit 1 is represented by high voltage (positive) level and low voltage (negative) level alternatively for bit duration (T_b).

3. ENCODING ALGORITHMS

As we know that in Xilinx ISE Project Navigator can represent only two voltage levels (either 0 or 1) in the waveforms, therefore signed binary notation used to implement the design. For that purpose high voltage (positive) level is represented by 01 and low voltage (negative) level is represented by 11 while zero voltage level represented by 00.

Hence
 $+1=01$
 $-1=11$
 $0=00$

The respective truth tables for all the encoding schemes are explained in the tables given below. The algorithms for Unipolar NRZ, Unipolar RZ, Polar NRZ, Polar RZ, Manchester encoder format are given in table 1. Algorithms for AMI, pseudo ternary and CMI are given in Table 2, Table 3 and Table 4 respectively.

Table 1

Line Coding Techniques	Input bits	Output ($0 < t < T_b/2$)	Output ($T_b/2 < t < T_b$)
Unipolar NRZ	0	00	00
	1	01	01
Unipolar RZ	0	00	00
	1	01	00
Polar NRZ	0	11	11
	1	01	01
Polar RZ	0	11	00
	1	01	00
Manchester Format	0	11	01
	1	01	11

Table 2: AMI

Present State	Input bits	Output	Next State
0	0	00	0
0	1	01	1
1	0	00	1
1	1	11	0

Table 3: Pseudoternary

Present State	Input bits	Output	Next State
0	0	01	0
0	1	00	1
1	0	11	1
1	1	00	0

Table 4: CMI

Present State	Input bits	Output ($0 < t < T_b/2$)	Output ($T_b/2 < t < T_b$)	Next State
0	0	00	01	0
0	1	01	01	1
1	0	00	01	1
1	1	11	11	0

4. SIMULATION RESULTS

Xilinx project navigator is used to design and generate the RTL schematics of different Line coding techniques according to algorithms define in different tables describe above. Xilinx ISim simulator is used to verify and implement the logic of different line coding technique using waveforms. The simulation results shown in figure1-8. These logic design are implemented on Xilinx Spartans-6 XC6SLX45 FPGA platform.

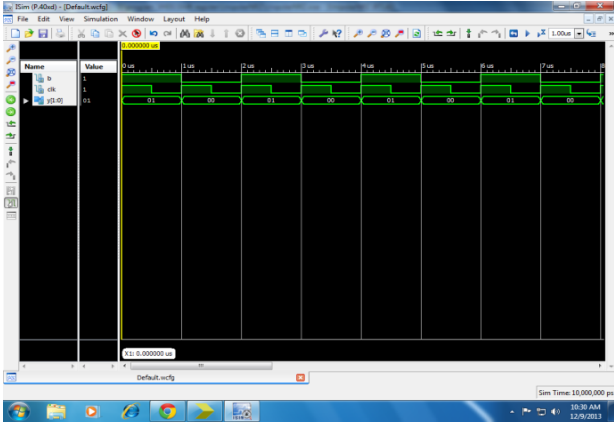


Fig.1 (Unipolar NRZ)

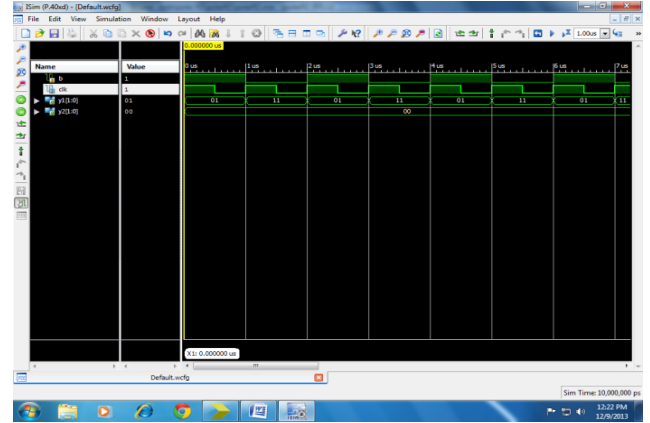


Fig. 4 (Polar RZ)

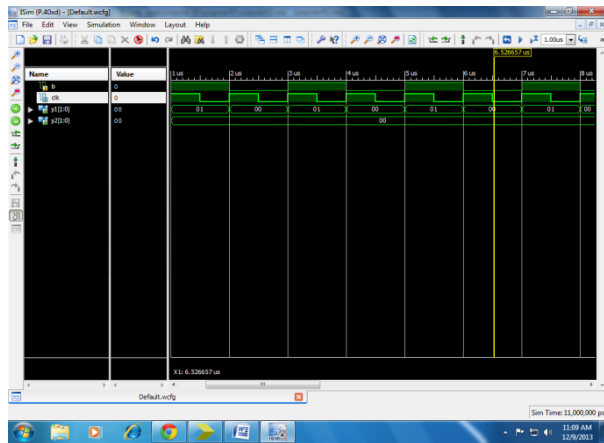


Fig. 2 (Unipolar RZ)

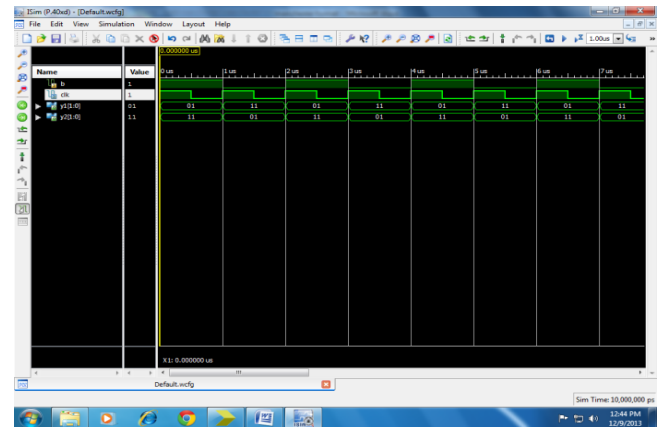


Fig. 5 (Manchester Format)

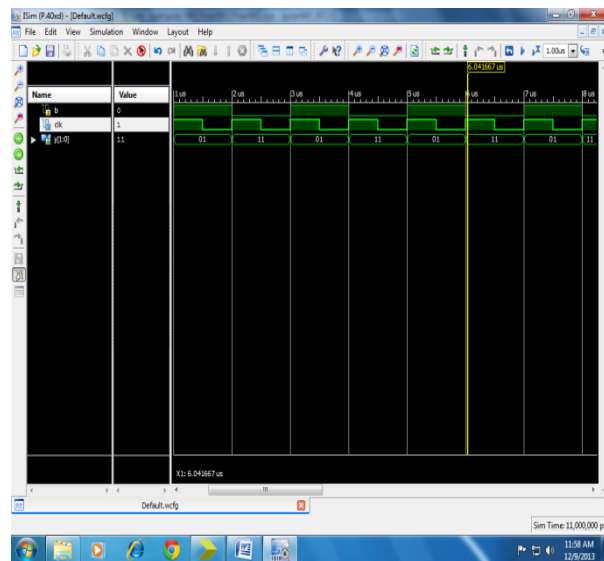


Fig. 3 (Polar NRZ)

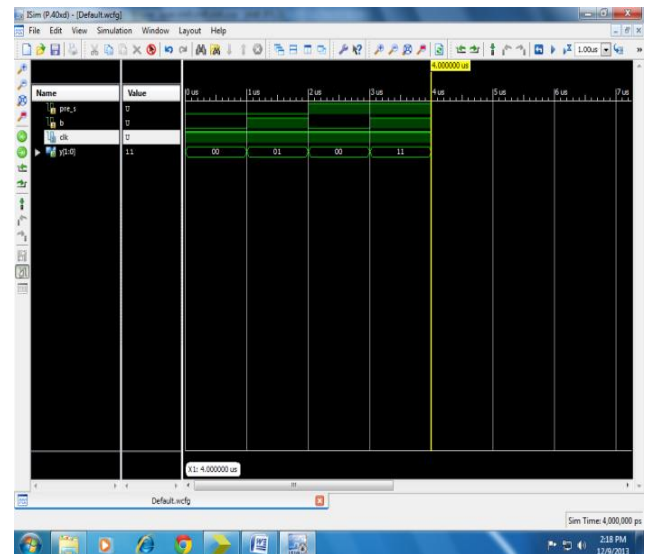


Fig. 6 (Alternate Mark Inversion)

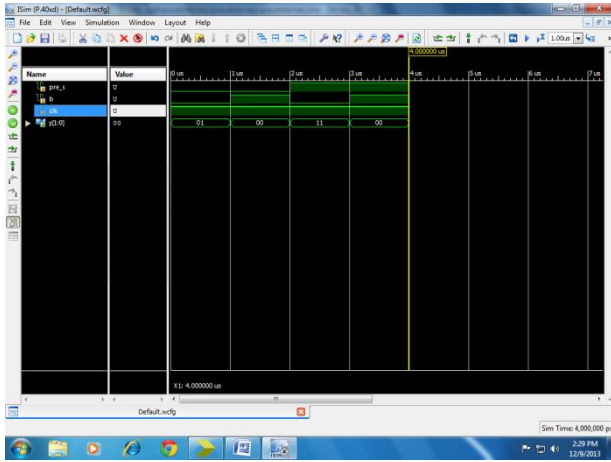


Fig. 7 (Pseudoternary Format)

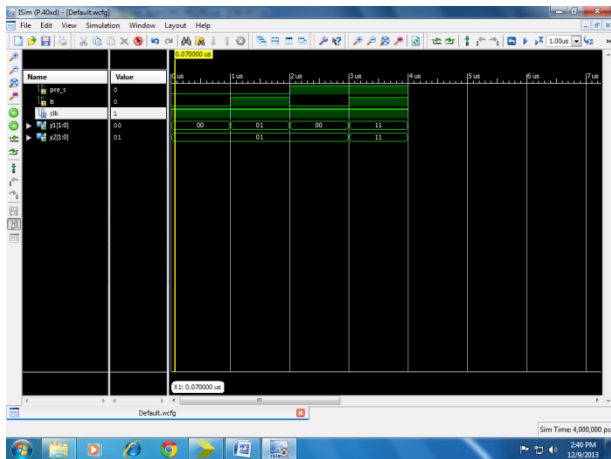


Fig. 8 (Coded Mark Inversion)

5. CONCLUSIONS

In this paper software implementation and hardware abstraction of different line coding techniques achieved using Xilinx design tools and Xilinx Spartans-6 XC6SLX45 FPGA. The architecture designed has low complexity, it is easy to implement and is efficient for all the encoding schemes for the transmission of baseband signal in digital communication.

REFERENCES

- [1]. Amrinder Kaur, Mandeep Singh, Balwinder Singh "VHDL Implementation of Universal Encoder for communication", ISP Journal of Electronics Engineering, Vol.1, Issue 2, ISSN 2250-0537(online), pp. (37-41). December 2011.
- [2]. David Alejandro Lopez-Ramirez, Mario Reyes-Ayala, Edgar Alejandro Andrade, Jose Alfredo Tirado-Mendez, "Educational prototype for line coding", proceeding of the 6th WSEAS International Conference on Engineering Education, ISSN: 1790-2769, 2009.

[3]. Chen Xinkun, Zhou, Yu Jingdong, "Design and Implementation of Manchester encoder", Journal of University of Electronics Science and Technology of China, Vol 32, pp.324-7, June 2003.

[4]. C.K. Chuang, C.G. Harrison, "Analogue Behavioral Modeling and Simulation using VHDL and Saber-mast", IEEE xplore, 1994

[5]. K W Cattermole. "Principle of digital line coding", International Journal of Electronics, vol.55, no. 1, pp. 3-33, July 1983.

[6]. K.F. Klein, W.E. Heinlein, Application of Transform Techniques to Digital Line Codes and Data Transmission", Electronics Letters, vol.18, no. 22, October 1982

[7]. N.Q. Duc, B. M. Smith, "Line Coding for Digital Data Transmission", Australian Telecommunication Research, vol. 11(2), 1977.

[8]. B.P. Lathi, "Modern Digital and Communication System" Third Edition.

[9]. Simon Haykins, "Communication System". Fourth Edition

[10]. J.Bhaskar, "A VHDL Primer". Third Edition, Person Education, Prentice Hall, 2008.