TEMPERATURE ANALYSIS OF LNA WITH IMPROVED LINEARITY FOR RF RECEIVER

Suvarna Gulab Shimpi[1], Subha Subramaniam[2], Vidya Gogate[3]

[1]*Shah and Anchor Kutchhi Engineering College, M.E. Electronics, Mumbai University, Maharashtra, India*
[2]*Shah and Anchor Kutchhi Engineering College, Department of Electronics, Mumbai University, Maharashtra, India*
[3]*Shah and Anchor Kutchhi Engineering College, Department of Electronics, Mumbai University, Maharashtra, India*

Abstract

In this paper we are fully integrated 5.5 GHz high-linearity low noise amplifier (LNA) is designing using post-linearization technique, in sub-120nm & sub-70nm technology. It developed using cascode amplifier with inductors. RC linearization circuit is designed to improve the linearity of the design. Cascode LNA circuit is designed for linearity improvement. In this work Temperature analysis is carried out for LNA circuit performance improvement fully integrated 5.5 GHz high-linearity low noise amplifier (LNA) is designing using post-linearization technique, in sub-120nm & sub-70nm technology.

Temperature stability of the circuit is analysed for different temperature ranges our results prove that the proposed LNA design achieve high gain with good linearity. Although power dissipation of the circuit is high, good temperature stability is achieved. Temperature stability of the circuit is analysed for different temperature ranges our results prove that the proposed LNA design achieve high gain with good linearity. Although power dissipation of the circuit is high, we are able to achieve good temperature stability. The Low Noise Amplifier is a special type of electronic amplifier used in communication systems which amplifies very weak signals captured by an antenna.

Keywords: *Linearity improvement LNA circuit, DSCH and Microwind software.*

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1. INTRODUCTION

Recently, telecommunication systems require high performance, low noise, low power, and highly linear RF integrated circuits [1]. Since the digital modulation scheme requires highly linear RF front-end circuits, the linearity requirement of the LNA becomes more stringent. Owing to possible large interference signal tones at the receiver end along with the carrier, the LNA is expected to provide high linearity, thus preventing the intermodulation tones created by the interference signal from corrupting the carrier signal. Moreover, the high linearity should be achieved in combination with a high gain and low current consumption. However, its poor linearity limits its usage to high-jammer applications.

To improve the linearity of the cascode LNA, several linearization methods have been proposed. Multiple gated transistors (MGTR) techniques is introduced by Kim, T. W., B. Kim, and K. Lee [2], which falls under the category of feed forward, uses two transistors connected in parallel and biased in weak and strong inversion region, respectively. The folded cascode PMOS topology has been proposed by Kim, T. S. and B. S. Kim [3]. Moreover, this topology has the advantages of low transconductance and low current consumption. Another linearization method, post-linearization technique, is introduced by Zang, H., X. Fan, and E. S. Sinencio [4]. This linearization technique uses a diode connected NMOS transistor to apply to a cascode common gate (CG) LNA, and the linearity performance looks good. However, by applying this technique to a cascode CS LNA, the linearity improvement is needed at the penalty of degrading the gain and current consumption.

In a common source (CS) circuit, the cascode topology is often employed to provide high gain and high reverse isolation. cascode stage Gain can be increased by increasing the length of the input transistor for a given bias current. Note that the transconductance of M1 becomes half and leading to higher noise. The application of cascode topology is in building constant current sources Published by Behzad Razavi [12].

In this paper, we present a post-linearization technique for the cascode CS LNA with the comparison of sub-70nm and sub-120nm technology. In the proposed method, sub-70nm technology circuit Gain and power dissipation is almost constant for variations of temperature, which is suitable for the high-frequency and high-linearity cascode CS LNAs.

2. DETAIL OF CMOS LNA

The schematic diagram of the proposed LNA is shown in Fig. 1. The idea behind the cascode structure is to convert the input voltage to a current and apply the result to a common gate stage. Transistor in a common source arrangement converts a voltage signal to a current signal. The cascade of a CS stage and a CG stage is called a "cascode" topology. The basic configuration: M1 generates a small signal drain current proportional to Vin and M2 simply routes the current to RD. M1 is the input device and M2 is the cascode device. An important property of the cascode structure is its high output impedance. Voltage gain of the cascode stage is equal to that of common source stage.

The inductive source degeneration structure provides simultaneous input matching. At higher frequencies, the device capacitances, such as gate-to-source, gate-to-drain, drain-to-substrate and source-to-substrate capacitances, significantly affected the current-voltage relationship. The input impedance seen from RFin of LNA is the same with and without the linearization circuit (L.C.) refered from [4]. The degradation in gain and current consumption is not severe because the transconductance and bias current of the linearization circuit are much smaller than those of the cascode stage.

An important property of the cascode structure is its high output impedance [12]. The circuit can be viewed as a common source stage with a degeneration inductor. M2 boosts the output impedance of M1. Cascoding can be extended to three or more stacked devices to achieve higher output impedance. It is also interesting to compare the increase in gain due to cascoding with that due to increasing the length of the input transistor for a given bias current. Transistor Ma, Resistor R1 and Capacitor C1 this components are use for linearization. For example, that the length of the input transistor of CS stage is quadrupled while the width remains constant.

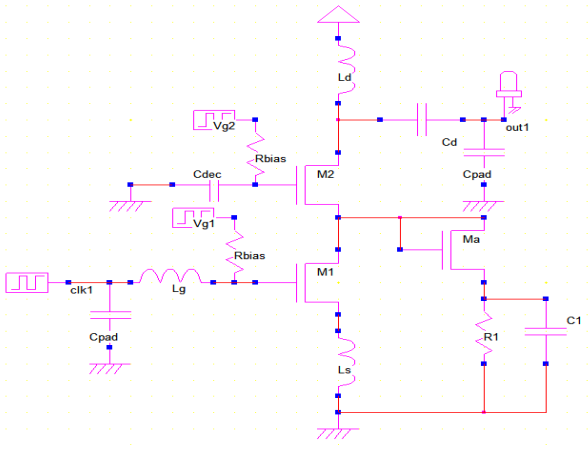


Fig 1 Schematic diagram of the proposed LNA [11]

3. EXPERIMENTAL RESULTS AND DISCUSSION

The LNA under this study was fabricated with a standard sub-120nm & sub-70nm CMOS technology on a p-type substrate. The proposed LNAs consume only 10mW (sub-120nm tech) & 6.58mW (sub-70nm tech) DC power supply voltage of 1V. For comparison, the LNAs with different temperature are realized.

Table1 Performance comparison with sub-70nm & sub-120nm Technology of LNA with Temperature

	Sub-120nm tech		Sub-70nm tech	
Temp in °C	Gain in dB	power dissipation in uW	gain in dB	power dissipation in uW
15	10.7	22.16	14.1	31.56
20	10.2	22.77	13.9	31.59
25	9.7	23.37	13.7	31.67
30	9.1	23.95	13.5	31.8
35	8.5	24.52	13.4	31.97
40	7.8	25.4	13.2	32.2

The measured gain, Power dissipation, and output voltage of the LNAs are plotted in the following Figures.

The gains are approximately 9.7 dB and 13.7 dB, respectively, sub-120nm & sub-70nm Technology at 5.5 GHz. The power dissipation of the LNAs are approximately and 23.37 uW & 31.67 uW, respectively, sub-120nm & sub-70nm Technology at 5.5 GHz.

Here we are comparing the gain of the LNA circuit with two different technologies with temperature

Table 2 – Analysis of AV in terms of temperature and frequency for different biasing voltages (sub-120 nm technology)

Biasing voltage in volts	Vb1= 0.5V, Vb2 = 1.05V			Vb1= 0.5V, Vb2 = 1V		
Temp in °C	Gain in dB	power dissipation (uW)	Vout (Volt)	Gain in dB	power dissipation (uW)	Vout (Volt)
15°C	10.7	22.16	0.343	11.9	54.077	0.397
20°C	10.2	22.77	0.324	11.8	54.247	0.394
25°C	9.7	23.37	0.305	11.6	54.414	0.382
30°C	9.1	23.95	0.286	11.5	54.76	0.381
35°C	8.5	24.52	0.267	11.2	55.85	0.367
40°C	7.8	25.4	0.246	11.1	55.97	0.366

By keeping biasing voltage Vb1 constant and a small change in biasing voltage Vb2. By keeping Resistor of RVb2 constant and reduce the Resistor of RVb1, power dissipation of the circuit can be change.

It means that, Voltage gain of the circuit changes by varying biasing voltages, as biasing voltage varies it changes current Idd also. As we change the value of biasing resistors it affects the power dissipation of the circuit. Small change in biasing voltage changes the Voltage gain.

Table 3 - Analysis of AV in terms of temperature and frequency for different biasing voltages (sub-70nm technology)

	Vb1= 0.5V, Vb2 = 1.05V			Vb1= 0.5V, Vb2 = 1V		
Temp in °C	gain in dB	power dissipation (uW)	Vout (Volt)	gain in dB	power dissipation (uW)	Vout (Volt)
15°C	14.1	31.56	0.508	18	28.075	0.792
20°C	13.9	31.59	0.497	18	28.095	0.788
25°C	13.7	31.67	0.488	17.9	28.1	0.786
30°C	13.5	31.8	0.479	17.9	28.099	0.785
35°C	13.4	31.97	0.47	17.8	28.1	0.774
40°C	13.2	32.2	0.462	17.8	28.146	0.774

For Table – 3 By keeping biasing voltage Vb1 constant and a small change in biasing voltage Vb2, gives use large change in Voltage gain.

Table 4 Comparison of Vout performance of the (sub-70nm & 120nm tech) LNA with temp

Temperature in °C	Sub-70nm tech Vout in Volt	Sub-120nm tech Vout in Volt
15	0.508	0.343
20	0.497	0.324
25	0.488	0.305
30	0.479	0.286
35	0.47	0.267
40	0.462	0.246

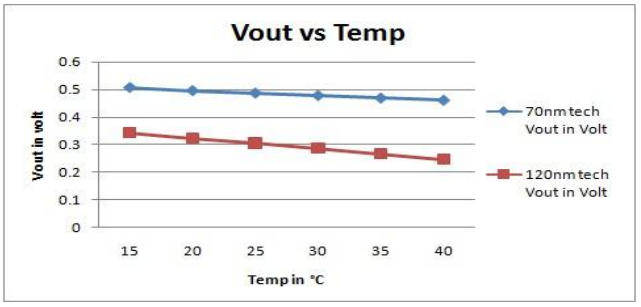


Fig 2 Compared Vout performance of the (sub-70nm & sub-120nm tech) LNA with temp.

From table4, as temperature increases output voltage decreases. It means the performance of the output voltage is dependent on the temperature. The output voltage of the sub-70nm technology is higher than the sub-120nm technology. This compared with the graph as shown in figure 2.

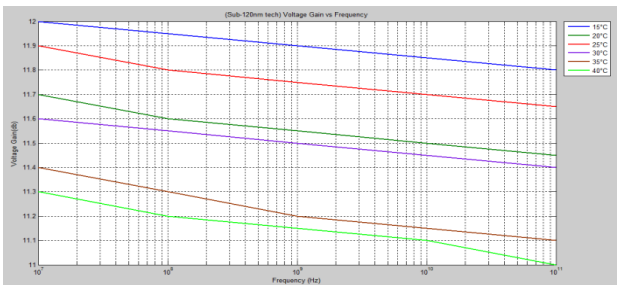
It is also interesting to compare the increase in gain due to cascading with that due to increasing the length of the input transistor for a given bias current. The length of the input transistor of a CS stage is quadrupled while the width remains constant. The application of cascode topology is in building constant current sources. The linearization is obtained at the cost of lower gain and higher noise.

However, the input device and the cascode device need not be of the same type. Instead of NMOS we can use PMOS.

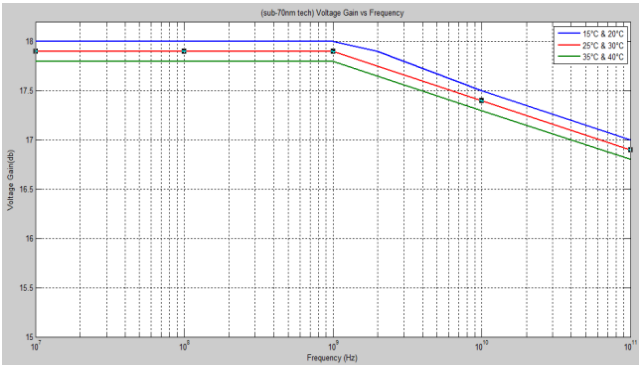
The comparisons of the circuit performance with the recently published LNAs with 25°C temperature are summarized in Table 5.

Table 5 Performance comparisons with the recently published LNAs

Technology	120nm	70nm
Gain in dB	9.7	13.7
Pdc in mW	10	6.58
Output voltage in Volts	0.305	0.488
PowerDissipation in uW	23.37	31.67



(a) sub-120nm



(b) sub-70nm

Fig 3 Voltage Gain (dB) vs Frequency (Hz) of linearity improvement LNA circuit

From figure 3 Linearity Improvement LNA implemented and simulated on sub-120nm tech & Sub-70nm technology. The simulation result shows that as temperature of the circuit increases the Voltage Gain reduces.It should be noted that the proposed LNAs are fully integrated without off-chip components. The proposed technique usable at higher frequency range

Equations

$$\text{Gain} = \frac{\text{Vout}}{\text{Vin}} \quad \text{in dB} \qquad (1)$$

4. CONCLUSIONS

From our simulation results depicts the fact that the down scaling in VLSI technology increases gain for sub-70nm in comparison with the same implementation in sub-120nm. We have designed and shown a improved linearity improvement circuit for LNA with better gain.

The design shows temperature stability with increased gain. The limitation of this design is with the power dissipation of the circuit.

We are proving again the well known fact that the down scaling improves gain.

The proposed linearization technique adopts an additional folded diode with a resistor and capacitor in parallel.

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BIOGRAPHIES

Suvarna Gulab Shimpi M.E. Electronics, SAKEC, Mumbai University, Mumbai, India
suvilas@gmail.com

Subha Subramaniam Associate Professor, SAKEC, Department of Electronics, Mumbai, India
subhasubramaniam@yahoo.co.in

Vidya Gogate, Assistant Professor, SAKEC, Department of Electronics, Mumbai, India
vidyagogate@gmail.com