LOC, LOS AND LOES AT-SPEED TESTING METHODOLOGIES FOR AUTOMATIC TEST PATTERN GENERATION USING TRANSITION DELAY FAULT MODEL

Parth Borda[1], Pankaj Prajapati[2]

[1]*M.E, Department of Electronics & Communication, L.D.College of Engineering, Gujarat, India*
[2]*Assistant Professor, Department of Electronics & Communication, L.D.College of Engineering, Gujarat, India*

Abstract

Faults, caused by timing-related defects in very large scale integrated circuits, are important to detect to optimize coverage and test time. Delay faults are only due to timing malfunction. At-speed test is only method to detect these delay faults. This paper describes and compares different at-speed testing techniques on vivid point of views along with them practical implementation. This paper also shows results generated by automatic test pattern generation tool for these techniques. Next, generated test patterns are simulated by using simulator and correctness of these methods are verified.

Keywords: *LOC (Launch on capture), LOS (Launch on shift), LOES (Launch on extra shift), At-speed testing.*

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1. INTRODUCTION

Down scaling of feature sizes in current submicron technology results in high operating frequencies and clock speeds. For this current VLSI technology, testing of only stuck-at fault is not sufficient. It is very important to detect faults produced by timing-related defect, which cannot be detected by ATEs whose frequency are lower than operating frequency of design. Timing related defect causes delay faults like transition delay fault and path delay fault. They can only be detected when testing frequency is same as functional frequency. This type of testing of design is called At-Speed testing. Transition delay model and path delay model are two widely used at-speed model today. [6][7]

Unlike stuck-at fault test, at-speed test requires two test vectors or test patterns. First pattern initialize or active the fault at input of combinational logic block and second pattern launch transition in the logic value at fault site and propagate this transition to the outputs of the combinational block which are captured back in the scan chains. For an example, as shown in figure-1, second output signal cannot be detected because it is exerted by delay fault. Delay test can be classified based on how second vector is obtained as Launch on shift test (Skewed load delay test), Launch on capture test (Broad side delay test) and Launch on extra shift. [6]

This section-I introduce transition and path delay faults, delay fault models and at-speed testing. Section-II explains LOC and LOS techniques for transition fault detection along with their advantages and disadvantages. Also we discuss importance of them in the design. Section-III explains LOES technique in detail along with its benefits and its comparison with other two techniques. Section-IV shows practical results and simulations of these delay fault detection techniques. And section-V concludes the paper by comparing all techniques.

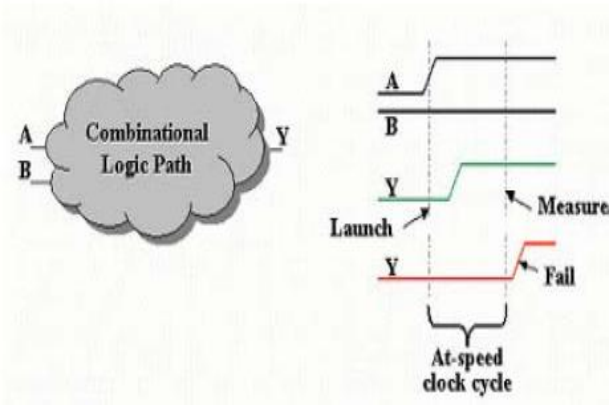


Fig-1: At-speed testing for a pattern (Pass – if transition captured and Fail – if transition not captured) [6]

1.1 Transition Delay and Path Delay Fault Models

Transition fault model assumes only one gate is affected by slow-to rise fault and slow-to-fall fault. In faulty circuit, each gate has nominal delay and in the faulty circuit, any gate is exerted by high value of this delay. So under transition delay fault model, extra delay caused by delay fault is large enough. Hence signal cannot make transition within time of observation at primary output of combinational block. This transition delay fault is observed independently, whether it is

propagated through short or longer path, at output. The advantage of this fault model is that number of faults in the circuit are relatively small or linear in terms of the number of gates. [1]

In the path delay fault model, circuit is behave like faulty if the delay of any of its path exceeds threshold limit. The delay defect on a path is detected by propagating transition through the path therefore transition is applied at the begging of the path. The limitation of path delay fault model is that number of paths in the circuit are very large. One strategy commonly is used for path delay fault testing is to select all paths which delays are greater than specified threshold. The reason of selecting the longer path is that the defects on shorter paths might not affect the circuit behaviour and if it large enough to affect circuit performance, it would be detected by transition delay fault test. [1]

2. LAUNCH ON CAPTURE (LOC) and LAUNCH ON SHIFT (LOS)

Main transition fault ATPG methodologies are Launch on Capture and Launch on Shift (also known as broadside-load and skewed-load respectively). They both launch transition at the input of combinational block in different way for the same fault detection.

As shown in figure-2, two vectors V1 and V2 are used to perform transition delay fault testing. Here figure-2(a) describes the LOC waveform. As illustrated, last shift of scan chain initialize the inputs of combinational block and first functional clock is used to launch transition in the combination block (here scan enable signal is de-asserted after V1).

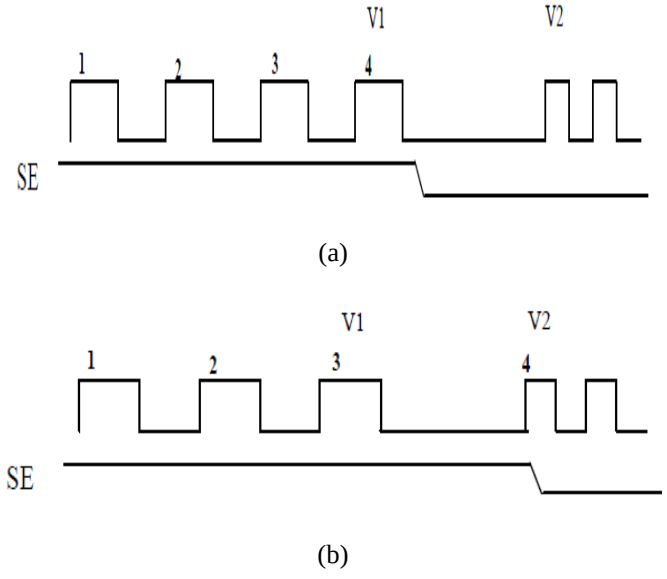


Fig-2 (a): LOC Waveform (b) LOS Waveform [2]

Second functional clock would captures the propagated transition at the output. Then scan enable signal would asserted. Example, for scan chain having N scan-length, in LOC, first vector of N bit is loaded in to scan chain by N slow clock. Then two fast clock (functional clock) are used to launch and capture transition into and from the combinational block. Again scan chain unloads with N slow clocks. Here scan enable signal transit from high to low after last shift of loading process. So, launch clock always occur in function mode and launching of transition would be along function path.

Now in LOS, launching of transition is different than LOC. In LOS, as shown in figure-2(b), last shift clock is used as second vector to launch transition in combinational block. Here during launching scan enable signal remains asserted so transition is launched along shift path. Let's take scan chain of scan-length N as an example, under the LOS methodology, first N-1 bits of vector are loaded (shifted-in into scan chain) by slow clock would initialize the logic value at input of combinational block and Nth shift with fast clock would launch transition. Then scan enable signal goes low. After that fast capture clock comes as shown in figure-2(b). Again slow clock is used to unload the scan chain.

2.1 Pros and Cons of LOC and LOS

1) In LOC, V2 is generated by applying functional clock from V1 whereas in LOS, V2 is shifted vector of V1. And to launch transition on shift path is very easy than to launch transition on functional path.
2) LOC techniques uses sequential engine during automatic test pattern generation (ATPG) whereas LOS uses combination engine for ATPG. So LOS requires to do some extra setup to perform ATPG.
3) In LOS, the fault activation path or scan path is fully controllable from the input of scan chain while in LOC, controllability of launching transition at fault site is less (its depends on the functional response of logic blocks to initialize vector) results LOS give better controllability cause better fault coverage and less patterns than LOC.
4) In LOC, after all slow clocks for loading there is dead clock zone so, scan enable signal can easily make transition from high to low. But in case of LOS, fast scan enable signal must design to make transition between two high speed clocks means scan enable signal must operate at full speed. This will increase cost of testing. As solution of this problem in LOS, pipelined architecture is used for scan enable signal. This scan enable signal is called pipelined scan enable signal. [2]
5) In LOS, last shift happen with fast clock and entire design will become active result average power in launch cycle is very high.
6) In LOS, lash shift would happen at high speed clock will force to place additional timing requirements on an On chip Clock (OCC) controller in multi-clock domain design.

3. LAUNCH ON EXTRA SHIFT (LOES)

LOES – Launch on Extra shift is delay fault test technique used to solve problems of LOS methodology already mentioned. In LOES methodology, transition is launched by extra fast shift clock at inputs of combinational block as shown in figure-3. In case of scan chain having N bit scan-length, N slow shift clock cycle require to load entire scan chain and (N+1)th fast shift clock is used to launch the transition.

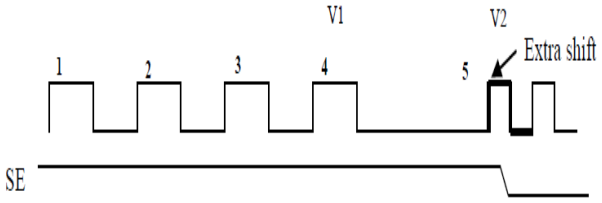


Fig-3: LOES Waveform [2]

Then fast functional clock happens to capture response after scan enable signal goes low. So, in LOES, extra shift and capture clocks are at-speed clocks. Essentially, loading-unloading processes of LOES are similar to LOC whereas launching process is same as LOS because transition is launched through shift path. [2]

3.1 Comparisons with LOC and LOS

1) Since in LOES, transition is launched by an extra shift this methodology is as efficient as LOS in terms of coverage and test patterns.
2) LOES also uses sequential engine to perform ATPG like LOC and all ATPG setup are same as LOC.
3) LOES also has a same problem scan enable signal as shown in LOS that scan enable signal must be design to operate at high speed. And also pipelined scan enable signal requires as solution that need pipelined architecture.
4) In LOES, all bits of patterns are shifted into scan chain through slow clocks so, unlike LOS, LOES doesn't need additional timing hardware on an OCC controller.

3.2 Pipelined Structure for LOS and LOES Methodologies

As we have discussed earlier, transition of scan enable signal between two function frequency clocks would increase the cost of testing and also it is very difficult with low speed ATEs. So, pipelined scan enable signal is a solution for that. Figure-4 illustrates the structure of pipelined scan enable signal normally used for LOS and LOES techniques and waveforms for same.

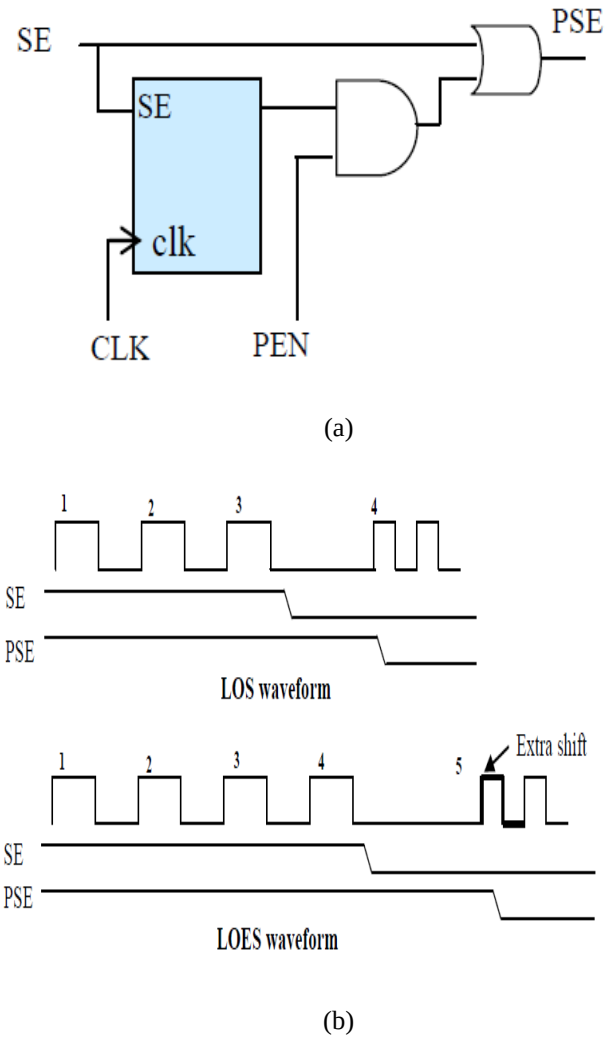


Fig-4: (a) Scan Enable Pipelined Circuitry (b) waveforms of pipelined scan enable signal for LOS and LOES [2]

Above figure-4(a) shows implementation of pipelined scan enable signal in ASIC design. SE is controlled by external tester and PSE is pipelined scan enable signal is internally generated and is forwarded to all scan enable pins of scannable flops available in scan chain. Here PEN is pipelined enable signal. It is generally high to active pipelined structure during LOS and LOES automatic test pattern generation. It remains low during LOC because it gives same logic values on SE and PSE pins. So, low logic value on PSE would deactivate pipelined structure.

Figure-4(b) shows even-though for LOS and LOES external tester make transition in scan enable (SE) signal before launch shift, pipelined scan enable (PSE) signal switches between two fast clocks. This would solve the problem of requirement of costly external signal to operate top level scan enable signal at functional speed.

4. RESULTS AND SIMULATIONS

Here below figure-5 shows results of one VLSI design in terms of fault coverage and number of test patterns for LOC, LOS and LOES methodology which are generated by automatic test pattern generation tool.

fault class	code	#faults
Detected	DT	145114
Possibly detected	PT	2875
Undetectable	UD	1802
ATPG untestable	AU	5244
Not detected	ND	18939
total faults		173974
test coverage		85.12%
fault coverage		84.24%

Pattern Summary Report

#internal patterns	4199
#fast_sequential patterns	4199

(a)

fault class	code	#faults
Detected	DT	159811
Possibly detected	PT	4
Undetectable	UD	1692
ATPG untestable	AU	12259
Not detected	ND	208
total faults		173974
test coverage		92.76%
fault coverage		91.86%

Pattern Summary Report

#internal patterns	1601
#basic_scan patterns	1601

(b)

fault class	code	#faults
Detected	DT	166705
Possibly detected	PT	58
Undetectable	UD	1802
ATPG untestable	AU	4498
Not detected	ND	911
total faults		173974
test coverage		96.84%
fault coverage		95.84%

Pattern Summary Report

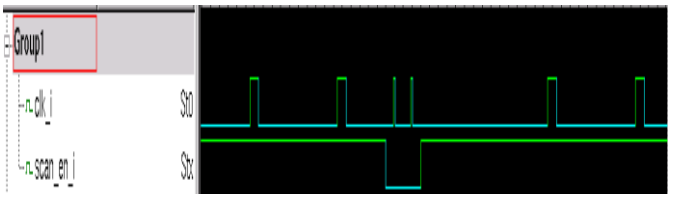
#internal patterns	3249
#fast_sequential patterns	3249

(c)

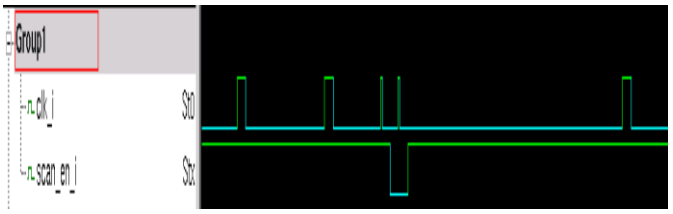
Fig-5: Fault coverage and Number of test patterns for (a) LOC, (b) LOS and (c) LOES

As shown in above figure, it becomes very easy to compare these three techniques.

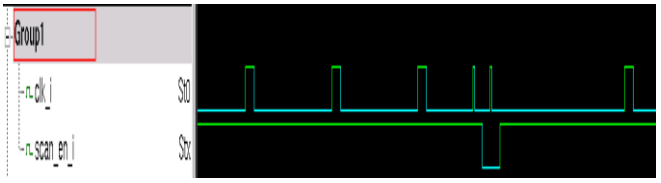
Here as per our discussion LOS and LOES are efficient methodologies in terms of test coverage and test patterns but major disadvantage of both is its implementation is difficult because they require fast scan enable signal.



(a)



(b)



(c)

Fig-6: Simulated waveforms of a test pattern for (a) LOC, (b) LOS and (c) LOES

Also figure-6 shows simulated waveforms for all these techniques that verifies correctness of these methodology. These are similar to our theoretical waveform discussed above. In this figure-6, launch and capture clock cycles of one pattern are shown.

5. CONCLUSIONS

In this paper, we studied an effective and practical transition and path delay testing methodologies. This paper also convey the basic understanding of LOC, LOS and LOES transition delay testing techniques along with their comparison. The main goal of this paper is to give brief about benefits and difficulties, of these three methodologies, we need to consider during delay testing and automatic test pattern generation. Also results compare these methods in terms of coverage and number of test patterns.

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