A 2.4 GHZ CMOS LNA INPUT MATCHING DESIGN USING RESISTIVE FEEDBACK TOPOLOGY IN 0.13μm TECHNOLOGY

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Abstract

The attempt made in the paper shows an innovative designing for the enhancement and reliability in CMOS technology. A 2.4 GHz resistive feedback narrowband noise amplifier (LNA) using a series inductor input matching networks. It is easy reliable with an extra g_m boosting as well as inductively degenerated topology. By using this resistive feedback topology increases the gain as well as noise figure of 2.2 dB,S_{21} parameter of 26dB,and IIP3 of -13dBm,while 2.8mW of power consuming from a 1.2V and its area 0.6mm^2 in 0.13µm CMOS ,which gives the best figure of merit and performance.

Keywords: *LNA, CMOS, noise figure, resistive feedback, g_m boosting, voltage gain boosting.*

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1. INTRODUCTION

Still the challenge is CMOS radio frequency (RF) front end circuit is for high performance, low cost, low power consumption [1]-[7]. The topologies like inductively coupled degenerated common source. LNA [3], and the resistive feedback LNA have their own advantages and disadvantages with limitations. In order to overcome the limitations so many designs have been implemented and investigated.

By using inductively degenerated narrow band systems low NF, ease of input matching, high gain and low power consumption[8]. However due to inductor at gate and source the input device large inductance values would be required and also occupies large chip area due to these RF LNA provides wideband input and output matching and small die area because no inductor is required for input matching.

The input matching can be a series resonator circuit for the RF front end to an external device antenna, an RF switch as shown in below figure 1.It can generate Q-times if voltage gain across c_{gs} [1] to match the input impedance. At a resonant frequency w_0, the quality factor is given by $Q_L=(w_0\ L_{ser}/R_{ser})$and the voltage across the C_{ser} is jQ_LV_{in}.

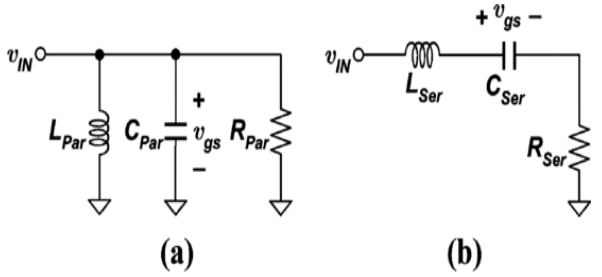


Fig (1) Input matching network (a) parallel RLC network (b) Series RLC network

In section I this paper proposed a resistive feedback topology LNA g_m boosting from inductively degenerated topology and input matching network from resistive feedback. Section II describes the proposed LNA concepts, noise analysis with small signal models. In section III implementation and experimental results of LNA conclusions are in section IV.

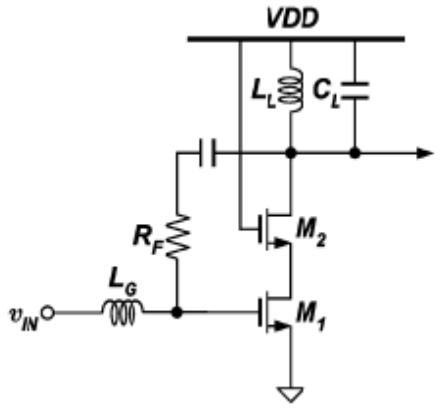
1.1 LNA Requirements:

1. Gain (10-20 db) to amplify the received signal and to reduce the input referred noise of the subsequent stages.
2. Good linearity: Handling large undesired signals without much distortion.
3. Low noise for high sensitivity
4. Maximum power gain 50 Ω termination for proper operation and can route the LNA to the antenna which is located an unknown distance away without worrying about the length of the transmission line [10],[12].

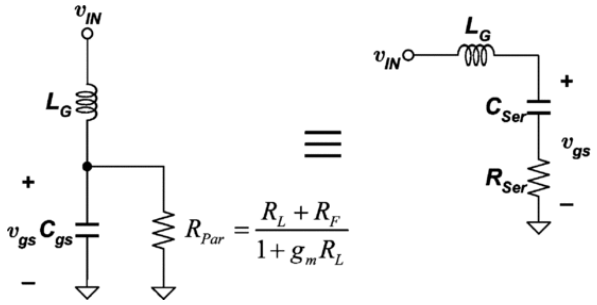
1.2 Basic Topologies

1. Wide band LNA input matching topologies (a) Resistive termination (b) common gate (c) resistive shunt feedback.
2. Narrow band LNA input matching topologies (a) inductive degenerated (b) resistive terminated [10] , [12].

1.3. Resistive Feedback LNA:



(a)



(b)

Fig 2(a): Resistive feedback low noise amplifier (b): equivalent input matching network

Fig(2) shows the RF LNA schematic ,the series RLC resonator matching for the resistive feedback topology, the input impedance at the gate of M_1 is converted into series network C_{res} and R_{ser} ,as shown in above fig. where C_{sc} is[12]

$$c_{gs}\left(1+\frac{1}{Q_L^{\,2}}\right),\ R_{\text{Series}}\ \frac{R_F + R_L}{\left(1+g_m R_L\right)\left(1+Q_L^{\,2}\right)},$$

R_L is output impedance $\frac{L_L}{C_L}$ at the operating frequency and is

$$Q_L\left(\frac{\omega_0 LG}{R_{series}}\right).$$

The series matching topology boosts the voltage gain at the gate M_1 by $(1\text{-}jQ_L)$ and hence the effective trans conductance is boosted by $\left(1+Q_L^{\,2}\right)$ this LNA can achieve a voltage gain by a factor of $\sqrt{\frac{\left(1+Q_L^{\,2}\right)}{Q_L^{\,2}}}$ when compared to L-degenerated LNA [12].

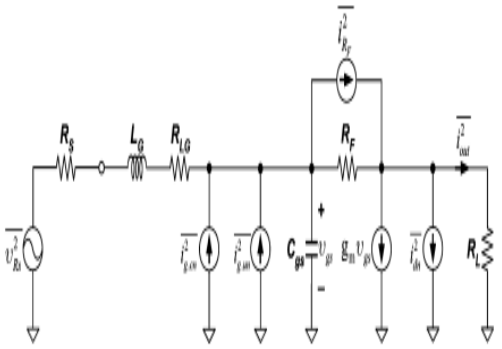


Fig: (3) Noise analysis of small signal model of the gm boosted resistive feedback.

From above fig 3.The input impedance [12]

$$z_{in} = sL_G + \left[\frac{1}{sC_{gs}} \square \frac{R_F + R_L}{1+g_m R_L}\right]$$

$$= sL_G + \frac{1}{sC_{gs}\left(1+\frac{1}{Q_L^{\,2}}\right)} + \frac{R_F + R_L}{\left(1+g_m R_L\right)\left(1+Q_L^{\,2}\right)} 1$$

z_{in} is equal to

$$\frac{R_F + R_L}{\left(1+g_m R_L\right)\left(1+Q_L^{\,2}\right)}$$ at resonant frequency $\omega_{o..}$

In this proposed LNA, the inductor at the source of M_1 is Eliminated compared with the inductive common source LNA .By removing this source inductor reduces the chip area. The typical q of a an integrated inductor is in the range of 5-20 [13].In order to reach noise figure 1 Db ,the parasitic ,such as substrate resistance ,ESD ,and series inductor resistance dominate the noise performance of LNA. This topology more freedom for the chosen of single inductor (L_G), with nice quality factor for high noise performance design aspect [14].

2. NOISE ANALYSIS

The small signal model of fig(3) is the gate resistance of the input resistor,M1 is neglected with consideration of gate impedance is capacitive ,and the blocking capacitor in the feedback path is shorted, since it has a small impedance at the required frequency R_L is the loss of gate inductor L_G .the transistor M_2 is not considered in case of the noise contribution

because of noise cancellation mechanism of cascade configuration of the transistor when the inverse trans conductance of the cascade .R_L is the load impedance when L_L and C_L resonate at the resonant frequency.

The noise factor calculation for designed topology is

$$F = 1 + \frac{R_{LG}}{R_S} + \frac{\left(R_F + 2R_L\right)^2}{R_F R_L^2 \left(1+Q_L{}^2\right) g_m{}^2 R_s} + \frac{\gamma}{\alpha\left(1+Q_L{}^2\right) g_m R_s} + \left(\frac{R_F + R_L}{R_L}\right) \frac{1}{\left(1+Q_L{}^2\right) g_m R_s} 2|c| \sqrt{\frac{\gamma\delta}{5}} \left(\frac{\omega_o}{\omega_T}\right) + \left(\frac{R_F + R_L}{R_L}\right)^2 \frac{1}{\left(1+Q_L{}^2\right) g_m R_s} \frac{\alpha\delta}{5} \left(\frac{\omega_o}{\omega_T}\right)^2 (2)$$

Where α is the ratio of device trans conductance and the zero bias drain conductance, where γ is the thermal noise factor, δ is the gate induced noise factor, C is correlation coefficient between drain noise and induced gate noise for long channel devices=1, γ=2/3, δ=4/3 and C=-j0.395[1], [14]. The important relation $(R_F+R_L)/(g_mR_L(1+Q_L{}^2))$ is equal to $R_s(g_mR_L>>1)$ for the narrow band LNA.

From fig(2), the input matching condition is applied , when $R_F>>R_L$, it can be assumed that $[(R_F+2R_L)/ (R_F+R_L)^2]=1$, at this condition noise factor function of Q_L can be expressed as

$$F = 1 + \frac{R_{LG}}{R_S} + \frac{1}{g_m R_L} + \frac{\gamma}{\alpha\left(1+Q_L{}^2\right) g_m R_s} + 2|c| \sqrt{\frac{\gamma\delta}{5}} \left(\frac{\omega_o}{\omega_T}\right) + \frac{\alpha\delta}{5} \left(\frac{\omega_o}{\omega_T}\right)^2 \left(1+Q_L{}^2\right) g_m R_s \quad (3)$$

The minimum noise factor and optimum Q factor is expressed by

$$F_{\min.p_D} = 1 + 2.30 \frac{\gamma}{\alpha} \left(\frac{\omega_o}{\omega_T}\right) (4)$$

And

$$Q_{Lopt} = |c| \sqrt{\frac{\gamma\delta}{5}} \left[\frac{1 + \sqrt{1 + \frac{3}{|c|^2} \left(1 + \frac{5R_S}{\delta R_L}\right)}}{\left(1 + \frac{5R_S}{\delta R_L}\right)} \right] (5)$$

Let α=1, C=-J0.395, γ =2.5 and α=5 for a short channel device [1] and R_S =50Ω,R_L=1KΩ then 4 and 5 equations become as

$$F_{\min.p_D} = 1 + 5.75 \left(\frac{\omega_o}{\omega_T}\right) (6)$$

$$Q_{Lopt} \cong 3.34 (7)$$

2.1 LNA Implementation

The complete schematic of the proposed resistive feedback LNA input matching topology designed in a standard 8 metal 0.18mm RF CMOS technology which is operated at 2.4 GHz shown in fig 4.the two stage cascaded architecture of a core amplifier and an open-drain output buffer. the cascade configuration of core amplifier have provided isolated and reduce the Miler capacitance in between gate and drain of the input device M1 with size 200μm/0.13μm which gives minimum NF, with 2 ma and 1.2 V supply for transistor biasing.

The M5 transistor M6 transistor which have thick gate oxide, high threshold and break down voltage to protecting the gate of the input device from electro static discharge(ESD)[15]. The ESD protection device improves the noise figure by 0.1 dB because of parasitic capacitance and finite output resistance. The total gate inductance is approximately 8.8 ηH .the feedback resistance R_F is 8.4 k Ω and load impedance is 8nH.the quality factor is10.

2.2 Simulated Results And Discussion:

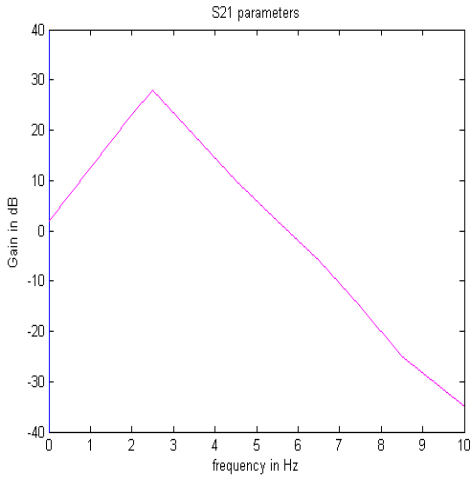
The fig (4) Shows the S-parameter.S_{11} of the designed LNA is -10.7dB,S_{21} is28.3 dB .The noise figure is 2.2dB ,the IIP3(third order interception point)including buffer is -22.4 dBm and table is given below

3. SIMULATION RESULT ANALYSIS

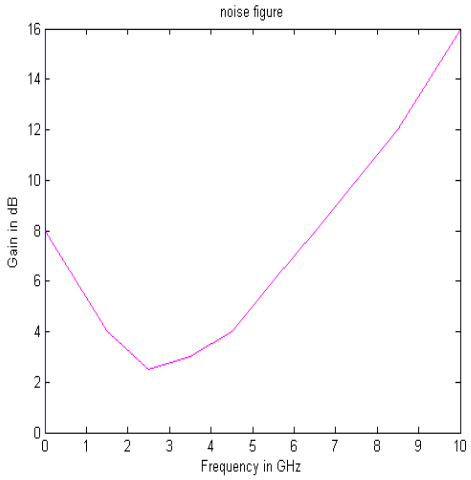
Table-1 parameters and performance

	Specs	Simulation
Frequency	2.4Ghz	2.4Ghz
S_{11}	-10dB	- 12 dB
S_{21}	28dB	28.7dB
NF	2dB	2.2dB
IIP3	10dBm	-22.4dBm
Power	4.8mw	4.8mw
Supply	1.2v	1.2v

The design was simulated using the ADS and also cadence tools provided for the 0.13μm RF CMOS process. The following graphs shows S21, S11, noise figure, IIP3, of resistive feedback topology LNA



(a)



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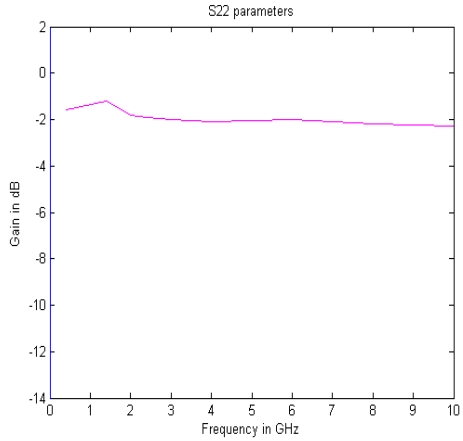

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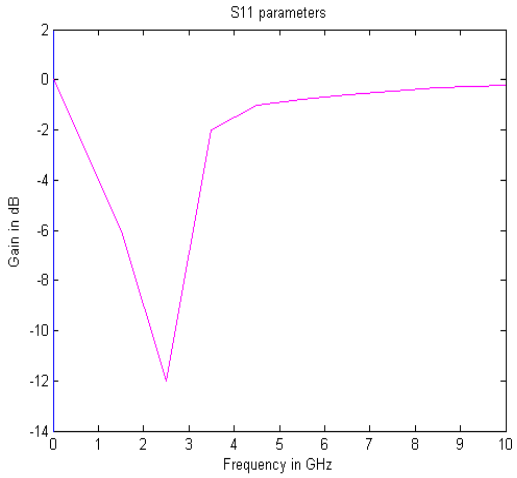

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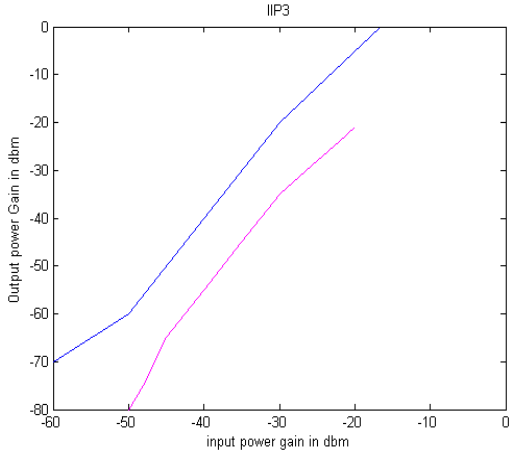

(e)

Fig 4 (a) S21 parameters (b) noise figure (c) S22parameters (d) S11Parameters (e) Third order intercept point

4. CONCLUSIONS

The design of receiver supporting 4G wireless applications in all bands presents many challenges. Some of the characteristics of the receivers are multi band multi standard operation, MIMO support, low power and low cost. By applying analytical mode lings for key performance parameters of LNA is required 4G front ends. This paper has presented the design of gain S_{21} 28dB with a noise figure 2dB while drawing 4.8mW power from 1.2 volts supply by using resistive feedback LNA topology. A lesson learned in this design is the importance of intuitive understanding of resonance and circuit theory, while the design of LNA is being made with wireless telemetry telecommand system and also for wireless sensor networks.

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